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Question Paper Code : 50481

B.E./B.Tech. DEGREE EXAMINATIONS, APRIL/MAY 2023.

Third Semester

Electronics and Communication Engineering

EC 8351 – ELECTRONIC CIRCUITS – I

(Common to : Electronics and Telecommunication Engineering)

(Regulations 2017)

Time : Three hours   Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Draw the DC load line and define operating point.

2. Sketch the voltage divider biasing circuit of E-MOSFET.

3. Define early effect.

4. State the advantages of unbypassed emitter resistor in CE configuration.

5. Write down the small signal parameters of JFET.

6. N channel FET's are preferred over P channel FET's. Justify.

7. For an amplifier, midband gain is 100 and lower cutoff frequency is 10kHz. Find the gain of an amplifier when frequency is 10Hz.

8. What is the relationship between bandwidth and risetime?

9. List the advantages and disadvantages of Half wave rectifier.

10. Why protection circuit is required for the regulator?

PART B — (5 × 13 = 65 marks)

11. (a) Elaborate the bias compensation techniques that use diode, thermistor and Sensistor to maintain constant operating point and explain in detail.

Or

(b) The amplifier shown in Figure 11(b). an n-channel FET for which, I_D=0.8mA, V_P= −2V, V_{DD}=24V and I_{DSS}=1.6mA. Assume that rd>Rd. Calculate the parameters V_{GS}, g_m and Rs.
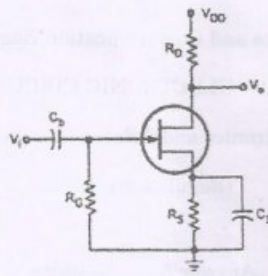

Figure 11(b)

12. (a) Draw the circuit diagram of common emitter amplifier with voltage divider bias, coupling capacitor and bypass capacitor. With the help of small signal equivalent, obtain the expression for current gain, voltage gain, input and output impedance.

Or

(b) Derive the expression of common mode rejection ratio of dual input, balanced output emitter coupled differential amplifier.

13. (a) Sketch the small signal hybrid π equivalent circuit of a common source amplifier with voltage divider bias and derive the expressions for voltage gain, input impedance and output impedance using small signal model.

Or

(b) Design and analyze the characteristics of BiCMOS cascade amplifier, and explain graphically the amplification process in a simple MOSFET amplifier circuit.

14. (a) For hybrid — π common emitter transistor model, derive the expressions for the short circuit current gain of common emitter amplifier at a high frequency.

Or

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(b) Describe the operation of high frequency common source FET amplifier with neat diagram. (5)

Also Derive the expression for

(i) Voltage gain (2)

(ii) Input admittance (2)

(iii) Input capacitance (2)

(iv) Output admittance (2)

15. (a) Explain the working of C filter with Full wave rectifier. Also derive the expression for ripple factor with and without C filter.

Or

(b) Analyse the following protection circuit that could be applied to voltage regulator.

(i) Fold back limiting circuit (7)

(ii) Over Voltage Protection (6)

PART C — (1 × 15 = 15 marks)

16. (a) Determine the small-signal voltage gain and input and output resistances of a common source MOSFET amplifier which has the parameter $V_{DD} = 10$ V, $R_1 = 70$ $K\Omega$, $R_2 = 29$ $K\Omega$, $R_D = 5 K\Omega$, $V_{TN} = 2$V, $K_n = 0.5$ mA/V² and $\lambda = 0.01$ V⁻¹. Assume $R_S = k\Omega$.

Or

(b) Design a bridge rectifier which is applied with input from a step down transformer having turns ratio 8:1 and input 230V, 50Hz. If the $R_f = 1 \Omega$, $R_S = 1 \Omega$ and $R_L = 2 k\Omega$. Find DC power output, PIV across each diode, Percentage efficiency and percentage regulation at full load.

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