Reg. No. : | | | | | | | | | | | | |

Question Paper Code : 50422

B.E./B.Tech DEGREE EXAMINATIONS, APRIL/MAY 2023.

Third Semester

Computer Science and Engineering

CS 8351 — DIGITAL PRINCIPLES AND SYSTEM DESIGN

(Common to Electronics and Telecommunication Engineering/ Information Technology)

(Regulations – 2017)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Implement AND gate using only NOR gate
2. State consensus theorem
3. Define combinational circuit
4. Draw the truth table of half adder
5. What is ring counter?
6. Define propagation delay
7. How is lockout avoided?
8. Compare static and dynamic hazards
9. Compare SRAM and DRAM
10. List the types of ROM.

PART B — (5 × 13 = 65 marks)

11. (a) Design and implement a 8241 to gray code converter. Realize the converter using only NAND gates.

Or

(b) Simplify AC'+ B'D+ A'CD+ ABCD in (i) SOP (ii) POS using K-map. (6+7)

12. (a) Explain the 4–bit adder with carry lookahead and design 2–bit magnitude comparator. (6+7)

Or

(b) Design a combinational circuit to perform BCD addition. Design a BCD to 7 segment decoder. (6+7)

13. (a) Design a modulo 5 synchronous counter using JK flipflop and construct its timing diagram.

Or

(b) Design a shift register using JK flipflops. Compare state table and excitation table. (9+4)

14. (a) Discuss the procedure for reducing the table with an example.

Or

(b) Explain the steps in designing asynchronous sequential circuits.

15. (a) Design a BCD to Excess–3 code converter and implement using PLA

Or

(b) Design a combinational circuit using ROM that accepts a 3 bit binary number and outputs a binary number equal to the square of the input number.

PART C — (1 × 15 = 15 marks)

16. (a) Implement the following Boolean functions with PLA.

F1 = AB'+ AC+ A'BC'

F2 = (AC + BC) '

Or

(b) Design a synchronous counter using JK flipflop to count the sequence 7,4,3,15,0,7.