Reg. No. : | | | | | | | | | | | | |

Question Paper Code : 10072

M.E./M.Tech. DEGREE EXAMINATIONS, APRIL/MAY 2023.

Elective

Applied Electronics

AP 4001 – APPLICATIONS SPECIFIC INTEGRATED CIRCUITS

(Regulations 2021)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. List the types of ASICs.
2. Compare combinational logic cell and sequential logical cell.
3. Distinguish between EPROM and E²PROM.
4. What is metal-metal anti-fuse?
5. Name the high-end and low-end FPGA family by Altera.
6. Mention the salient features of Stratix FPGAs.
7. Mention the placement goals in an ASIC design.
8. State any power and clocking strategies.
9. What are the advantages of SDRAM?
10. Write down the analysis and synthesis equation of DCT.

PART B — (5 × 13 = 65 marks)

11. (a) Draw and analyse the CMOS transistor circuit and explain its operation as switch. (13)

Or

(b) Elucidate the features and working of data path logic cell with neat sketches. (13)

12. (a) Compare and contrast on Actel, Xilinx and Altera devices with reference to logic modules and delay. (13)

Or

(b) Draw the architecture of Actel ACT and explain. (13)

13. (a) Draw and explain the architecture and configuration of Spartan low end FPGA family by Xilinx. (13)

Or

(b) Write a detailed note on the various signal probing techniques. (13)

14. (a) Illustrate the Eigen value placement algorithm with necessary mathematical analysis. (13)

Or

(b) Explain an end-to-end optimal floor plan for a Viterbi decoder with all necessary schematics? Also explain about measurement of delay. (13)

15. (a) Explain the design steps involved in high performance filters using delta-sigma modulators. (13)

Or

(b) Briefly explain on how SOCs are used in

(i) Digital cameras (7)

(ii) SDRAM (6)

PART C — (1 × 15 = 15 marks)

16. (a) Design and analyse a transistor circuit used as a resistor and derive the parasitic capacitance of transistor. (15)

Or

(b) (i) With necessary circuit diagram, explain the operation of SRAM. (8)

(ii) With an architectural diagram, explain Altera Flex. (7)