Reg. No. : | | | | | | | | | | | | |

Question Paper Code : 30148

B.E./B.Tech. DEGREE EXAMINATIONS, APRIL/MAY 2023.

Third Semester

Electrical and Electronics Engineering

EE 3302 — DIGITAL LOGIC CIRCUITS

(Regulations 2021)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. What is the best example of digital system?
2. Define Nibble and Byte.
3. Define Boolean algebra and Boolean Expression.
4. State De Morgan's theorem.
5. Difference between Combinational & Sequential Circuits.
6. What are the classifications of sequential circuits?
7. How can the hazards in combinational circuit be removed?
8. What is static 1 hazard?
9. What are the types of gate arrays in ASIC?
10. Give the different bitwise operators.

PART B — (5 × 13 = 65 marks)

11. (a) (i) Draw the circuit diagram and explain the working of TTL inverter with tristate out

(ii) Explain the concept and implementation of ECL logic family.

Or

(b) (i) Explain the operation of TTL NAND gate with a neat circuit diagram. (8)

(ii) Draw the circuit of CMOS NOR gate and explain its operation. Mention any two points about the advantages of CMOS over the other digital logic families. (5)

12. (a) Obtain the minimum SOP using K-map.

$F=M_0+M_2+M_4+M_8+M_9+M_{10}+M_{11}+M_{12}+M_{13}$

Or

(b) Using 8:1 multiplexer, realize the Boolean function
T=f (w,x,y,z) = m (0,1,2,4,5,7,8,9,12,13)

13. (a) A sequential circuit has four flip flops ABCD and an input x is described by the following state equations.

$A(t+1) = (CD'+C'D)x + (CD + (CD)')x'$

$B(t+1) = A$

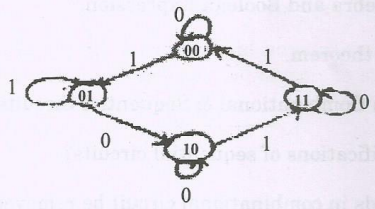
$C(t+1) = B$

$D(t+1) = C$

Obtain the sequence of states when x = 1 starting from state ABCD = 0001 Obtain the sequence of states when x = 10 starting from state ABCD = 0000

Or

(b) Design a synchronous sequential circuit using JK for the given state diagram.



14. (a) Develop the state diagram and primitive flow table for a logic system that has two inputs S and R and a single output Q. The device is to be an edge triggered SR flip-flop but without a clock. The device changes state on the rising edges of the two inputs. Static input values are not to have any effect in changing the Q output.

Or

(b) Design an asynchronous sequential circuit that has two inputs X_2 and X_1 and one output Z. The output is to remain a 0 as long as X_1 is a 0. The first change in X_2 that occurs while X_1 is a 1 will cause a Z to be a 1. Z is to remain a 1 until X_1 returns to 0. Construct a state diagram and flow table. Determine the output equations.

15. (a) Write a VHDL module that implements a full adder using an array of bit-vectors to represent the truth table.

Or

(b) (i) Write HDL behavioral description of JK flipflop using if- else statement based on value of present state. (8)

(ii) Draw the logic diagram for the following module. (5)

```
module seqcrt (A,B,C,Q,CLK);
input A,B,C,CLK;
output Q: reg Q,E;
always @ (Posedge CLK) begin E<= A&B;
Q <=E / C;
end end module
```

PART C — (1 × 15 = 15 marks)

16. (a) An asynchronous sequential circuit has two internal states and one output. The excitation and output functions describing the circuit are

$$Y_1 = X_1 + X_1Y_2' + X_2Y_1 \quad Y_2 = X_2 + X_1Y_1' \quad Y_2 + X_1Y_1, \quad Z = X_2 + Y_1$$

(i) Draw the logic diagram of the circuit. (5)

(ii) Derive the transition table and output map. (5)

(iii) Obtain a flow table for the circuit. (5)

Or

(b) Design an asynchronous binary toggle circuit that changes state with each rising edge of clock input. Assume the initial output as zero.

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