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Question Paper Code : 50496

B.E./B.Tech. DEGREE EXAMINATIONS, APRIL/MAY 2023.

Fifth Semester

Electronics and Communication Engineering

EC 8552 – COMPUTER ARCHITECTURE AND ORGANIZATION

(Common to: Electronics and Telecommunication Engineering)

(Regulations 2017)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Compare volatile and nonvolatile memory.
2. Define Amdhal's law.
3. Differentiate exception and interrupt.
4. Define sticky bit.
5. Why single cycle implementation is not used today?
6. What are imprecise and precise interrupts?
7. List the writing strategies in cache memory.
8. Define hit time and miss penalty.
9. What is a warehouse scale computer? List its characteristics.
10. List the difficulties while writing parallel processing programs.

PART B — (5 × 13 = 65 marks)

11. (a) (i) Consider a color display using 8 bits for each of the primary colors (red, green, blue) per pixel and a frame size of 1280 × 1024.

(1) What is the minimum size in bytes of the frame buffer to store a frame? (3)

(2) How long would it take, at a minimum, for the frame to be sent over a 100 Mbit/s network? (3)

(ii) What is addressing mode, explain the different types of addressing modes available? (7)

Or

(b) Consider three different processors P1, P2 and P3 executing the same instruction set. P1 has a 3GHz clock rate and a CPI of 1.5. P2 has a 2.5GHZ clock rate and a CPI of 1.0. P3 has a 4.0 GHz clock rate and has a CPI of 2.2. (5+4+4)

(i) Which processor has the highest performance expressed in instructions per second?

(ii) If the processors each execute a program in 10 seconds, find the number of cycles and the number of instructions.

(iii) If the execution time is reduced by 30%, which leads to an increase of 20% in the CPI. What would be the clock rate to get this time reduction?

12. (a) (i) Give the binary representation of the decimal number 63.25 assuming the IEEE 754 single precision format. (5)

(ii) Using 4-bit numbers to save space multiply $0010_2 \times 0011_2$ (8)

Or

(b) Add 0.510 and –0.437510 in binary using the binary floating point addition algorithm. (13)

13. (a) Design a simple data path with control implementation scheme and explain. (13)

Or

(b) (i) Discuss the three types of hazards in pipelining. (7)

(ii) Explain the schemes to resolve any two hazards. (6)

14. (a) Discuss the methods used to measure and improve the performance of the cache. (13)

Or

(b) (i) Draw and explain the timing diagram for synchronous and asynchronous bus data transfer. (8)

(ii) Consider a cache with 64 blocks and a block size of 16 bytes. To what block number does byte address 1200 map? (5)

15. (a) Draw and explain the block diagram of GPU architecture and compare CPU and GPU. (13)

Or

(b) What is hardware multithreading? Compare Fine grained and Coarse grained multithreading. (13)

PART C — (1 × 15 = 15 marks)

16. (a) (i) Calculate the total bits required for a direct mapped cache with 16KB of data and 4 word blocks, for a 32-bit address. (6)

(ii) For each code sequence given, check whether it must stall, can avoid stalls using only forwarding, or can execute without stalling or forwarding. (9)

Sequence 1	Sequence 2	Sequence 3
Id × 10, 0(×10)	add ×11, ×10, ×10	addi ×11, ×10, 1
add ×11, ×10, ×10	addi ×12, ×10, 5	addi ×12, ×10, 2
	addi ×14, ×11, 5	addi ×13, ×10, 3
		addi ×14, ×10, 4
		addi ×15, ×10, 5

Or

(b) (i) Explain Booth's multiplication algorithm with an example. (10)

(ii) Discuss the factors that affect the performance of a program. (5)

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