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Question Paper Code : 31518

M.E./M.Tech. DEGREE EXAMINATIONS, NOVEMBER/DECEMBER 2022.

First Semester

Applied Electronics

VL 4152 – DIGITAL CMOS VLSI DESIGN

(Common to : M.E. VLSI Design/M.E. VLSI and Embedded Systems)

(Regulations 2021)

Time : Three hours   Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Give the relation between voltages in cutoff, non-saturated and saturated regions of a CMOS device.

2. Draw the stick diagram of 2-input CMOS NAND gate.

3. Determine the logical effort of n-input NOR gate, assuming a pMOS-nMOS ratio of 2.

4. For the dynamic CMOS logic circuit shown below, determine the states of the transistors during the pre-charge and evaluation phase, and hence state the logic expression realized by the circuit.
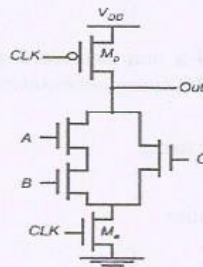
5. Draw the pipelined logic implementation of the expression $\log(|a + b|)$ and hence obtain the minimum allowable clock period for the circuit operation.

6. Discuss the bistability principle with reference to operation of two cascaded inverter.

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7. Design a one-bit left-right programmable shifter with nop condition using nMOS transistors.

8. List the techniques to reduce the power consumption in a complex CMOS logic circuit.

9. State the purpose of a floating gate transistor in a MOS memory cell.

10. Draw the CMOS implementation of a 1-bit SRAM cell.

PART B — (5 × 13 = 65 marks)

11. (a) For an n-channel MOS transistor with $\mu_n = 600\,cm^2/V.s, C_{ox} = 7*10^{-8}F/cm^2, W = 20\,\mu m, L = 2\,\mu m$ and $V_{TO} = 1.0\,V$, examine the relationship between the drain current and the terminal voltages.

Or

(b) Draw and explain the voltage transfer characteristics of CMOS inverters and hence obtain the expressions for noise margin NM_H and NM_L for symmetric CMOS inverter.

12. (a) Explain how transmission gates are used to overcome voltage problems in CMOS circuits.

Or

(b) Describe the working and characteristics of DCVSL logic gate.

13. (a) A C²MOS register with CLK − $\overline{CLK}$ clocking is insensitive to overlap, as long as the rise and fall times of clock edges are sufficiently small. Justify the above statement with appropriate explanation.

Or

(b) Discuss the working of a non-bistable sequential circuit and draw the characteristics of the CMOS implementation.

14. (a) Design a 4×4 multiplier using
    (i) Array multiplier
    (ii) Carry save multiplier

Or

(b) Design a 4-bit Carry-Lookahead Adder and hence obtain the CMOS implementation of the same.

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15. (a) Explain the operation of a CMOS RAM cell during read and write operation.

Or

(b) Discuss the advantages of applying differential sensing to an SRAM memory column.

PART C — $(1 \times 15 = 15$ marks$)$

16. (a) Consider a CMOS inverter with the following parameters

nMOS $V_{T0,n} = 0.6$ V $\mu_n C_{ox} = 60\,\mu A / V^2$ $(W/L)n = 8$

pMOS $V_{T0,p} = 0.7$ V $\mu_p C_{ox} = 25\,\mu A / V^2$ $(W/L)p = 12$

Calculate the noise margins and switching thresholds of this circuit. The power supply voltage is VDD = 3.3 V.

Or

(b) Design a combinational logic circuit for the following Boolean expression.

$$Z = \overline{A(D+E)+BC}$$

Obtain the required (W/L) ratio of nMOS and pMOS network.

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