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Question Paper Code : 90475

B.E./B.Tech. DEGREE EXAMINATIONS, NOVEMBER/DECEMBER 2022

Fourth Semester

Electronics and Communication Engineering

EC 8453 – LINEAR INTEGRATED CIRCUITS

(Common to : Biomedical Engineering/Medical Electronics/Robotics and Automation)

(Regulations 2017)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

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1. Define the need for Differential Amplifier compared to conventional Amplifier.
2. Why Active load is preferred compared to passive load in any Amplifier.
3. Draw the circuit to get the mentioned output using op-amp, $V_0 = -(0.2V_1 + 0.1V_2 + 10V_3)$.
4. If $V_{in} = 5V, R = 10k\Omega$ in a $V-I$ converter, Draw suitable circuit and find gain, I_L of op-amp circuit in non-inverting mode assume potential at non-inverting input is I, what is the output voltage?
5. Draw the pin diagram of AD 633 and list out alteast six Applications of Multiplier IC_S.
6. State the importance of Active filter in a PLL with neat sketches.
7. State various Applications of most commonly used ADC's.
8. The maximum frequency of input sine ware is 100 Hz and the conversion time is 10 μs (microsecond) for digitization. Determine Resolution of data converter.
9. What are linear voltage regulators and mention its limitations?
10. List the two modes of operation of 555 Ic timer.

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PART B — (5 × 13 = 65 marks)

11. (a) (i) Discuss the AC characteristics of an op-amp with suitable illustration, Explain Dominant pole compensation technique. (8)

(ii) Briefly explain the transfer characteristics of a differential pair with passive load. (5)

Or

(b) (i) With neat sketches, explain the block schematic of an op-amp IC 741. (8)

(ii) A 741 op-amp is used as an inverting Amplifier with a closed loop gain of 50. Find the maximum input signal that can be applied to get undistorted output if frequency response is constant upto 20 kHz? (5)

12. (a) (i) With neat diagram, Demonstrate the operation of a practical Integrator and derive an expression for gain. Plot the frequency Response. (8)

(ii) Discuss the Applications of V-I converter? (5)

Or

(b) (i) Explain the principle and operation of a Schmitt Trigger circuit with Transfer Characteristics? (8)

(ii) Design a wide band pass filter having $f_L = 400Hz$, $f_H = 2kHz$ and band pass gain of 4 find the Quality factor of the filter. (5)

13. (a) (i) Derive ΔI in terms of input voltages and emitter current I_{EE} and show that Gilbert cell can be used as Analog Multiplier. (8)

(ii) Explain the operation of a digital phase detector with relevant sketches. (5)

Or

(b) (i) With neat Block diagram, Explain the frequency multiplication and AM Detection using PLL? (8)

(ii) Design a four Quadrant analog multiplier using emitter coupled pair. (5)

14. (a) (i) Explain the operation of a Voltage Mode R – 2R DAC with suitable example. (8)

(ii) With neat sketches, Explain the operation of sample and hold circuit. (5)

Or

(b) (i) Explain the principle and operation of a 3-bit flash ADC with neat sketches. (8)

(ii) Discuss the need for sigma-delta converters and how it is better that other converters in terms of Resolution? (5)

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15. (a) (i) Explain the principle and operation of a Wein bridge Oscillator with neat sketches? (8)

(ii) With neat sketches Explain the functional block diagram of 723 Regulator? (5)

Or

(b) (i) Explain the functional Block diagram of MF 10 state variable IC with neat sketches. (8)

(ii) Write a note on the following, Video Amplifier and Opto couplers. (5)

PART C — (1 × 15 = 15 marks)

16. (a) (i) Design an astable multivibrator using 555 IC with Duty cycle 75% and $fo=50kHz$, assume $C=1\mu F$? (10)

(ii) Design a Differentiator that will Differentiate an input signal with $f_{max}=100Hz$, assume $C_1=0.1\mu F$. (5)

Or

(b) (i) Design a 3-Bit SAR type ADC with $V_{in}=6.5V$ tabulate the conversion process to show digital output? (8)

(ii) A VCO has a free Running frequency of $21KHz/v$ and input signal frequency $f_s=20kHz, K_v=4kHz/v$. Find the change in the dc control voltage V_C during the lock time? (7)

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