Reg. No. : | | | | | | | | | | | | |

Question Paper Code : 90468

B.E./B.Tech. DEGREE EXAMINATIONS, NOVEMBER/DECEMBER 2022

Third/Fourth Semester

Electronics and Communication Engineering

EC 8392 – DIGITAL ELECTRONICS

(Common to : Biomedical Engineering/Computer and Communication Engineering/Mechatronics Engineering/Medical Electronics/Robotics and Automation)

(Regulations 2017)

Time : Three hours Maximum :100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Subtract $(1010)_2$ from $(1111)_2$ using 2's complement method. Also verify result using direct method.

2. Map the given POS expression on K-map.
$f(A,B,C)=(A'+B'+C')(A+B+C)(A'+B+C)$

3. Construct Full adder using two half adders and obtain its truth table.

4. Draw 4 × 1 multiplexer using 2 × 1 Multilpexer and give its function table.

5. Differentiate Mealy and Moore type Sequential circuits.

6. Draw master-slave JK Flip Flop and mention how race condition is eliminated in master-slave JK Flip Flop.

7. Define race in Asynchronous sequential circuits. Give examples.

8. Differentiate Static-1 and Static-0 Hazard.

9. How many 16K × 4 RAMs are required to achieve a memory with a capacity of 64K and a word length of 8 bits?

10. Define Noise Margin and give the significance of Noise Margin.

PART B — (5 × 13 = 65 marks)

11. (a) Determine the sum of the product (SOP) and product of the sum (POS) forms for the Boolean expression $f(A,B,C)=\overline{A}B+\overline{B}C+\overline{A}\overline{C}$.

Or

(b) Obtain minimized sum of products for the Boolean expression $f=\Sigma(1, 2, 3, 7, 8, 9, 10, 11, 14, 15)$ using the Quine-McCluskey method. Also, verify the answer using K-map.

12. (a) Design a 4-bit Carry Look Ahead (CLA) adder and mention its applications.

Or

(b) Compare Decoder with encoder and design 3 to 8 decoder.

13. (a) Design a Mod-6 counter using JK Flip-Flop and draw timing diagram for the counter.

Or

(b) A Sequential circuit has two JK flip-flops, A and B; two inputs, x and y; and one output z. The flip-flop input functions and circuit output functions are as follows:

$J_A=Bx+B'y', K_A=B'xy', J_B=A'x, K_B=A+xy', z=Ax'y+Bx'y'$

(i) Draw the logic diagram of the circuit. (6)

(ii) Obtain the state table. (4)

(iii) Derive next state expressions for A and B. (3)

14. (a) Design an asynchronous circuit that produces output only when first pulse is received and ignores any other pulses.

Or

(b) An asynchronous sequential circuit has two internal states and one output. The excitation and output functions describing the circuit are

$Y_1=xy_1+x'y_2, Y_2=xy_1'+x'y_2$

(i) Draw the logic diagram of the circuit. (6)

(ii) Derive the output map and transition table. (4)

(iii) Obtain flow table of the circuit. (3)

15. (a) Explain with neat diagram, the operation of TTL 3-input NAND gate and discuss about totem pole configuration of TTL logic.

Or

(b) Explain the classification of ROM and RAM memories. Also, mention the applications of ROM.

PART C — (1 × 15 = 15 marks)

16. (a) Design a 3-bit Binary to Gray code converter using PLA. Also, compare PLA with PAL.

Or

(b) A clocked sequence circuit with single input x and single output z produces an output of $z = 1$ whenever the input x completes the sequence 1011 and assume overlapping is allowed. Design the Sequence detector and assume mealy model.

(i) Obtain state diagram

(ii) Obtain minimum state table and design circuit using D Flip flops.