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M.E./M.Tech. DEGREE EXAMINATIONS, NOVEMBER/DECEMBER 2022

First Semester

Applied Electronics

AP 4153 – SEMICONDUCTOR DEVICES AND MODELING

(Common to : M.E. VLSI Design)

(Regulations 2021)

Time : Three hours | Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Draw the energy band diagram of a MOS capacitor.

2. In VLSI fabrication process, how mobile ion contamination problem can be avoided?

3. Draw the typical MOSFET $I_{DS}-V_{gs}$ characteristics at low drain bias voltages.

4. Explain about the three regions of MOSFET operations.

5. An N-channel transistor has $V_t = 0.34V$ and $S = 85mV, W = 10\mu m$ and $L = 50nm$. Estimate I_{off}. Estimate I_{ds} at $Vg = 0.17V$.

6. What is the effect of scaling of MOSFET on circuit parameters?

7. What is the basic operation of a bipolar transistor?

8. Mention the Gummel plot of an n-p-n transistor (i.e., significant avalanche multiplication region).

9. Define the drift-diffusion equations for electrons and holes.

10. Define the mean electron velocity and effective mass tensor in n-th band.

PART B — (5 × 13 = 65 marks)

11. (a) Assume silicon, room temperature, complete ionization. An abrupt p-n junction with $N_a = N_d = 10^{17} cm^{-3}$ is reversed biased at 2.0 V.

Draw the band diagram. Label the Fermi levels and indicate where the voltage appears.

What is the total depletion layer width?

What is the maximum field in the junction?

Or

(b) Consider an MOS device with 20nm thick gate oxide and uniform p-type substrate doping of 10^{17} cm^{-3}. The gate work function is that of $n^{+}Si$.

What is the flat band voltage? What is the threshold voltage for strong inversion?

Sketch the high frequency C-V curve. Label where the flat band voltage and threshold voltage are.

Calculate the maximum and minimum capacitance (per area) values.

12. (a) Mathematically explain the dependance of MOSFET threshold voltage on substrate bias and temperature.

Or

(b) The effective field plays an important role in MOSFET channel mobility. Show that effective field represented below leads to the following expression

$$\mathscr{E}_{\text{eff}} = \left(|Q_d| + |Q_i|/2\right)/\varepsilon_{si}$$

$$\mathscr{E}_{\text{eff}} \equiv \frac{\int_0^{x_i} n(x)\, \mathscr{E}(x)\, dx}{\int_0^{x_i} n(x)\, dx}$$

Assume that the below equation follows Gauss Law.

The inversion layer depth x_i is assumed to be much smaller than the bulk depletion width.

13. (a) Consider a uniformly doped nMOSFET of $N_a = 10^{18}$ cm^{-3} biased at the threshold condition. Calculate the first three quantum mechanical energy levels for inversion electrons in the lower valley with an effective mass of 0.92m$_0$. m$_0$ represents the free electron mass. Express the answer in eV.

Or

(b) Explain CMOS Inverter switching characteristics.

14. (a) Describe the effect of base-collector voltage on collector current.

Or

(b) The hole current density in the n-side of a p-n diode is given by the below expression.

$$J_p(x) = -qD_p \frac{n_{ie}^2}{n_n} \frac{d}{dx}\left(\frac{n_n p_n}{n_{ie}^2}\right).$$

Derive the above equation starting the approximations made in the derivation.

15. (a) Explain about the Liouville equation for kinetic transport models.

Or

(b) Explain the different extensions of Boltzmann equation.

PART C — (1 × 15 = 15 marks)

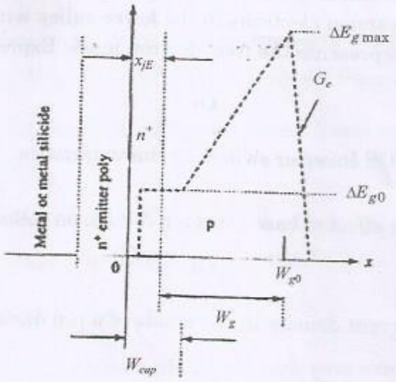
16. (a) (i) The small-signal transconductance in the saturation region is defined as $g_{mass} = dI_{dsat}/dV_{gs}$. Derive an expression for g_{msat}, based on the $n = 1$ velocity saturation model. Show that g_{msat} approaches the saturation velocity limited value (when L tends to 0). What becomes of the expression for g_{msat} in the long channel limit when V_{sat} tends to infinite?

Also calculate the carrier velocity at the source end of the channel. Assume when L tends to 0 and V_{sat} tends to infinite.

(ii) For and nMOSFET with $t_{ox} = 10nm$ and a uniform p-type doping of $10^{17} cm^{-3}$, the gate is n^+ polysilicon doped to 10^{20} cm^3. Estimate the depletation layer width in the polysilicon gate at gate voltage of 3V.

Or

(b)



The above figure represents the emitter and base regions of a polysilicon-emitter SiGe-base bipolar transistor having Ge distribution that make the collector current less sensitive to emitter depth variation. Show that the collector current ratio for SiGe-base bipolar transistor is represented by the below expression.

$$\frac{J_{C0}(SiGe, x_{jE})}{J_{C0}(Si, x_{jE})} = \frac{\overline{\gamma\eta}\exp(\Delta E_{g0}/kT)}{\left(\frac{W_{cap}-x_{jE}}{W_{B0}-x_{jE}}\right)+\left(\frac{W_{B0}-W_{cap}}{W_{B0}-x_{jE}}\right)\left(\frac{kT}{\Delta E_{g\max}-\Delta E_{g0}}\right)\left[1-\exp\left(\frac{\Delta E_{g0}-\Delta E_{g\max}}{kT}\right)\right]}$$
