Reg. No. : | | | | | | | | | | | | |

Question Paper Code : 20465

B.E./B.Tech. DEGREE EXAMINATIONS, APRIL/MAY 2022.

Third/Fourth Semester

Electronics and Communication Engineering

EC 8392 — DIGITAL ELECTRONICS

(Common to : Biomedical Engineering/Computer and Communication Engineering/ Mechatronics Engineering/Medical Electronics/Robotics and Automation)

(Regulations 2017)

Time : Three hours | Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Given a binary value 100010010111. Convert to Hexadecimal and octal values.
2. Reduce the Boolean expression $ABC'D + A'BD + ABCD$ to two literals.
3. Suggest a suitable circuit, to determine the equality of two, two-bit binary variables.
4. What is a multiplexer? List two applications.
5. Draw a 4-bit serial-in, serial-out shift register using suitable flip-flop(s).
6. Sketch the block schematic of three-decade decimal BCD counter.
7. List the different types of hazards faced in combinational circuits.
8. What are critical races in combinational circuits? How can it be prevented?
9. A DRAM chip uses two-dimensional address multiplexing. It has 13 common address pins, with the row address having one bit more than the column address. What is the capacity of the memory?
10. How many 32K * 8 RAM chips are needed to provide a memory capacity of 256K bytes?

PART B — (5 × 13 = 65 marks)

11. (a) Simplify using Karnaugh map and implement the following Boolean function F, using the two-level forms of logic

(a) NAND-AND (4)

(b) AND-NOR (3)

(c) OR NAND (3)

(d) NOR-OR (3)

F(A, B, C, D) = Σ (0, 4,8,9, 10, 11, 12, 14)

Or

(b) Write the Boolean equations and draw the logic diagram of the circuit whose outputs are defined by the truth table shown in Table 1.

Table 1

inputs			out puts	
a	b	c	f_1	f_2
0	0	0	1	1
0	0	1	0	1
0	1	0	1	0
0	1	1	1	1
1	0	0	1	0
1	0	1	0	1
1	1	0	×	×
1	1	1	1	0

12. (a) Implement a four-bit adder with carry look ahead logic. Write the relevant equations for carry generate and carry propagate at each stage. (13)

Or

(b) Implement the following Boolean functions using appropriate multiplexers:

(a) $F(x,y,z) = \Sigma m(1,2,6,7)$ (7)

(b) $F(A,B,C,D,) = \Sigma m(1, 3, 4, 11, 12, 13, 14, 15)$ (6)

13. (a) A sequential circuit with two D flip-flops A and B with two inputs, x and y; and one output z, is specified by the following next-state and output equations:

$$A(t+1) = xy' + xB$$
$$B(t+1) = xA + xB'$$
$$z = A$$

(i) Draw the logic diagram of the circuit

(ii) List the state table for the sequential circuit

(iii) Draw the corresponding state diagram.

Or

(b) Using JK flip-flops, design a counter with the following repeated binary sequence: 0, 1, 2, 3, 4, 5, 6.

(i) Draw the logic diagram of the counter

(ii) List the state table for the counter

(iii) Draw the corresponding state diagram, considering the unused states too.

14. (a) Assume the inverters shown in Figure 1, having a delay of 1 ns and the other gates, have a delay of 2 ns. Initially A = B = C = 0 and D = 1; C changes to 1 at time 2 ns. Draw a timing diagram, showing the glitch, corresponding to the hazard. Modify the circuit, so that it is hazard free. (Leave the circuit as a two-level, OR- AND circuit)

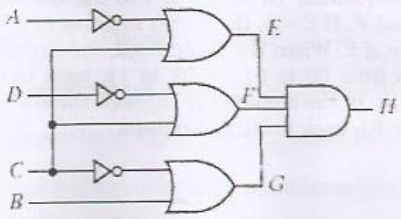

Figure 1

Or

(b) Consider the three-level NOR circuit shown in Figure 2. Find all hazards in this circuit. Redesign the circuit, as a three-level NOR circuit, that is free of all hazards.

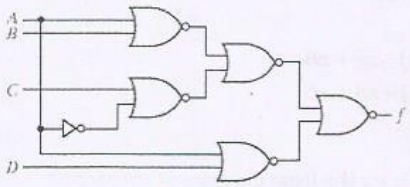

Figure 2

15. (a) Design a Programmable Logic Array (PLA) for the following boolean junctions.

$$F_1 = AB' + AC + A'BC'$$

$$F_2 = (AC + BC)'$$

Draw the corresponding PLA programming table.

Or

(b) Design a combinational circuit using a ROM. The circuit accepts a three-bit number and outputs a binary number equal to the square of the input number. Draw the truth table of the combinatorial circuit, block diagram of ROM, and truth table of ROM.

PART C — (1 × 15 = 15 marks)

16. (a) Using required number of 64 * 8 ROM chips with an enable input, design a 512 * 8 ROM. (15)

Or

(b) Design a sequential circuit with two JK flip-flops, A and B and two inputs E and F. If E = 0, the circuit remains in the same state regardless of the value of F. When E = 1 and F = 1, the circuit goes through the state transitions from 00 to 01, to 10, to 11, back to 00, and repeats. When E = 1 and F= 0, the circuit goes through the state transitions from 00 to 11, to 10, to 01, back to 00, and repeats. (15)

———————