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Question Paper Code : 40490

B.E./B.Tech. DEGREE EXAMINATIONS, NOVEMBER/DECEMBER 2021.

Fourth Semester

Electrical and Electronics Engineering

EE 8451 — LINEAR INTEGRATED CIRCUITS AND APPLICATIONS

(Common to : B.E. Electronics and Instrumentation Engineering and Instrumentation and Control Engineering)

(Regulations 2017)

Time : Three hours | Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. What is meant by dielectric isolation?

2. How does FET fabrication differ from BJT?

3. Find the maximum frequency for a sine wave output voltage of 5 V peak with an OP-AMP whose slew rate is 2V/μs.

4. Design an adder circuit using Op-amp to get the output expression as $V_0 = -(0.1\,V_1 + V_2 + 10\,V_3)$ where V_1, V_2, V_3 are inputs

5. A basic step of a 9-bit DAC is 10.3 mV. If 000000000 represents 0V, what output is produced if the input is 101101011?

6. What is the use of Sample and Hold circuit in A/D Converter?

7. Find the change in output frequency for input change of 1.2V to 1.5V with voltage to frequency conversion factor is 30×10^3 Hz/V.

8. Why pin4 is connected to V_{cc} in a 555 timer?

9. The unregulated input voltage of the three terminal regulator is 8V. Find the output voltage.

10. Compare the linear and switching regulator.

PART B — (5 × 13 = 65 marks)

11. (a) Describe the Epitaxial Growth, Oxidation, Photolithography and Diffusion processes in Silicon Planar technology with relevant diagrams. (13)

Or

(b) Explain in detail the different fabricating methods involved in Integrated Resistors and diodes with neat diagrams. (13)

12. (a) Discuss any two DC and AC characteristics of OPAMP with their importance. (13)

Or

(b) (i) Explain the operation of practical differentiator with neat diagrams. (8)

(ii) Design an op-amp differentiator that will differentiate an input signal with f_{max} = 500 Hz. Assume, C = 0.01 µF. (5)

13. (a) (i) Derive the output expression of an Instrumentation amplifier with neat diagram. (8)

(ii) Design a second order Butterworth Low pass filter for a higher cut-off frequency of 5 kHz. Assume, C = 0.1µF and feedback resistor is 10 kΩ. (5)

Or

(b) (i) Derive and design a RC-Phase shift oscillator with the frequency of oscillations equal to 2 KHz. Assume, C = 0.01 µF and R_f = 5 kΩ. (8)

(ii) Obtain the output of R-2R ladder DAC with binary data $d_1d_2d_3$ is 101. Assume, V_R = –5V and d_1 is the MSB bit. (5)

14. (a) (i) Draw the block Diagram of IC 566 Voltage Controlled Oscillator and explain its operation and derive its free running frequency. (10)

(ii) Explain the application of PLL as AM detection. (3)

Or

(b) Explain the internal circuit of 555 timer and explain the design of monostable multivibrator using 555 timer. (13)

15. (a) (i) Describe the operations of AD623 Instrumentation amplifier and mention its applications. (7)

(ii) With neat diagram, explain the operation of High voltage regulator using IC 723. (6)

Or

(b) Explain the operation of Switched mode power supply with relevant diagrams. (13)

PART C — (1 × 15 = 15 marks)

16. (a) (i) Design an Astable Multivibrator using Op-Amp with the frequency of 3 KHz. Assume C = 0.1 μF, R_1 = 2 KΩ, β = 0.3. (8)

(ii) Design and explain the triangular waveform generator using Op-Amp. (7)

Or

(b) (i) Calculate the free running frequency, Lock-range and capture range of a 565 PLL if R_T = 6.2 kΩ, C_T = 0.001 μF and filter capacitor is 1 μF. The supply voltage is ±6V. (8)

(ii) Explain the construction of 4 bit D/A converter using Op-Amp. (7)