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Question Paper Code : 40450

B.E./B.Tech. DEGREE EXAMINATIONS, NOVEMBER/DECEMBER 2021.

Fifth Semester

Electronics and Communication Engineering

EC 8552 – COMPUTER ARCHITECTURE AND ORGANIZATION

(Common to B.E. Electronics and Telecommunication Engineering)

(Regulations 2017)

Time : Three hours

Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. List the difference between wall clock time and response time.
2. Find the cycle time of a 450MHz clock frequency.
3. What is underflow in floating point arithmetic?
4. Write the expression for double precision number available in IEEE 754 format.
5. In a data path diagram, what is the size of ALUop control signal?
6. How PCSrc signal generated in a data path diagram?
7. In memory organization, what is temporal locality?
8. Considering memory hierarchy, define hit and miss.
9. Define fine-grain multithreading.
10. List the benefits of clustering in a computer architecture.

PART B — (5 × 13 = 65 marks)

11. (a) What is the role of each idea in the design of computer architecture? Explain. each of them with suitable examples. (4+9)

Or

- (b) Explain about the central processing unit performance and its factors.(13)
12. (a) Determine the floating point multiplication of two numbers 2.5×10^8 and 8.0×10^{-3} . In this regard neatly sketch the corresponding flowchart too. (10+3)

Or

- (b) How the division hardware is refined to speed up the division operation? Explain with diagrams. (4+9)
13. (a) What do you mean by hazards and what are the pipelining hazards occurs in a computer architecture? Describe each of them with suitable example. (3+10)

Or

- (b) Build a suitable Data path for branch instruction. Explain all the blocks with suitable example. (6+7)
14. (a) What is cache memory? How to improve cache performance? Explain. (3+10)

Or

- (b) What is virtual memory? Explain in detail about the virtual memory with suitable diagram. (3+10)
15. (a) What is hardware multi-threading? Explain different types of multi-threading occurs in parallel architectures. (3+10)

Or

- (b) What is Graphics Processing Unit (GPU) and How GPUs can be distinguished from CPUs? Neatly sketch the GPU memory structure which is shared by vectorized loops. Explain briefly. (6+7)

PART C — (1 × 15 = 15 marks)

16. (a) Consider two different implementations of the same instruction set architecture. The instructions can be divided into four classes according to their CPI (class A, B, C and D). P1 with a clock rate of 2.5 GHz and CPIs of 1, 2, 3, and 3, and P2 with a clock rate of 3 GHz and CPIs of 2, 2, 2, and 2. Given a program with a dynamic instruction count of 1000 instructions divided into classes as follows: (15)
- 10% class A, 20% class B, 50% class C, and 20% class D.
- (i) Find the clock cycles required in both cases.
 - (ii) Which implementation is faster and how much?

Or

- (b) Discuss on the concept and applications of clusters and warehouse scale computers.
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