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Question Paper Code : 40439

B.E./B.Tech. DEGREE EXAMINATIONS, NOVEMBER/DECEMBER 2021.

Third/Fourth Semester

Electronics and Communication Engineering

EC 8392 — DIGITAL ELECTRONICS

(Common to Biomedical Engineering/Computer and Communication Engineering/Mechatronics Engineering/Medical Electronics/ Robotics and Automation

(Regulations 2017)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — ($10 \times 2 = 20$ marks)

1. What is the largest binary number that can be expressed with 14 bits? What are the equivalent decimal and hexadecimal numbers?

2. Simplify the Boolean expression, $xy + x(wz + wz')$ to minimum number of literals.

3. Assume that the Ex-OR gate has a propagation delay of 10 ns and that the AND or OR gates have a propagation delay of 5 ns. What is the total propagation delay time in the four-bit adder?

4. Draw the logic diagram for 2 to 4 line decoder using NOR gates.

5. Draw the logic diagram for a 3-bit ring counter.

6. Write down the characteristic equation and excitation table for T flip-flop.

7. What is meant by pulse mode sequential circuit?

8. Differentiate dynamic hazard and static hazard.

9. A DRAM chip uses two-dimensional address multiplexing. It has 13 common address pins, with the row address having one bit more than the column address. What is the capacity of the memory?

10. Define the terms ‘fan-in’ and ‘fan-out’.

PART B — (5 × 13 = 65 marks)

11. (a) With the use of maps, find the simplest sum-of-products form of the function $F = fg$ where $f = abc'+c'd + a'cd'+b'cd'$ and

$g = (a + b + c'+d')\ (b'+c'+d)\ (a'+c + d')$. (13)

Or

(b) Determine all the prime implicants of the function $f(a, b, c, d) = \Sigma m(0, 2, 3, 4, 8, 10, 12, 13, 14)$ using Quine-McCluskey method. Verify the same using K-Map Technique. (13)

12. (a) Design an octal-to-binary priority encoder. Provide an output 'V' to indicate that at least one of the inputs is present. The input with the highest subscript number has the highest priority. What will be the value of the four outputs if inputs D_2 and D_6 are 1 at the same time? (13)

Or

(b) Construct the BCD adder-subtractor circuit. Explain its working by providing relevant inputs to the circuit. (13)

13. (a) With neat sketches and function table, briefly explain the working of a positive edge triggered D flip-flop and also mention its significance. (13)

Or

(b) With neat logic diagram and timing diagram, explain the working of PISO and SIPO shift registers. (13)

14. (a) An asynchronous sequential circuit has two internal states and one output. The two excitation functions and one output function describing the circuit are, respectively.

$Y_1 = x_1x_2 + x_1y_2' + x_2'y_1$
$Y_2 = x_2 + x_1y_1'y_2 + x_1'y_1$
$z = x_2 + y_1$

Draw the logic diagram of the circuit. Obtain the transition table, flow table and output map for the circuit. (13)

Or

(b) Obtain the binary state assignment for the reduced flow table shown in Fig. 1. Avoid critical race conditions. Also draw the logic diagram of the circuit using NAND latches and gates. (13)

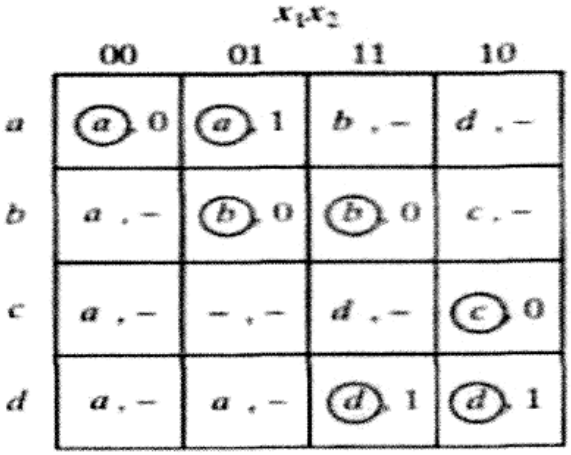

Fig 1

15. (a) Derive the PLA programming table for the four Boolean functions listed below. Minimize the numbers of product terms, (13)

$A(x, y, z) = \Sigma(1, 2, 4, 6)$

$B(x, y, z) = \Sigma(0, 1, 6, 7)$

$C(x, y, z) = \Sigma(2, 6)$

$D(x, y, z) = \Sigma(1, 2, 3, 5, 7)$.

Or

(b) With neat sketches, explain the working of tristate TTL gate. (13)

PART C — (1 × 15 = 15 marks)

16. (a) Design an asynchronous circuit using positive edge triggered JK flip-flops with minimal combinational gating to generate the following sequence 0-1-2-0; if input $X = 0$ and 0-2-1-0; if input $X = 1$, provide an output which goes high to indicate the non-zero state in the 0-1-2-0 sequence. Is this a mealy machine? (15)

Or

(b) Design the sequential circuit for the state diagram shown in Fig.2. (15)

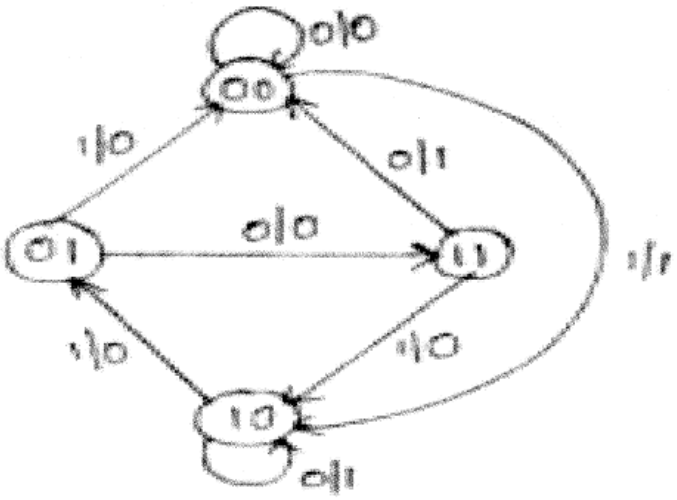

Fig 2