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Question Paper Code : 40431

B.E./B.Tech. DEGREE EXAMINATIONS, NOVEMBER/DECEMBER 2021.

Sixth/Seventh Semester

Electronics and Communication Engineering

EC 8095 – VLSI DESIGN

(Common to : B.E. Electrical and Electronics Engineering/B.E. Electronics and Instrumentation Engineering/B.E. Electronics and Telecommunication Engineering/ B.E. Instrumentation and Control Engineering/B.E. Robotics and Automation)

(Regulations 2017)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. How does a transmission gate produce fully restored logic output?

2. Define low noise margin and high noise margin of a CMOS inverter.

3. State the operations performed during pre charge and evaluate phase of dynamic circuits.

4. List the sources of power dissipation in CMOS circuits.

5. What is meant by bistability?

6. Define clock skew in digital circuits.

7. Draw the circuit diagram of 1-bit binary shifter using MOS transistor.

8. State the need of a sense amplifier in a memory cell.

9. List the common techniques for ad hoc testing.

10. What are the limitations of IDDQ testing?

PART B — (5 × 13 = 65 marks)

11. (a) Derive the expression for current in cutoff, linear and saturation region in long channel I-V characteristics.

Or

(b) Draw and explain the equivalent RC circuit for an Inverter.

12. (a) Compare the circuit implementation of 2-input multiplexer using static CMOS, domino and dual-rail domino logic.

Or

(b) Describe how dynamic voltage scaling can reduce dynamic power dissipation.

13. (a) Explain the circuit and working of CMOS implementation of schmitt trigger.

Or

(b) Discuss the timing parameters that characterize the timing of sequential circuit.

14. (a) Elaborate on rotate right and rotate left operations using barrel shifters.

Or

(b) Draw the NOR and NAND implementation of 4-word, 4-bit ROM.

15. (a) Describe the built-in self-test procedure.

Or

(b) Explain the factors to be considered to optimize circuits for manufacturability.

PART C — (1 × 15 = 15 marks)

16. (a) Design a 4-bit incrementer / decrementer using the CMOS design for 1-bit incrementer / decrementer. The 1-bit logic cell designed has a control input to control the increment or decrement operation. The truth table for 1-bit incrementer cell is as shown in Table 1.

Table 1. Truth table for 1-bit incrementer cell

Inputs			Output	
Clock	Ci	Qn-1	Ci+1	Qn
0	0	0	0	0
1	0	0	0	0
0	1	0	0	0
1	1	0	0	1
1	1	0	0	1
0	0	1	0	0
1	0	1	0	1
0	1	1	0	0
1	1	1	1	0

Or

(b) Design a circuit described by the Boolean Function $Y = \overline{A.(B+C)(D+E)}$ using CMOS logic. Calculate the equivalent CMOS inverter circuit for simultaneous switching of all inputs assuming that $\left[\frac{w}{L}\right] = 5$ for pMOS transistor and $\left[\frac{w}{L}\right] = 2$ for all nMOS transistor.