3.1 ANALOG MULTIPLIERS

A multiple produces an output V0 which is proportional to the product of two inputs $V_x$and V_y.

$$V_0 = KV_xV_y$$

where K is the scaling factor = (1/10) V^{-1}.

There are various methods available for performing analog multiplication. Four of such techniques, namely,

1. Logarithmic summing technique
   Pulse height/width modulation Technique
2. Variable trans conductance Technique
3. Multiplication using Gilbert cell and
4. Multiplication using variable trans conductance technique.

An actual multiplier has its output voltage V_0 defined by

$$V_0 = \frac{(V_x+\phi_x)(V_y+\phi_y)}{10(1+\varepsilon)} + \phi_0$$

where φx and φy are the offsets associated with signals Vx and Vy, ε is the error signal associated with K and φ0 is the offset voltage of the multiplier output.

TERMINOLOGIES ASSOCIATED VOLTAGE OF THE MULTIPLIER CHARACTERISTICS

- **Accuracy**

This specifies the derivation of the actual output from the ideal output, for any combination of X and Y inputs falling within the permissible operating range of the multiplier.

- **Linearity**

This defines the accuracy of the multiplier. The Linearity Error can be defined as the maximum absolute derivation of the error surface. This linearity error imposes a lower limit on the multiplier accuracy.

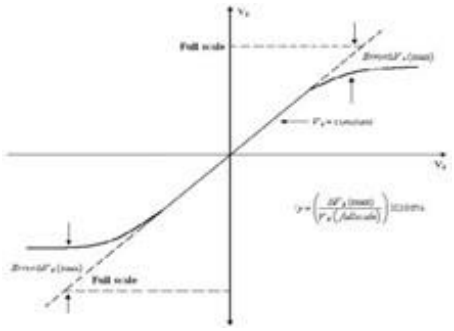


Figure 3.1.1 Linearity of the multiplier

[source:"Linear Integrated Circuits"by S.Salivahanan& V.S. Kanchana Bhaskaran, Page-396]

The figure 3.1.1 shows the response of the output as a function of one input voltage V_x when the other V_y is assumed constant. It represents the maximum percentage derivation from the ideal straight line output. An error surface is formed by plotting the output for different combinations of X and Y inputs.

- **Square law accuracy**

The Square – law curve is obtained with the X and Y inputs connected together and applied with the same input signal. The maximum derivation of the output voltage from an ideal square –law curve expresses the squaring mode accuracy.This is shown in figure 3.1.2

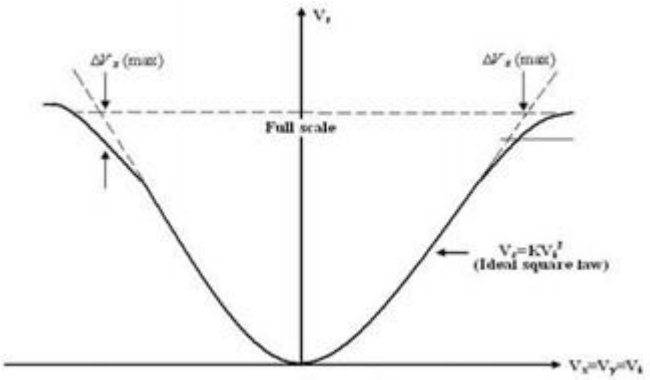


Figure 3.1.2 Squaring mode Accuracy

[source:"Linear Integrated Circuits"by S.Salivahanan& V.S. Kanchana Bhaskaran, Page-396]

- **Bandwidth**

The Bandwidth indicates the operating capability of an analog multiplier at higher frequency values. Small signal 3 dB bandwidth defines the frequency f_0 at which the output reduces by 3dB from its low frequency value for a constant input voltage. This is identified individually for the X and Y input channels normally.

The transconductance bandwidth represents the frequency at which the transconductance of the multiplier drops by 3dB of its low frequency value. This characteristic defines the application frequency ranges when used for phase detection or AM detection.

- **Quadrant**

The quadrant defines the applicability of the circuit for bipolar signals at its inputs. First – quadrant device accepts only positive input signals, the two quadrant device accepts one bipolar signal and one unipolar signal and the four quadrant device accepts two bipolar signals.

LOGARITHMIC SUMMING TECHNIQUE

This technique uses the relationship $\ln V_x + \ln V_y = \ln(V_x V_y)$

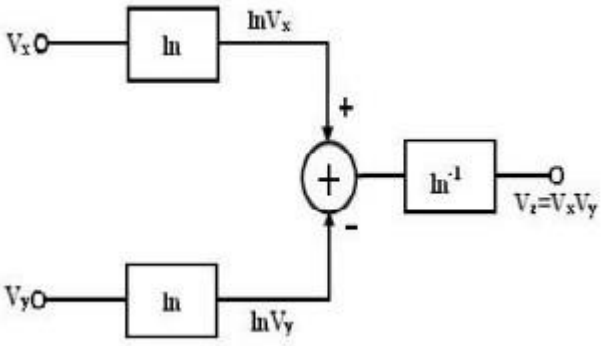


Figure 3.1.3. Multiplication using Logarithmic Summing Technique

[source:"Linear Integrated Circuits"by S.Salivahanan& V.S. Kanchana Bhaskaran, Page-396]

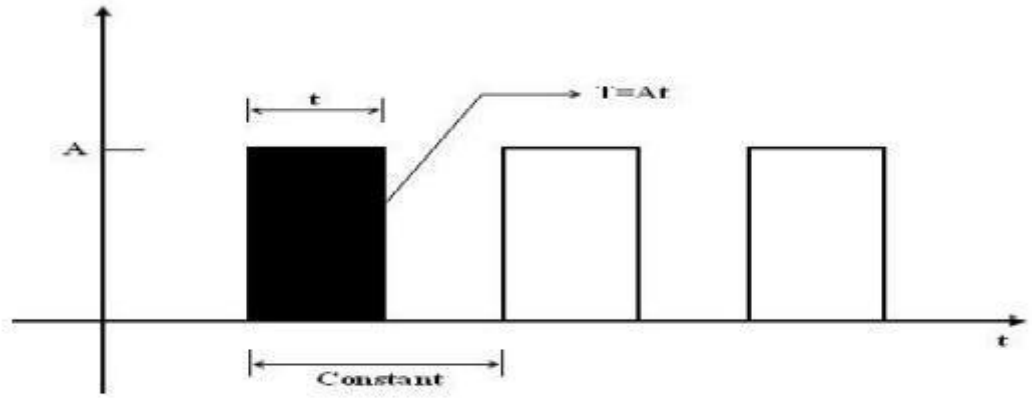
As shown in figure 3.1.3 the input voltages V_x and V_y are converted to their logarithmic equivalent, which are then added together by a summer. An antilogarithmic converter produces the output voltage of the summer. The output is given by,

$$V_z = \ln^{-1}(\ln(V_x V_y)) = V_x V_y .$$

The relationship between I_0 and V_{BE} of the transistor is given by $I_C = I_0 e^{(V_{BE}/V_T)}$. It is found that the transistor follows the relationship very accurately in the range of 10nA to 100mA. Logarithmic multiplier has low accuracy and high temperature instability. This method is applicable only to positive values of V_x and V_y.

Limitation: this type of multiplier is restricted to one quadrant operation only.

PULSE HEIGHT/ WIDTH MODULATION TECHNIQUE



Pulse Height/ Width Modulation Technique

Figure 3.1.4.Pulse Height/Width Modulation Technique

[source:"Linear Integrated Circuits"by S.Salivahanan& V.S. Kanchana Bhaskaran, Page-397]

In this method, the pulse width of a pulse train is made proportional to one input voltage and the pulse amplitude is made proportional to the second input voltage. Therefore, $V_x=K_x$ A, $V_y = K_y$ t, and $V_z = K_z T$ where K_x, K_y, K_z are scaling factors. In figure 3.1.4 A is the amplitude of the pulse, t is the pulse width and T is the area of=the pulse=. Therefore,

$$V_z = K_z T = \frac{V_x V_y}{k_x k_y}$$

The modulated pulse train is passed through an integrated circuit. Therefore, the input of the integrator is proportional to the area of pulse, which in turn is proportional to the product of two input voltages.

ANALOG MULTIPLIER USING AN EMITTER COUPLED TRANSISTOR PAIR

An circuit using an emitter coupled pair is shown in figure 3.1.5.The output currents I_{C1} an d I_{C2} are related to the differential input voltage V_1 by

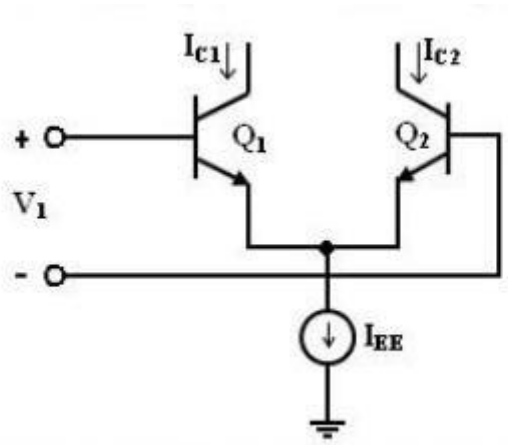


Figure 3.1.5 Multiplier circuit using an emitter coupled pair

[source:"Linear Integrated Circuits"by S.Salivahanan& V.S. Kanchana Bhaskaran, Page-397]

$$I_{C1} = \frac{I_{EE}}{1+e^{-V_1/V_T}}$$

$$I_{C2} = \frac{I_{EE}}{1+e^{V_1/V_T}}$$

where V_T is thermal voltage and the base currents have been neglected. Combining above eqn., difference between=the two output currents as

$$\Delta I_C = I_{C1} - I_{C2}$$

$$= I_{EE}\left(\frac{1}{1+e^{-V_1/V_T}} - \frac{1}{1+e^{V_1/V_T}}\right)$$

$$= I_{EE}\tanh\left(\frac{V_1}{2V_T}\right)$$

The dc transfer characteristics of the emitter – coupled pair is shown in figure 3.1.6. It shows that the emitter coupled pair can be used as a simple multiplier using this configuration. When the differential input voltage $V_1 << V_T$, we can appropriate as given by

$$I_{EE}\tanh\left(\frac{V_1}{2V_T}\right) = I_{EE}\left(\frac{V_1}{2V_T}\right)$$

Then the equation becomes

$$\Delta I_C = I_{EE} \left(\frac{V_1}{2V_T}\right)$$

The current I_{EE} is the bias current for the emitter – coupled pair. If the current I_{EE} is made proportional to a second input signal V_2, then

$$I_{EE} = K_0 (V_2 - V_{BE(on)})$$

Substituting above eqn. , we get

$$\Delta I_C = K_0 V_1 (V_2 - V_{BE(on)})/2V_T$$

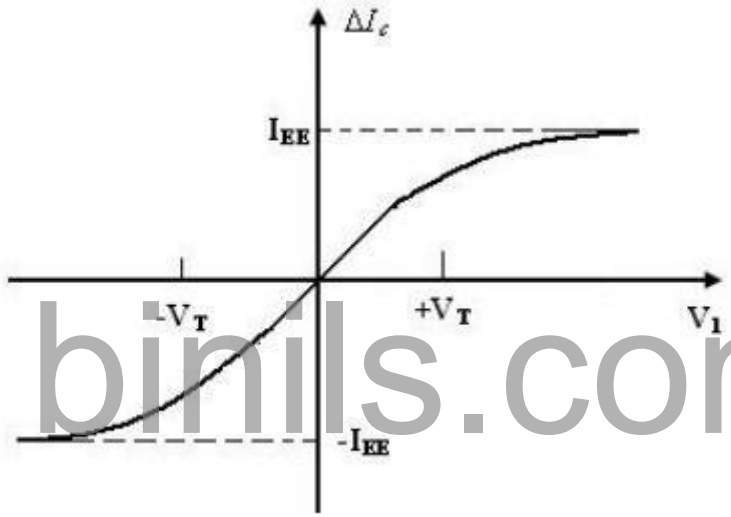


Figure 3.1.6 DC Transfer Characteristics of emitter coupled pair

[source:"Linear Integrated Circuits"by S.Salivahanan& V.S. Kanchana Bhaskaran, Page-398]

This arrangement is shown in figure 3.1.7. It is a simple modulator circuit constructed using a differential amplifier. It can be used as a multiplier, provided V_1 is small and much less than 50mV and V_2 is greater than V_{BE} (on). But, the multiplier circuit shown in figure has several limitations. The first limitation is that V_2 is offset by V_{BE} (on).

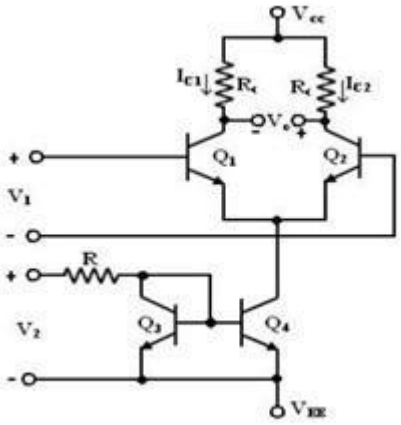


Figure 3.1.7 A Simple modulator using a differential Amplifier

[source:"Linear Integrated Circuits"by S.Salivahanan& V.S. Kanchana Bhaskaran, Page-398]

The second is that V_2 must always be positive which results in only a two-quadrant multiplier operation. The third limitation is that, the tanh (X) is approximately as X, where X = $V_1 /2V_T$. The first two limitations are overcome in the Gilbert cell.

3.3 ANALOG MULTIPLIER ICs

Analog multiplier is a circuit whose output voltage at any instant is proportional to the product of instantaneous value of two individual input voltages. Important applications of these multipliers are multiplication, division, squaring and square – rooting of signals, modulation and demodulation. These analog multipliers are available as integrated circuits consisting of op-amps and other circuit elements. The Schematic of a typical analog multiplier, namely, AD633 is shown in figure 3.3.1.

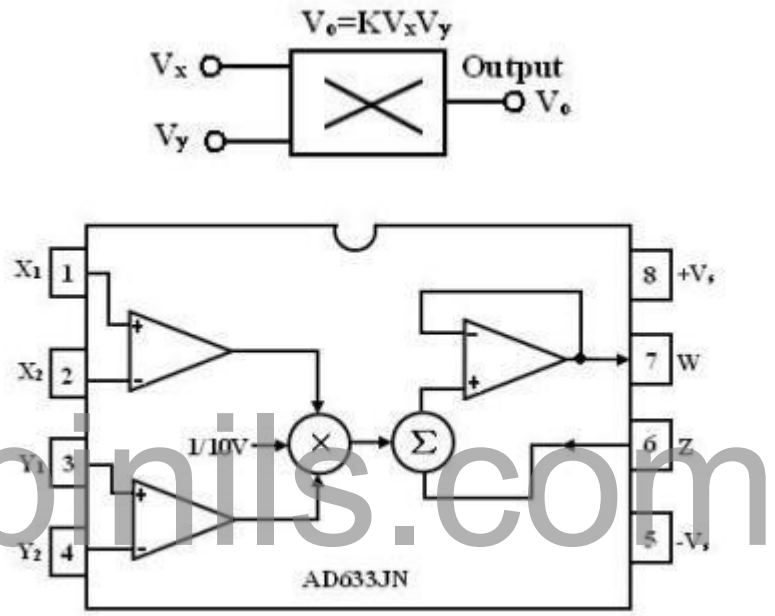


Figure 3.3.1 Schematic of Analog Multiplier IC and its symbol

[source: https://www.brainkart.com/subject/Linear-Integrated-Circuits_220/]

The AD633 multiplier is a four – quadrant analog multiplier.

- It possesses high input impedance; this characteristic makes the loading effect on the signal source negligible.
- It can operate with supply voltages ranging from ±18V.
- IC does not require external components.
- The typical range of the two input signals is ±10V.

SCHEMATIC REPRESENTATION OF A MULTIPLIER

The schematic representation of an analog multiplier is shown in figure 3.3.1. The output V_0 is the product of the two inputs V_x and V_y is divided by a reference voltage V_{ref}. Normally, the reference voltage V_{ref} is internally set to 10V. Therefore, V0 =V_xV_y/10. In other words, the basic input – output relationship can be defined by KV_x V_y when K = 1/10, a constant. Thus for peak input voltages of 10V, the peak magnitude of output voltage is 1/10 *10 *10 =10V. Thus, it can be noted that, as long as V_x < 10V and V_y < 10V, the multiplier output will not saturate.

MULTIPLIER QUADRANTS

The transfer characteristics of a typical four-quadrant multiplier are shown in figure 3.3.2. Both the inputs can be positive or negative to obtain the corresponding output as shown in the transfer characteristics.

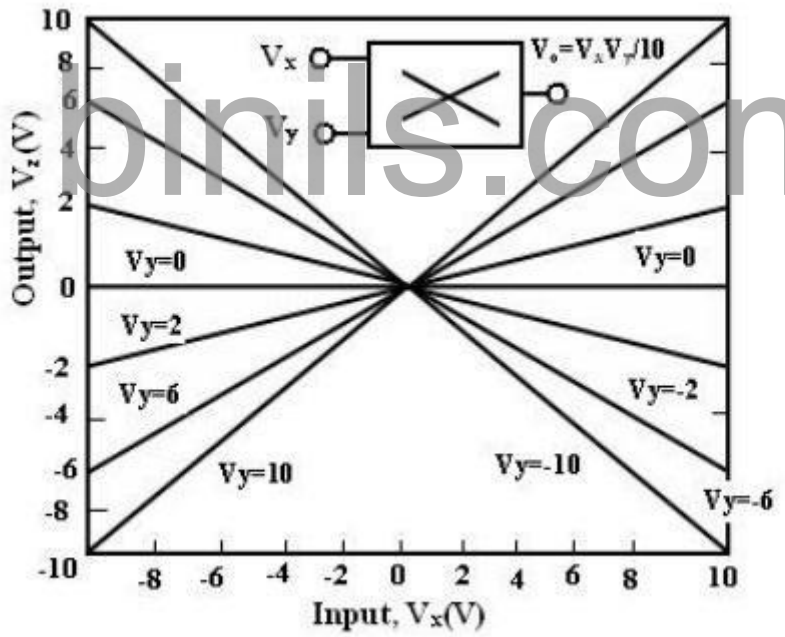


Figure 3.3.2. Transfer Characteristics of a typical four-quadrant multiplier

[source: https://www.brainkart.com/subject/Linear-Integrated-Circuits_220/]

APPLICATIONS OF MULTIPLIER ICs

The multiplier ICs are used for the following purposes:

1. Voltage Squarer
2. Frequency doublers
3. Voltage divider
4. Square rooter
5. Phase angle detector
6. Rectifier

VOLTAGE SQUARER

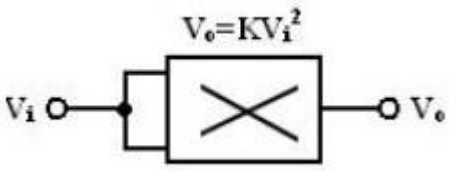


Figure 3.3.3. Voltage squarer Circuit

[source:"Linear Integrated Circuits"by S.Salivahanan& V.S. Kanchana Bhaskaran, Page-408]

Figure 3.3.3 shows the multiplier IC connected as a squaring circuit. The inputs can be positive or negative, represented by any corresponding voltage level between 0 and 10V. The input voltage V_i to be squared is simply connected to both the input terminals, and hence we have, $V_x = V_y = V_i$ and the output is $V_0 = KV_i^2$. The circuit thus performs the squaring operation. This application can be extended for frequency doubling applications.

FREQUENCY DOUBLERS

Figure 3.3.4 a). shows the squaring circuit connected for frequency doubling operation. A sine-wave signal V_i has a peak amplitude of Av and frequency of f Hz. Then, the output voltage of the doublers circuit is given by

$$v_0 = \frac{A_v \sin 2\pi ft * A_v \sin 2\pi ft}{10} = \frac{A_v^2}{10}\sin^2 2\pi ft = \frac{A_v^2}{20}(1 - \cos 4\pi ft)$$

Assuming a peak amplitude Av of 5V and frequency f of 10KHz, V_0 =1.25–1.25cos2 π(20000) t. The first term represents the dc term of 1.25V peak amplitude. The input and output waveforms are shown in figure. The output waveforms ripple with twice the input frequency in the rectified output of the input signal. This forms the principle of application of analog multiplier as rectifier of ac signals. Figure 3.3.4 b)Input-output waveform of frequency doubler.

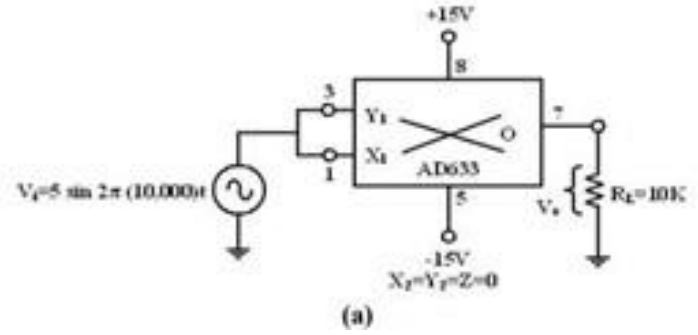


Figure 3.3.4 a) Frequency Doubler circuit diagram

[source:"Linear Integrated Circuits"by S.Salivahanan& V.S. Kanchana Bhaskaran, Page-408]

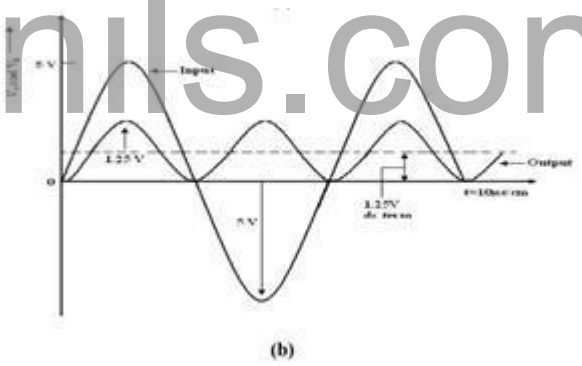


Figure 3.3.4 b)Input-output waveform

[source:"Linear Integrated Circuits"by S.Salivahanan& V.S. Kanchana Bhaskaran, Page-408]

The dc component of output V_0 can be removed by connecting a 1µF coupling capacitor between the output terminal and a load resistor, across which the output can be observed.

VOLTAGE DIVIDER

In voltage divider circuit the division is achieved by connecting the multiplier in the feedback loop of an op-amp.The voltages V_{den} and V_{num} represent the two input voltages, V_{dm} forms one input of the multiplier, and output of op-amp V_{oA} forms the second input.The output

V_{OA} forms the second input. The output VOM of the multiplier is connected back of op- amp in the feedback loop. Then the characteristic operation of the multiplier gives

$$V_{om} = KV_{OA}\, V_{dm} \text{ ------ (1)}$$

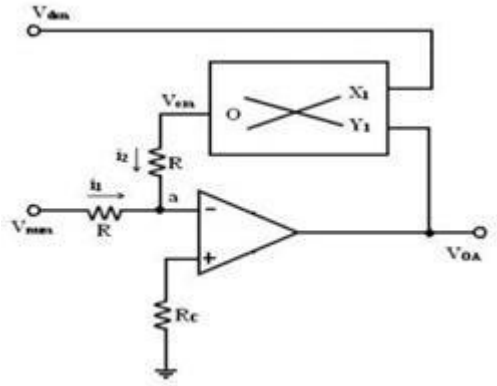


Figure 3.3.5.Voltage Divider Circuit

[source:"Linear Integrated Circuits"by S.Salivahanan& V.S. Kanchana Bhaskaran, Page-409]

As shown in figure 3.3.5 no input signal current can flow into the inverting input terminal of op-amp, which is at virtual ground. Therefore, at the junction a, $i_1 + i_2 = 0$, the current i1 = V_{num} / R, where R is the input resistance and the current $i_2 = V_{om}$ /R. With virtual ground existing at a,

$$i_1 + i_2 = V_{num} / R + V_{om} / R = 0$$

$$KV_{OA}\, V_{den} = - V_{num}$$

or

$$voA = - v_{num}/Kv_{den}$$

where V_{num} and V_{den} are the numerator and denominator voltages respectively. Therefore, the voltage division operation is achieved. V_{num} can be a positive or negative voltage and V_{den} can have only positive values to ensure negative feedback. When V_{dm} is changed, the gain $10/V_{dm}$ changes, and this feature is used in automatic gain control (AGC) circuits.

SQUARE ROOTER

The divider voltage can be used to find the square root of a signal by connecting both inputs of the multiplier to the output of the op-amp. Substituting equal in magnitude but

opposite in polarity (with respect to ground) to Vi. But we know that V_{om} is one- term (Scale factor) of $V_0 * V_0$ or

$$-V_i = V_{om} = V^2/1\ 0$$

Solving for V_0 and eliminating $\sqrt{-1}$ yields. $V0 = \sqrt{10}|Vi|$

Eqn. states that V_0 equals the square root of 10 times the absolute magnitude of V_i.The input voltage Vi must be negative, or else, the op-amp saturates.The range of Vi is between -1 and -10V. Voltages less than -1V will cause inaccuracies in the result.The diode prevents negative saturation for positive polarity Vi signals. For positive values of Vi the diode connections are reversed.

PHASE ANGLE DETECTOR

The multiplier configured for phase angle detection measurement is shown in figure 3.3.6. When two sine-waves of the same frequency are applied to the inputs of the multiplier, the output V0 has a dc component and an AC component.

The trigonometric identity shows that

$$\text{Sin A sin B} = 1/2\ (\cos\ (A-B) - \cos\ (A+B)).$$

When the two frequencies are equal, but with different phase angles, e.g. $A=2\pi ft +\theta$ for signal Vx and $B= 2\pi ft$ for signal V_y, then using the identity

$$[\sin\ (2\ ft+\ )][\sin 2\ ft)]=1/2[\cos\ -\cos(4\ ft\ +\ )]$$

$$=1/2(\text{dc- the double frequency term})$$

Therefore, when the two input signals V_x and V_y are applied to the multiplier, V_0 (dc) is given by

$$v_v(dc) = \frac{v_{xp}v_{yp}}{20}\cos\theta$$

where V_{xp} and V_{yp} are the peak voltage amplitudes of the signals V_x and V_y. Thus, the output V_0(dc) depends on the factor cos θ. A dc voltmeter can be calibrated as a phase angle meter when the product of V_{xp} and V_{yp} is made equal to 20. Then, a (0-1) V range dc voltmeter can

directly read cos θ, with the meter calibrated directly in degrees from a cosine table. The input and output waveforms are shown in figure 3.3.7.

Then the above eqn becomes V_0 (dc) = cos θ, if we make the product V_{xp} V_{yp} = 20 or in other words, V_{xp} – V_{yp} = 4.47V.

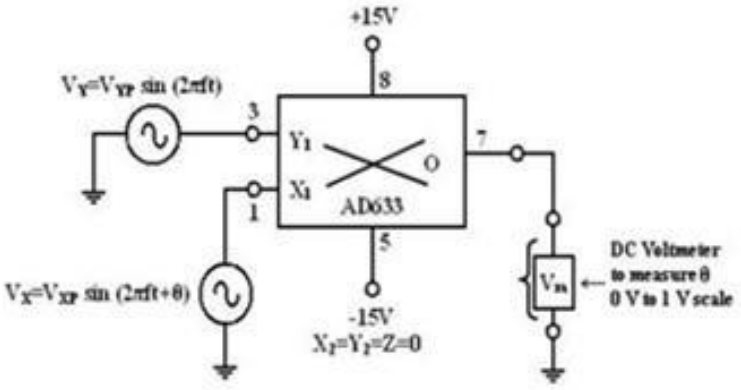


Figure 3.3.6 Phase angle measurement circuit diagram

[source: https://www.brainkart.com/subject/Linear-Integrated-Circuits_220/]

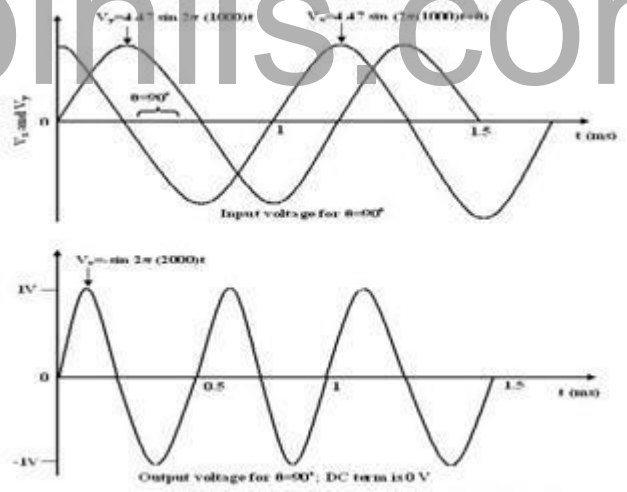


Figure 3.3.7.Input-output waveform

[source: https://www.brainkart.com/subject/Linear-Integrated-Circuits_220/]

3.4 OPERATION OF BASIC PHASE LOCKED LOOP

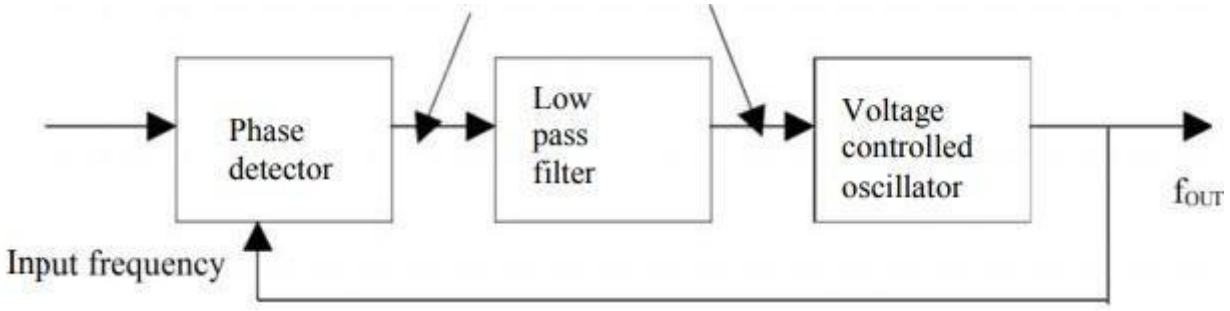


Figure 3.4.1.Block Diagram of PLL

[source: https://www.brainkart.com/subject/Linear-Integrated-Circuits_220/]

Before the input is applied, the PLL is in free running state. Once the input frequency is applied the VCO frequency starts to change and PLL is said to be in the capture mode. The VCO frequency continuous to change until it equals the input frequency and the PLL is in phase lock mode. When Phase locked, the loop tracks any change in the input frequency through its repetitive action.

If an input signal vs of frequency fs is applied to the PLL, the phase detector compares the phase and frequency of the incoming signal to that of the output vo of the VCO. If the two signals differ in frequency of the incoming signal to that of the output vo of the VCO.The phase detector is basically a multiplier and produces the sum ($f_s + f_o$) and difference ($f_s - f_o$) components at its output.The high frequency component ($f_s + f_o$) is removed by the low pass

filter and the difference frequency component is amplified then applied as control voltage v_c to VCO.

The signal v_c shifts the VCO frequency in a direction to reduce the frequency difference between fs and f_o. Once this action starts, we say that the signal is in the capture range. The VCO continues to change frequency till its output frequency is exactly the same as the input signal frequency. The circuit is then said to be locked. Once locked, the output frequency f_o of VCO is identical to fs except for a finite phase difference φ. This phase difference φ generates a corrective control voltage vc to shift the VCO frequency from f0 to fs and thereby maintain the lock. Once locked, PLL tracks the frequency changes of the input signal. Thus, a PLL goes through three stages (i) free running, (ii) capture and (iii) locked or tracking.

Capture range: The range of frequencies over which the PLL can acquire lock with an input signal is called the capture range. This parameter is also expressed as percentage of fo.

Pull-in time: The total time taken by the PLL to establish lock is called pull-in time. This depends on the initial phase and frequency difference between the two signals as well as on the overall loop gain and loop filter characteristics.

Lock-in Range: Once the PLL is locked, It can track frequency changes in the incoming signals.The range of frequencies over which the PLL can maintain lock with the incoming signal is called the lock in range or tracking range.

CLOSED LOOP ANALYSIS OF PLL

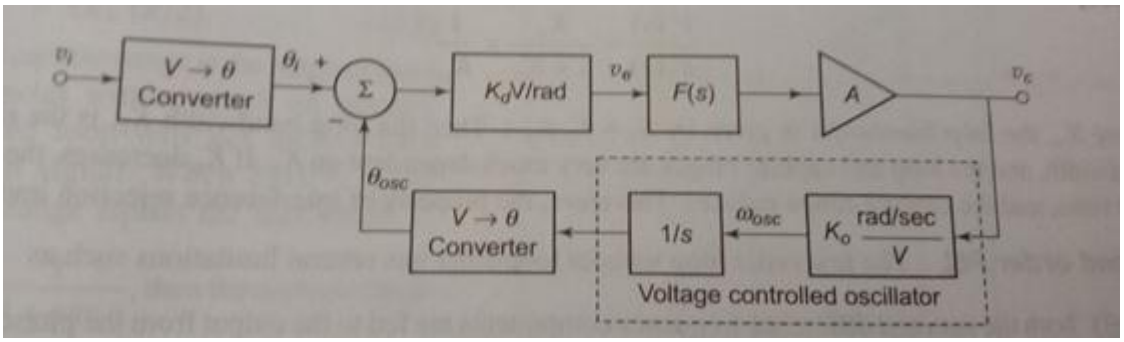


Figure 3.4.2.Detailed block diagram of PLL

[source:"Linear Integrated Circuits"by S.Salivahanan& V.S. Kanchana Bhaskaran, Page-417]

Figure 3.4.2 shown above is the detailed block diagram of PLL. The i/p sinusoidal gain V_i is given as

$$V_i = V_p \sin(\omega t + \theta)$$

If the phase shift of the signal at the VCO o/p is θ_{osc},then the average value of the o/p of phase detector is

$$V_e = K_d(\theta_i - \theta_{osc})$$

$$where\ \theta_i\ \&\theta_{osc} \rightarrow phase\ shift$$

The phase of the signal at the o/p of VCO as a function of time is equal to integral of the VCO o/p frequency & can be expressed as

$$\omega_{osc(t)} = \frac{d\theta_{osc(t)}}{dt}$$

$$d\theta_{osc(t)} = \omega_{osc(t)} dt$$

$$\int d\theta_{osc(t)} = \int \omega_{osc(t)} dt + \theta_{osc\ at\ t=0}$$

$$\theta_{osc(t)} = \int \omega_{osc(t)} dt + \theta_{osc\ at\ t=0}$$

The integral component is represented as 1/S inside the VCO block. Oscillator frequency ω_{osc} & the dc control voltage V_c are related by

$$\omega_{osc} = \omega_c + K_o V_c$$

$$where,\ \omega_c \rightarrow centre\ or\ free\ running\ angular\ frequency,$$

$$that\ results\ when\ V_c = 0\ \&\ K_o\ is\ the\ VCO\ gain\ in\ rad/\sec\ per\ volt.$$

Then the closed loop transfer function of PLL

$$\frac{V_c(s)}{\theta_i(s)} = \frac{K_d F(S) A}{1 + K_d A F(S) \frac{K_o}{S}} = \frac{S K_d F(S) A}{S + K_d A F(S) K_o}$$

Response of the loop to frequency variation at i/p than phase.

$$\frac{V_c(s)}{\omega_i(s)} = \frac{V_c(S)}{S\theta_i(S)} = \frac{K_d F(S) A}{S + K_d A F(S) K_o}$$

$$\omega_i = \frac{d\theta_i}{dt} \;\&\; \omega_i(s) = s\theta_i(s)$$

F(S)=0,with the loop having a first order low pass frequency response.

$$\frac{V_c(s)}{\omega_i(s)} = \frac{K_v}{S + K_v} X \frac{1}{K_o}$$

$$K_v \rightarrow loop\ bandwidth.$$

$$K_v = K_o K_d A$$

SECOND ORDER PLL

The first order loop without loop-filter has several limitations.

1. Both the sum & difference frequency components are fed to the o/p from the phase detector.
2. All out-of band interfering signals from the i/p will appear shifted in frequency at the o/p.

The most common configuration of monolithic PLL in the second order loop with a loop –filter F(s) of a simple single-pole LPF realized with a resistor R & a Capacitor C in Figure 3.4.3.

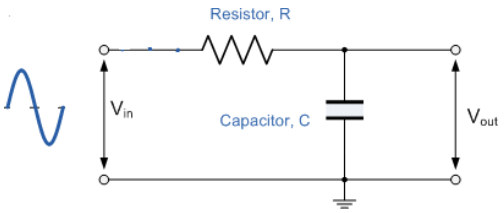


Figure 3.4.3 Single pole loop filter

[source: https://www.electronics-tutorials.ws/filter/filter_2.html]

$$F(s) = \frac{1/SC}{R + 1/SC} = \frac{1}{1 + SRC}$$

$$= \frac{1}{1 + S/\omega} = \frac{1}{1 + S\tau}$$

$$\omega = \frac{1}{RC} = \frac{1}{\tau}$$

The resulting block diagram of the second order PLL using single-pole loop filter is shown in Figure 3.4.4.

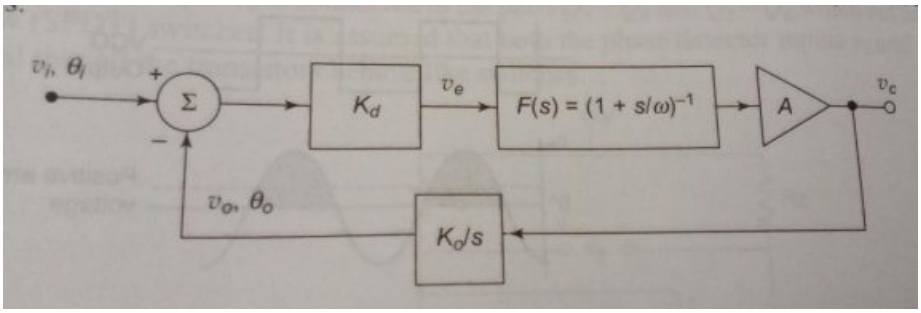


Figure 3.4.4. block diagram of the second order PLL using single-pole loop filter.

[source:"Linear Integrated Circuits"by S.Salivahanan& V.S. Kanchana Bhaskaran, Page-419]

LOOP LOCK-RANGE & CAPTURE RANGE

The loop lock-range is represented as the range of frequency about ω_o for which PLL maintains the relationship

$$\omega_i = \omega_{osc}$$

If the phase detector can determine the phase difference between θ_i & θ_{osc}

Over a $\pm\frac{\pi}{2}$ range ,then the lock-range is defined as

$$\omega_L = \pm\boldsymbol{\Delta\omega_{osc}}$$

$$= \boldsymbol{K_d A K_o}(\pm\frac{\boldsymbol{\pi}}{\boldsymbol{2}}) = \pm\boldsymbol{K_v}(\frac{\boldsymbol{\pi}}{\boldsymbol{2}})$$

The capture range is the range of i/p frequencies with in which a initially unlocked loop will get locked with an i/p signal. When F(s)=1 ,the capture range equals the lock-range. If $\boldsymbol{F(S)} = \frac{\boldsymbol{1}}{\boldsymbol{1+S/\omega_i}}$,then the capture range is smaller than the lock-range.

3.5 VOLTAGE CONTROLLED OSCILLATOR

The timing capacitor c_T is linearly charged or discharged by a constant current source/sink.The amount of current can be controlled by changing the voltage v_c applied at the modulating input (pin 5) or by changing the timing resistor R_T external to the IC chip.The voltage at pin 6 is held at the same voltage as pin 5.Thus, if the modulating voltage at pin 5 is increased, the voltage at pin 6 also increases, resulting in less voltage across R_T and thereby decreasing the charging current. Pin configuration of VCo is shown in figure 3.5.1.

Figure 3.5.2 shown below is the block diagram of VCO.A small capacitor of 0.001µf should be connected between pin 5 & 6 to eliminate possible oscillations.A VCO is commonly used in converting low frequency signals such as EEG,ECG in to an audio frequency range.These audio signals can be transmitted over telephone lines or a two way radio communication system for diagnostic purposes or can be recorded on a magnetic tape for further references.

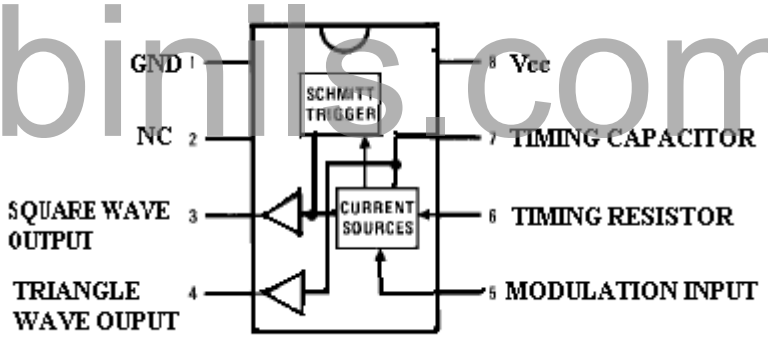


Figure 3.5.1.Pin configuration

[source: https://www.elprocus.com/voltage-controlled-oscillator-working-application/]

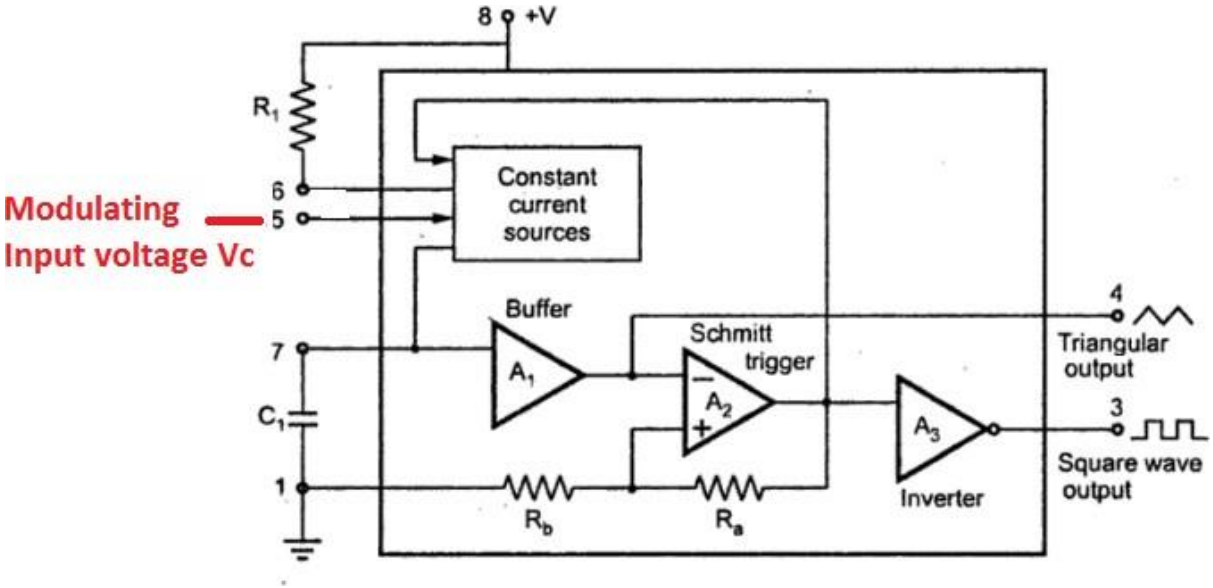


Figure 3.5.2 Voltage controlled oscillator Block diagram

[source: https://sthcphy.files.wordpress.com/2015/09/vco-566.pdf]

The voltage across the capacitor C_T is applied to the inverting i/p terminal of Schmitt trigger A_2 via buffer amplifier A_1 .The o/p voltage swing of the Schmitt trigger is designed to V_{cc} & 0.5 V_{cc} .If R_a=R_b in the +ive feedback loop, the voltage at the non-inverting i/p terminal of A_2 swings from 0.5V_{cc} to 0.25V_{cc}.Figure 3.5.3 a). when the voltage on the capacitor C_T exceeds 0.5V_{cc} during charging, the o/p of the Schmitt trigger goes low(0.5V_{cc})The capacitor now discharges & when it is at 0.25V_{cc}.The o/p of Schmitt trigger goes high(V_{cc}).Since the source & sink currents are equal, capacitor for the same amount of time.This gives a triangular voltage waveform across CT which is also available at pin 4.The square wave o/p of the Schmitt trigger is inverted by inverter A3 & is available at pin 3.The inverter A3 is basically a current amplifier used to drive the load.

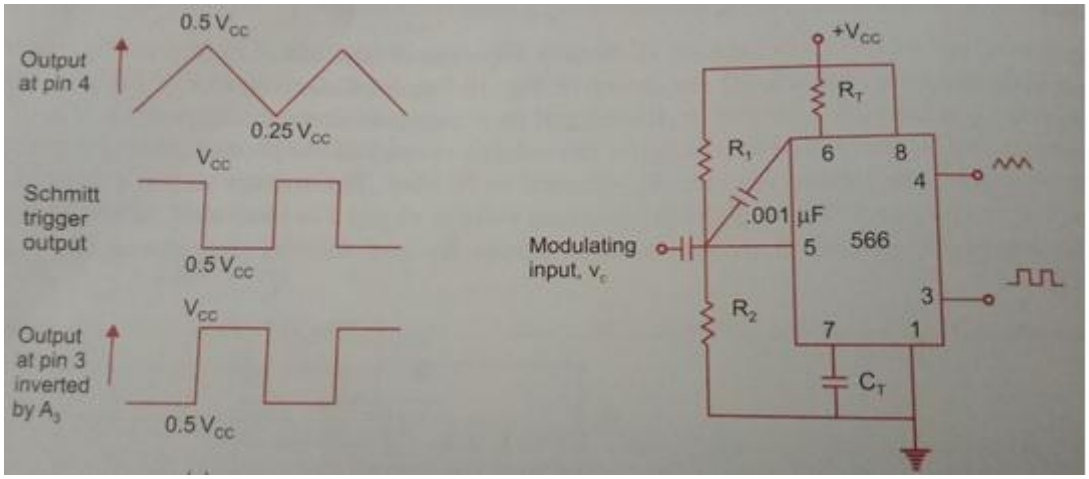


Figure 3.5.3 a)output waveform b)Typical connection diagram

[source:"Linear Integrated Circuits"by D.Roy Choudhry, Shail Bala Jain, Page-386]

The total voltage on the capacitor changes from $0.25V_{cc}$ to $0.5V_{cc}$.Thus $\Delta v=0.25V_{cc}$ The capacitor charges with a constant current source.

$$\frac{\Delta v}{\Delta t}=\frac{i}{C_T}$$

$$\frac{0.25V_{cc}}{\Delta t}=\frac{i}{C_T}$$

$$\Delta t=\frac{0.25V_{cc}C_T}{i}$$

The time period T of the triangular waveform $=2\Delta t$.The freq of oscillator f_o is

$$f_o=\frac{1}{T}=\frac{1}{2\Delta t}=\frac{i}{.5V_{cc}C_T}$$

$$But\ i=\frac{V_{cc}-V_c}{R_T}$$

$$Where\ V_c \rightarrow Voltage\ at\ pin\ 5$$

$$f_o=\frac{2(V_{cc}-V_c)}{C_T R_T V_{cc}} ----(1)$$

The o/p freq of VCO can be changed either by (i)R_T (ii)C_T or (iii) the voltage V_c at the modulating i/p terminal pin 5. The voltage vc can be varied by connecting a R_1R_2 circuit as

shown in the figure 3.5.3 b). The components R1 and c1 are first selected so that VCO output frequency lies in the centre of the operating frequency range. Now the modulating input voltage is usually varied from 0.75 V_{cc} to Vcc which can produce a frequency variation of about 10 to 1.

The signetics NE/SE 560 series is monolithic phase locked loops. The SE/NE 560, 561, 562, 564, 565 & 567 differ mainly in operating frequency range, poser supply requirements & frequency & bandwidth adjustment ranges.

With no modulating i/p signal .if the voltage at pin 5 is biased at $\frac{7}{8}V_{cc}$ (1) gives the VCO o/p frequency

$$f_o = \frac{2(V_{cc} - {}^{7}/_{8}V_{cc})}{C_T R_T V_{CC}} = \frac{1}{4R_T C_T} = \frac{0.25}{R_T C_T} - - - (2)$$

VOLTAGE TO FREQUENCY CONVERSION FACTOR

Voltage to frequency conversion factor K_v & is defined as

$$K_v = \frac{\Delta f_o}{\Delta C}$$

$\Delta V_c \rightarrow modulation\ voltage\ required\ to\ produce\ the\ frequency\ shift\ \Delta f_o\ for\ a\ VCO$

Original frequency is f_o & the new frequency is f_1 then

$$\Delta f_o = f_1 - f_o$$

$$= \frac{2(V_{cc} - V_c + \Delta V_c)}{C_T R_T V_{cc}} - \frac{2(V_{cc} - V_C)}{C_T R_T V_{cc}}$$

$$= \frac{2\Delta V_c}{C_T R_T V_{cc}}$$

$$\Delta V_c = \Delta f_o \frac{C_T R_T V_{cc} \Delta f_o}{2} \text{-----(3)}$$

From (2)

$$f_o = \frac{0.25}{R_T C_T}$$

$$R_T C_T = \frac{0.25}{f_o}$$

$$\Delta V_c = \Delta f_o \frac{V_{cc}}{8 f_o}$$

$$K_v = \frac{\Delta f_o}{\Delta V_c} = \frac{8 f_o}{V_{cc}}$$

3.6 MONOLITHIC PHASE LOCKED LOOPS

The signetics NE/SE 560 series is monolithic phase locked loops. The SE/NE 560, 561, 562, 564, 565 & 567 differ mainly in operating frequency range, poser supply requirements & frequency & bandwidth adjustment ranges. IC 565 is available in a 14 pin DIP package and 10 pin metal can package. Figure 3.6.1 shows the 14 pin DIP package of NE/SE 565.

NE/SE 565 PLL Block Diagram is shown in figure 3.6.2.The o/p frequency of the VCO is given by equation $$f_o = \frac{0.25}{R_T C_T} HZ$$

where R_1&C_1 are an external resistor & a capacitor connected to pins 8 & 9

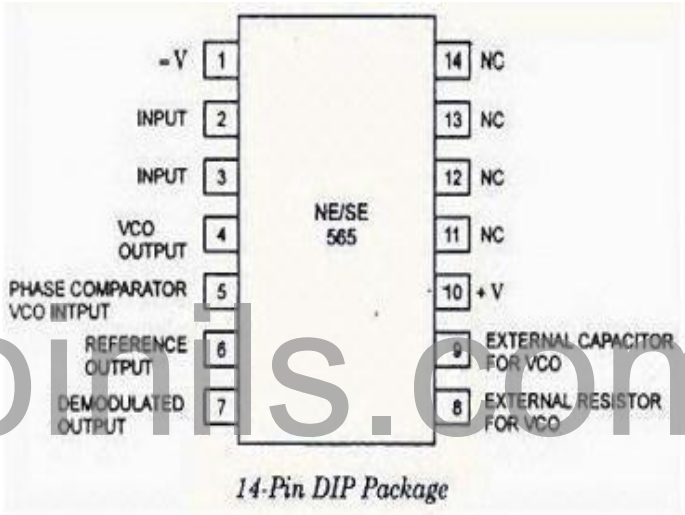


Figure 3.6.1.Pin Configuration of NE/SE565

[source: https://sites.google.com/site/learneasyyourself/home/lic/phase-locked-loop-ic-s]

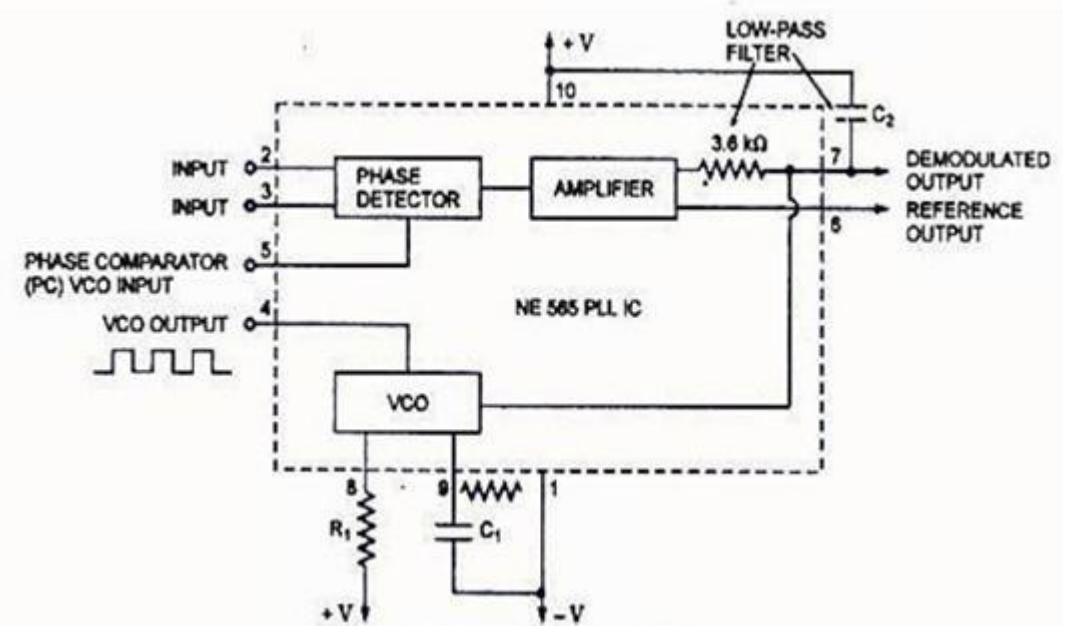


Figure 3.6.2 NE/SE 565 PLL Block Diagram

[source: https://sites.google.com/site/learneasyyourself/home/lic/phase-locked-loop-ic-s]

A value between 2KΩ & 20 KΩ is recommended for R_1.The VCO free running freq is adjusted with R_1 & C_1 be at the centre of the i/p frequency range. A short circuit between pins 4 & 5 connects the VCO o/p to the phase comparator so as to compare f_o with i/p signal f_s.A capacitor C is connected between pin 7 & pin 10 to make a low pass filter with the internal resistance of 3.6 KΩ.The important electrical characteristics of the 565 PLL are, ·

- Operating frequency range: 0.001Hz to 500 Khz. ·
- Operating voltage range: ±6 to ±12v ·
- Input level required for tracking: 10mv rms min to 3 Vpp max ·
- Input impedance: 10 K ohms typically. ·
- Output sink current: 1mA ·
- Output source current: 10 mA

DERIVATION OF LOCK-IN RANGE

If Φ radians- phase difference between the signal & the VCO voltage.The o/p voltage of the analog phase detector is given by

$$V_e = K_{\boldsymbol{\Phi}}(\Phi - \tfrac{\pi}{2})\text{-----(1)}$$

$where\ K_{\boldsymbol{\Phi}}$

$\rightarrow phase\ angle\ to\ voltage\ transfer\ coefficient\ of\ the\ phase\ detector.$

The o/p voltage of VCO is

$$V_c = AK_{\boldsymbol{\Phi}}(\Phi - \tfrac{\pi}{2})\text{-------(2)}$$

$$where\ A \rightarrow voltage\ gain\ of\ the\ amplifier$$

This V_c shifts VCO frequency from its free running frequency f_o to a frequency f given by

$$f = f_o + K_v V_c\text{---(3)}$$

Where K_v—voltage to freq transfer coefficient of the VCO

When PLL is locked in to signal frequency f_s

$$f = f_s = f_o + K_v V_c$$

$$f_s - f_o = K_v V_c$$

$comparing\ (4)\&\ (2)$

$$\frac{(f_s - f_o)}{KV} = AK_{\boldsymbol{\Phi}}(\Phi - \frac{\pi}{2})$$

$$(\Phi - \frac{\pi}{2}) = \frac{(f_s - f_o)}{KVAK_{\boldsymbol{\Phi}}}$$

$$(\Phi) = \tfrac{\pi}{2} + \tfrac{(f_s - f_o)}{KVAK_{\boldsymbol{\Phi}}}\ \text{----(5)}$$

Max o/p voltage magnitude available from the phase detector occurs for Φ=$\boldsymbol{\pi}$ & 0 radians.

$$(1) \rightarrow V_{e(max)} = \pm K_{\boldsymbol{\Phi}} \tfrac{\pi}{2}$$

The corresponding value of the max control voltage available to drive VCO will be

$$(2) \rightarrow V_{c(max)} = \pm AK_{\Phi}\frac{\pi}{2}$$

The max VCO frequency swing that can be obtained is given by

$$(3) \rightarrow (f - f_o)_{max} = K_V V_{C(max)}$$

$$(f - f_o)_{max} = K_V AK_{\Phi}\frac{\pi}{2}$$

The max range of signal frequencies over which PLL can remain locked will be

$$f_s = f_o \pm (f - f_o)_{max}$$

$$f_s = f_o \pm K_V AK_{\Phi}\frac{\pi}{2}$$

$$f_s = f_o \pm \Delta f_L$$

Lock –in Range

$$\Delta f_L = \pm K_V AK_{\Phi}\frac{\pi}{2}$$

$$2\Delta f_L = \pm K_V AK_{\Phi}\pi$$

$$w.k.t,\ K_v = \frac{8f_o}{V}$$

$$V = +V_{cc} - (-V_{cc})$$

$$K_{\Phi} = \frac{1.4}{\pi}$$

A=1.4

$$lock - in\,range\ \Delta f_L = \pm\frac{8f_o}{V}\ X\frac{1.4}{\pi}X1.4X\pi$$

$$\Delta f_L = \pm\frac{7.8f_o}{V}$$

DERIVATION OF CAPTURE RANGE

When PLL is not locked to the signal, the frequency of the VCO will be free running frequency f_o. The phase angle difference between the signal & the VCO o/p voltage

$$\Phi = (w_s t + \theta_s) - (w_o t + \theta_o)$$

$$\Phi = (w_s t) - (w_o t) + (\theta_s - \theta_o)$$

$$\Phi = (w_s - w_o)t + \Delta\theta$$

The phase angle difference does not remain constant but will change with time at a rate given by

$$\frac{d\Phi}{dt} = w_s - w_0$$

The phase detector o/p voltage will not have a dc component but will produces on ac voltage with a triangular waveform of peak amplitude ($K_\Phi \frac{\pi}{2}$) & a fundamental frequency

$$(f_s - f_o) = \Delta f$$

LPF is a simple RC network having transfer function

$$T(jf) = \frac{1}{1 + j\frac{f}{f_1}}$$

$$f_1 = \frac{1}{2\pi RC}$$

$$\left(\frac{f}{f_1}\right)^2 \gg 1 \; then \; T(f) = \frac{1}{j\frac{f}{f_1}}$$

$$T(f) = \frac{f_1}{jf}$$

Fundamental frequency term supplied to LPF by the phase Detector will be the difference frequency

$$\Delta f = f_s - f_o$$

LPF Transfer function will be

$$T(\Delta f) = \frac{f_1}{\Delta f}$$

$$T(\Delta f) = \frac{f_1}{f_s - f_o}$$

Voltage V_c to drive the VCO is

$$V_c = V_e \; X \; T(f) \; X \; A$$

$$V_{c(max)} = V_{e(max)} \; X \; T(f) \; X \; A$$

$$= \pm K_{\Phi} \frac{\pi}{2} A\left(\frac{f_1}{\Delta f}\right)$$

Then the corresponding value of the max VCO frequency shift is

$$(f - f_o)_{max} = K_v V_{c(max)}$$

$$= \pm K_v K_{\Phi} \frac{\pi}{2} A\left(\frac{f_1}{\Delta f}\right)$$

Sub $f = f_s \rightarrow$max signal freq range that can be acquired by PLL is

$$(f_s - f_o)_{max} = \pm K_v K_{\Phi} \frac{\pi}{2} A\left(\frac{f_1}{\Delta f_c}\right)$$

Now, $\Delta f_c = (f_s - f_o)_{max}$

$$\Delta f_c = \pm K_v K_{\Phi} \frac{\pi}{2} A\left(\frac{f_1}{\Delta f_c}\right)$$

$$\Delta f_c^{\,2} = K_v K_{\Phi} \frac{\pi}{2} A f_1$$

$$where, \Delta f_L = \pm K_v K_{\Phi} \frac{\pi}{2} A$$

$$\Delta f_c^2 = f_1 \Delta f_L$$

$$\Delta f_c = \pm\sqrt{f_1 \Delta f_L}$$

The total capture range is

$$2\Delta f_c = 2\sqrt{f_1 \Delta f_L}$$

$$f_1 = \frac{1}{2\pi RC}$$

IC PLL 565, R=3.6KΩ

Capture range is $\pm 2\left[\frac{\Delta f_L}{2\pi(3.6X10^3)C}\right]^{\frac{1}{2}}$,Where C→farads