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Question Paper Code : 40391

B.E./B.Tech. DEGREE EXAMINATIONS, NOVEMBER/DECEMBER 2021.

Fourth/Fifth/Seventh Semester

Computer Science and Engineering

CS 8491 — COMPUTER ARCHITECTURE

(Common to Computer and Communication Engineering/Electrical and Electronics Engineering/Robotics and Automation/Information Technology)

(Regulations 2017)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Mention the different types of fields that are part of an instruction. Give an example.

2. Give an example for Big Endian and Little Endian Representation

3. What is a carry look-ahead adder?

4. List out the 2 ways to detect overflow in an n-bit adder?

5. What is the role of cache memory in pipeline?

6. List the various types of pipeline hazards.

7. Write the formula for calculating the average access time experienced by the processor?

8. Differentiate UMA from NUMA.

9. Abbreviate and define – MTTF and AFT.

10. List the advantage of write through cache.

PART B — (5 × 13 = 65 marks)

11. (a) (i) Explain the different factors affecting the processing speed of CPU. (6)

(ii) Discuss in detail the general Structure of CPU. (7)

Or

(b) With a neat sketch illustrate the instruction cycle state with a program execution. (13)

12. (a) (i) Multiply 9 X -3 using Booth Algorithm, Show the contents of the Accumulator, Registers (Multiplicand and Multiplier) and Count, as a tabular column with stepwise details. (8)

(ii) Explain briefly the possible conditions that may be caused during floating point operation. (5)

Or

(b) Draw the flowchart for floating point Multiplication and explain with an example. (13)

13. (a) (i) List out the performance considerations using pipeline. (5)

(ii) Write down the MIPS Assembly language notation for conditional and unconditional branch operations. (8)

Or

(b) Explain briefly how to handle the conditional branch and branch prediction in pipelining with relevant examples. (13)

14. (a) (i) To achieve the required level of high performance it is necessary to utilize the fastest and most reliable hardware and apply innovative procedures from vector processing techniques. Justify the above statement with the unique feature available for the same. (8)

(ii) Distinguish between SIMD and SISD. (5)

Or

(b) Draw and discuss in detail the basic structure of Symmetric Shared Memory Multiprocessor. (13)

15. (a) With a neat block diagram of DMA, describe how DMA is used to transfer data from peripherals. (13)

Or

(b) Illustrate in detail measuring and improving cache performance. (13)

PART C — (1 × 15 = 15 marks)

16. (a) (i) Assume the given code sequence is from a small, embedded computer application, such as a microwave oven controller that uses 16-bit memory addresses and data operands. If load-store architecture is used, assume that it has 16 general-purpose registers.

For each architecture of your choice answer the following questions:

(1) How many instruction bytes are fetched?

(2) How many bytes of data are transferred from/to memory?

(3) Which architecture is the most efficient as measures in code size?

(4) Which architecture is most efficient as measured by total memory traffic (code + data)? (2 × 4 = 8)

(ii) Assume that a processor has a direct mapped cache

- Data words are 8 bits long (i.e. 1 byte), Data addresses are to the word
- A physical address is 20 bits long
- The tag is 11 bits
- Each block holds 16 bytes of data

How many blocks are in this cache? (7)

Or

(b) (i) With a neat sketch explain why there is translation lookaside buffer on the virtual-to-physical address critical path (10)

Consider the following: -

Virtual addresses are 32 bits

- Pages have 65,536 (or 2^{16}) addressable entries –

Each page table entry has: (1) 1 valid bit (2) 1 dirty bit (3) the physical frame number - Physical addresses are 30 bits long

(ii) How much memory would we need to simultaneously hold the page tables for two different processes? (5)