EE 8351 Digital Logic Circuits

Important 13mark questions

Unit I

1. Show that a positive logic NAND gate is a negative logic NOR gate and vice versa.
2. Assume a 3-input AND gate with output F and a 3-input OR gate with G output. Show the signals of the outputs F and G as functions of the three inputs ABC. Use all 8 possible combinations of inputs ABC.

Unit II

1. Draw the logic diagram of a 2-to-4-line decoder using NOR gates only. Include an enable input.
2. Design a 3×8 decoder using 2×4 decoders. Draw the truth table.

Unit III

1. Explain the operation, state diagram and characteristics of a T flip-flop and master-slave JK flip-flop.
2. Describe the design procedure with neat diagram about 4 bit bidirectional shift register with parallel load.

Unit IV

1. Discuss the operation of SR Latch with NOR and NAND gates analysis.
2. Illustrate about hazards in sequential circuits and the steps to avoid hazards in it.

Unit V

1. Explain the structure and working principles of TTL based Totem-pole output configuration.
2. Write a VHDL code to realize a half adder using behavioural modelling and structural modelling.