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CHENNAI – 600 025

STATE PROJECT COORDINATION UNIT

Diploma in Computer Engineering

Course Code: 1052
M – Scheme

e-TEXTBOOK
on

Basics of Electrical and Electronics Engineering

for

III Semester Dip. In Comp. Engg.

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UNIT I. AC FUNDAMENTALS, BATTERIES AND UPS

- **OBJECTIVES:**
- **Understand the AC fundamentals**
- **Understand the basic terms of AC**
- **Know about Batteries**
- **Battery charging method**
- **Understand the working principle of UPS**

1.1 AC FUNDAMENTALS

1.1.1 DIFFERENCE BETWEEN AC AND DC

AC current

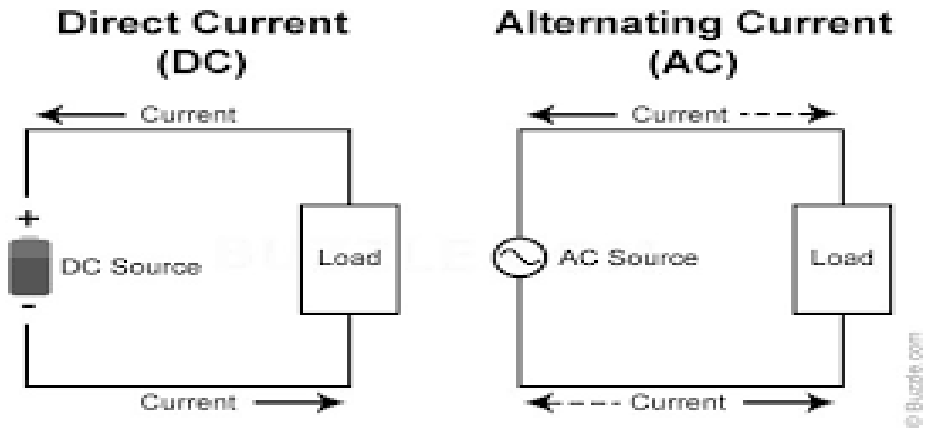
Alternating current is defined as the flow of charge that changes direction periodically. The result obtained will be, the voltage level also reverses along with the current.

A.C, current and voltages are varying in magnitude and polarity.

DC current

By D.C, we mean current and voltages have a fixed polarity and constant Magnitude.

Direct current (DC) is a flow of electrical charge carriers that always takes place in the same direction.



1.1.2

ADVANTAGES OF AC OVER DC

We all know that we got ac supply in our homes and we got this supply by transmitting ac over long distances.

Electric energy is generated and used is AC because it offers much advantages then DC. The few are listed below:-

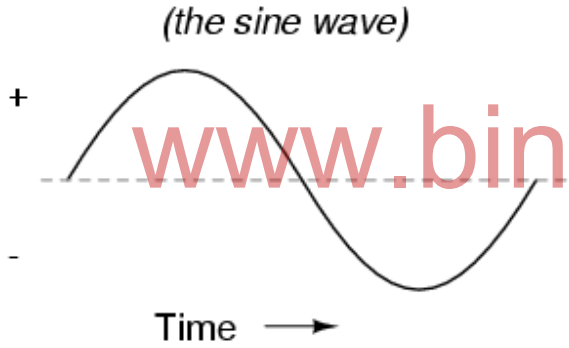
ADVANTAGES

1. AC can be transmitted using step up transformers but direct current or dc Cannot be transmitted by this method.

2. The ac is easy to generate than dc.
3. It is cheaper to generate ac than dc.
4. The ac generators have higher efficiency than dc.
5. The loss of energy during transmission is negligible for ac.
6. The ac can be easily converted into dc.
7. The variation of ac can easily be done using transformers either step up or step down.
8. AC can be generated at high voltages, but DC cannot be generated at high Voltages because sparking starts at the commentator at high voltage, due to which commutator gets damaged.
9. The magnitude of current can be reduced by using an inductance or a conductor Without any appreciable loss of energy
10. A.C. machines are simple, robust and do not require much attention for their Repairs and maintenance during their use.

1.1.3 WAVEFORM OF SINUSOIDAL A.C.CYCLE.

When an alternator produces AC voltage, the voltage switches polarity over time, but does so in a very particular manner. When graphed over time, the “wave” traced by this voltage of alternating polarity from an alternator takes on a distinct shape, known as a Sine wave: Figure below Graph of AC voltage over time (the sine wave).



1.1.4 GENERATION OF SINGLE PHASE A.C BY ELEMENTARY ALTERNATOR

Single-phase generator (also known as single-phase alternator) is an alternating current electrical generator that produces a single, continuously alternating voltage. Single-phase generators can be used to generate power in single-phase electric power systems.

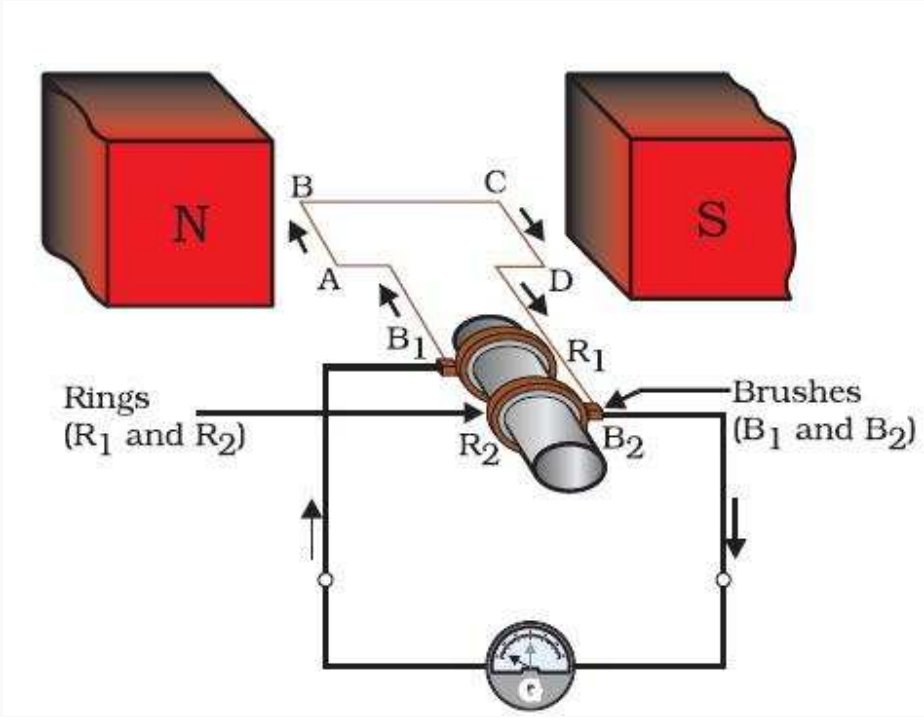


Fig 1.Elementary generator is an example of single-phase generators with two poles

A synchronous generator is an electrical machine producing alternating emf (Electromotive force or voltage) of constant frequency. The basic principles involved in the production of emf and the constructional details of the generators are:

* Faraday discovered that an emf can be induced (or generated) due to relative motion between a magnetic field and a conductor of electricity.

*This voltage was termed as the induced emf since the emf is produced only due to motion between the conductor and the magnetic field without actual physical contact between them.

*The magnetic field is produced by the two fixed poles one being the North Pole from which the magnetic flux lines emerge and enter into the other pole known as the South Pole.

*It was found that the magnitude of the voltage induced in the conductor is proportional to the rate of change of flux lines linking the conductor.

Mathematically it is given as

$e = d\varphi/dt \approx \varphi/t$ volts ---------- (1)

*The above Eqn. 1 holds good only when the magnetic circuit is physically the same at the end as at the beginning and also during the period of change of flux linkages as well.

*In practical rotating machinery, however the change of flux linking each individual conductor during rotation (of either the conductors or the poles) is not clearly defined or cannot be easily measured.

*It is therefore more convenient to express this rate of change of flux in terms of an average flux density (assumed constant) and the relative velocity between this field and a single conductor moving through it.

*For the conductor of active length l moving with a velocity of v in a magnetic field of flux density B, as shown in Fig. 1, the instantaneous induced emf is expressed as,

e = Blv Volts(2)

Where

B= flux density in Tesla (Wb/m2), l = active conductor length (m)

v = relative linear velocity between the conductor and the field (m/s).

* Thus the instantaneous voltage e and the average value E of the induced emf are

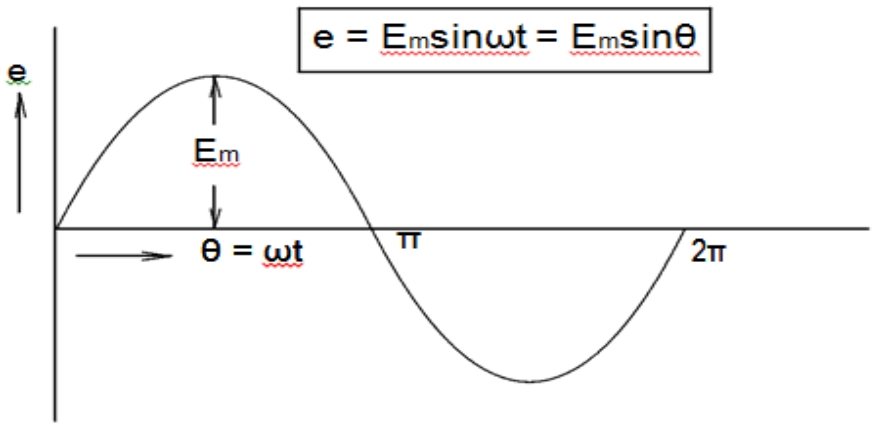
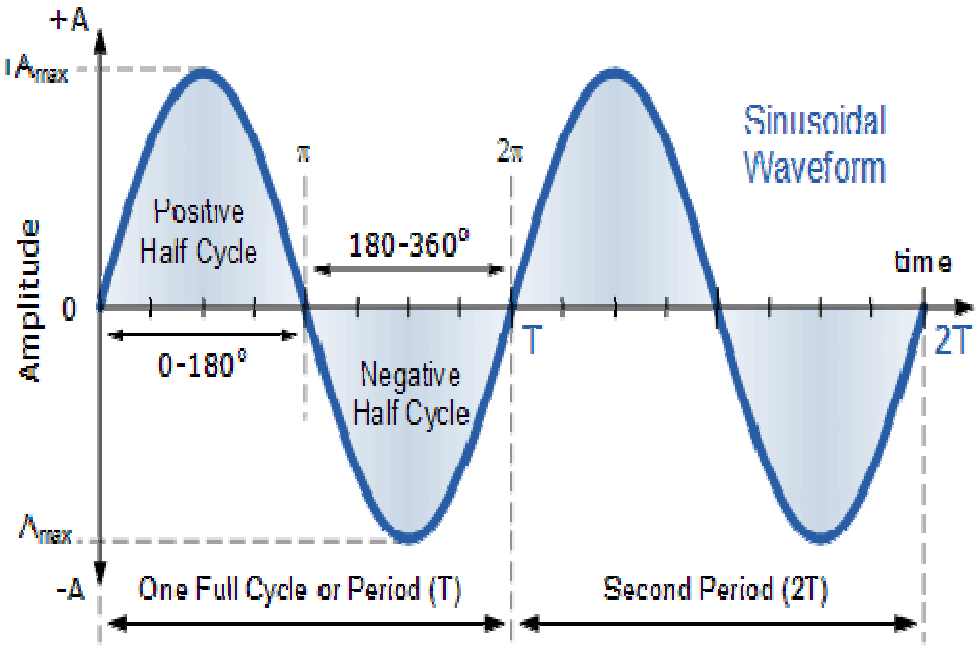


Figure 2: Sinusoidal voltage waveform

1.1.5 Definition

- **A Sine Wave Waveform**



CYCLE:

A set of positive and negative half cycle called one cycle.

Positive half cycle- 0-180°

Negative half cycle- 180-360°

One cycle=0-360°

PERIOD:

This is the length of time in seconds that the waveform takes to repeat itself from start to finish. This value can also be called the *Periodic Time*, (T) of the waveform for sine waves, or the *Pulse Width* for square waves.

- Units of periodic time, (T) include: Seconds (s), milliseconds (ms) and microseconds (μs).
- For sine wave waveforms only, we can also express the periodic time of the waveform in either degrees or radians, as one full cycle is equal to 360^o ($T = 360^o$) or in Radians as 2pi, 2π ($T = 2\pi$), then we can say that 2π radians = 360^o – (Remember this!).

FREQUENCY:

This is the number of times the waveform repeats itself within a one second time period.

*Frequency is the reciprocal of the time period, ($f = 1/T$) with the standard unit of frequency being the *Hertz*, (Hz).

- We now know that the time it takes for electrical waveforms to repeat themselves is known as the periodic time or period which represents a fixed amount of time. If we take the reciprocal of the period, (1/T) we end up with a value that denotes the number of times a period or cycle repeats itself in one second or cycles per second, and this is commonly known as **Frequency** with units of **Hertz, (Hz)**. Then Hertz can also be defined as **"cycles per second"** (cps) and 1Hz is exactly equal to 1 cycle per second.

- Both period and frequency are mathematical reciprocals of each other and as the periodic time of the waveform decreases, its frequency increases and vice versa with the relationship between *Periodic time* and *Frequency* given as.

- **Relationship between Frequency and Periodic Time**

$$\text{Frequency} = \frac{1}{\text{Periodic time}} \quad \text{or} \quad f = \frac{1}{T} \text{ Hz}$$

$$\text{Periodic time} = \frac{1}{\text{Frequency}} \quad \text{or} \quad T = \frac{1}{f} \text{ sec}$$

- Where: f is in Hertz and T is in Seconds.

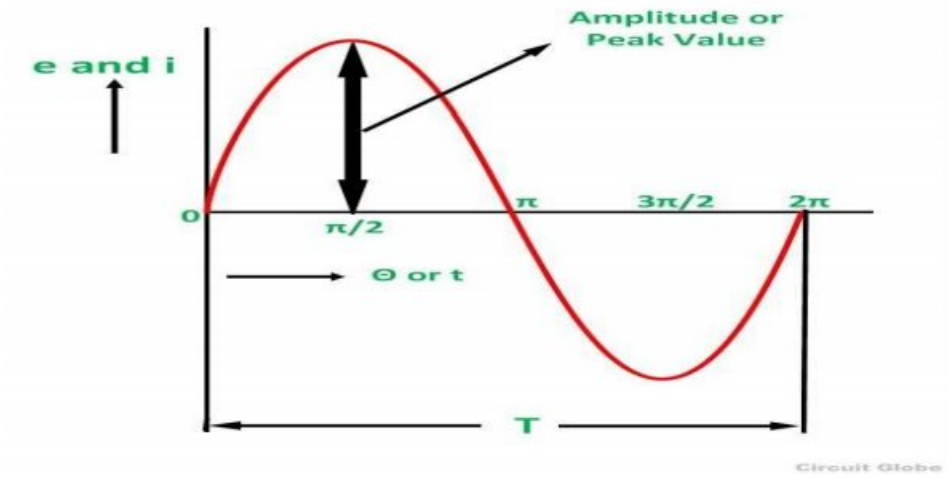
One **Hertz** is exactly equal to one cycle per second, but one hertz is a very small unit so prefixes are used that denote the order of magnitude of the waveform such as **kHz**, **MHz** and even **GHz**

AMPLITUDE:

This is the magnitude or intensity of the signal waveform measured in volts or amps.

PEAK VALUE

Definition: The maximum value attained by an alternating quantity during one cycle is called its P**eak value**.
It is also known as the maximum value or amplitude or crest value.
The sinusoidal alternating quantity obtains its peak value at 90 degrees as shown in the figure below. The peak values of alternating voltage and current is represented by E_m and I_m respectively.



AVERAGE VALUE

Definition: The average of all the instantaneous values of an alternating voltage and currents over one complete cycle is called **Average Value.**

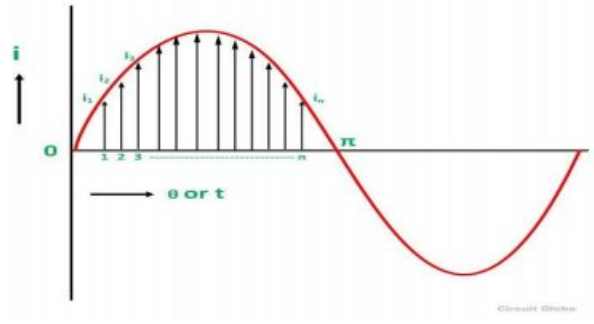
If we consider symmetrical waves like sinusoidal current or voltage waveform, the positive half

Cycle will be exactly equal to negative half cycle. Therefore, the average value over a **complete**

cycle will be zero.

The work is done by both, positive and negative cycle and hence the average value is determined without considering the signs.

So the only positive half cycle is considered to determine the average value of alternating quantities of sinusoidal waves. Let us take an example to understand it.



Divide the positive half cycle into (*n*) number of equal parts as shown in the above figure

Let i_1, i_2, i_3…….. i_n be the mid ordinates

The Average value of current I_{av} = mean of the mid ordinates

$$I_{av} = \frac{i_1 + i_2 + i_3 + \ldots\ldots\ldots + i_n}{n} = \frac{\text{Area of alternation}}{\text{Base}}$$

For Ac

Vavg=0.637*Vm

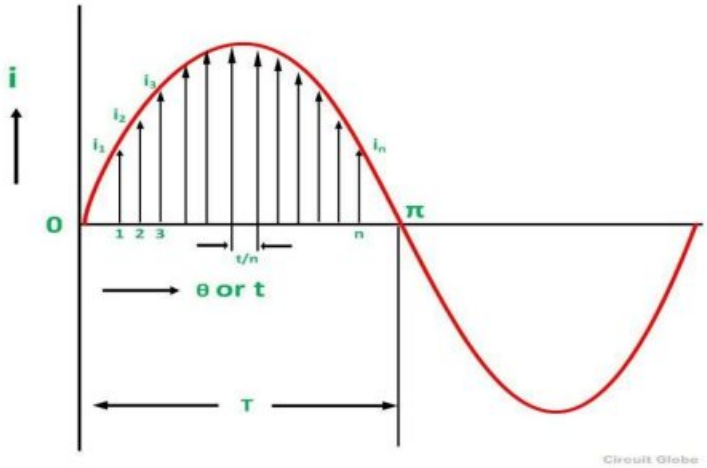
Iavg=0.637*Im

R.M.S Value (Root Mean Square)

Definition: That steady current which, when flows through a resistor of known resistance for a given period of time than as a result the same quantity of heat is produced by the alternating current when flows through the same resistor for the same period of time is

called **R.M.S** or effective value of the alternating current. In other words, the R.M.S value is defined as the square root of means of squares of instantaneous values.

Let I be the alternating current flowing through a resistor R for time t seconds, which produces the same amount of heat as produced by the direct current (I_{eff}). The base of one alteration is divided into n equal parts so that each interval is of t/n seconds as shown in the figure below



Let i_1, i_2, i_3,……in be the mid ordinates

$$\frac{I_{eff}^2 Rt}{J} = \frac{Rt}{J}\left(\frac{i_1^2 + i_2^2 + i_3^2 + \ldots\ldots + i_n^2}{n}\right) \quad \text{or}$$

$$I_{eff} = \sqrt{\frac{i_1^2 + i_2^2 + i_3^2 + \ldots\ldots + i_n^2}{n}}$$

$$I_{eff} = \sqrt{\text{mean of squares of instantaneous values}}$$

I_{eff} = square root of mean of squares of instantaneous values = R.M.S value

Root Mean Square is the actual value of an alternating quantity which tells us an energy transfer capability of an AC source. The ammeter records the RMS value of alternating current and voltmeter record's the root mean square (R.M.S) value of alternating voltage. The domestic single phase AC supply is 230 V, 50 hertz, where 230 V is the R.M.S value of alternating voltage.

For ac

Vrms (or) Veff (or) V=0.707*Vm

Irms (or) Ieff (or) I=0.707*Im

1.1.6 Define Peak factor and Form factor

There is a relation between the peak value, the average value, and the root means square (R.M.S) value of an alternating quantity. Therefore, to express the relationship between all these three quantities, the two factors are used, namely as Peak Factor and Form Factor

PEAK FACTOR

Definition:

Peak Factor is defined as the ratio of maximum value to the R.M.S value of an alternating quantity.

The alternating quantities can be voltage or current. The maximum value is the peak value or the crest value or the amplitude of the voltage or current and the root mean square value is the amount of heat produced by the alternating current will be same when the direct supply of current is passed through the same resistance in the same given time.

Mathematically it is expressed as

$$\text{Peak Factor} = \frac{I_m}{I_{r.m.s}} \text{ or } \frac{E_m}{E_{r.m.s}}$$

Where,
I_m and E_m are the maximum value of the current and the voltage respectively, and $I_{r.m.s}$ and $E_{r.m.s}$ are the root mean square value of the alternating current and the voltage respectively.

The value of Peak Factor is 1.4142

FORM FACTOR

Definition: The ratio of the root mean square value to the average value of an alternating quantity (current or voltage) is called **Form Factor.** The average of all the instantaneous values of current and voltage over one complete cycle is known as the average value of the alternating quantities. Mathematically, it is expressed as

$$\text{Form Factor} = \frac{I_{r.m.s}}{I_{av}} \text{ or } \frac{E_{r.m.s}}{E_{av}}$$

$I_{r.m.s}$ and $E_{r.m.s}$ are the roots mean square value of the current and the voltage respectively, and I_{av} and E_{av} are the average value of the alternating current and the voltage respectively.

The value of Form Factor is 1.11

1.1.7. CONCEPT OF PHASE

Phase denotes the particular point in the cycle of a waveform, measured as an angle in degrees

PHASE DIFFERENCE AND PHASE ANGLE

We saw that the Sinusoidal Waveform (Sine Wave) is an alternating quantity that can be presented graphically in the time domain along an horizontal zero axis.

We also saw that as an alternating quantity, sine waves have a positive maximum value at time π/2, a negative maximum value at time 3π/2, with zero values occurring along the baseline at 0, π and 2π.

However, not all sinusoidal waveforms will pass exactly through the zero axis point at the same time, but may be "shifted" to the right or to the left of 0^o by some value when compared to another sine wave.

Phase Difference Equation

$$A_{(t)} = A_{max} \times \sin(\omega t \pm \Phi)$$

- Where:
- A_m - is the amplitude of the waveform.
- ωt - is the angular frequency of the waveform in radian/sec.
- Φ (phi) - is the **phase angle** in degrees or radians that the waveform has shifted either left or right from the reference point.

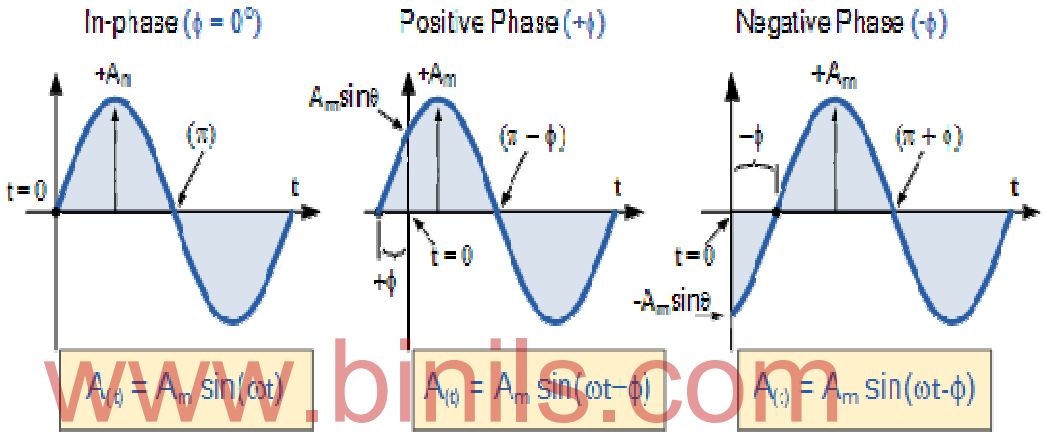
  For example, comparing a voltage waveform to that of a current waveform. This then produces an angular shift or **Phase Difference** between the two sinusoidal waveforms. Any sine wave that does not pass through zero at t = 0 has a phase shift.

The **phase difference** or phase shift as it is also called of a Sinusoidal Waveform is the angle Φ (Greek letter Phi), in degrees or radians that the waveform has shifted from a certain reference point along the horizontal zero axis. In other words phase shift is the

lateral difference between two or more waveforms along a common axis and sinusoidal waveforms of the same frequency can have a phase difference.

Phase Angle: The angle difference between zero crossing points of two wave form.

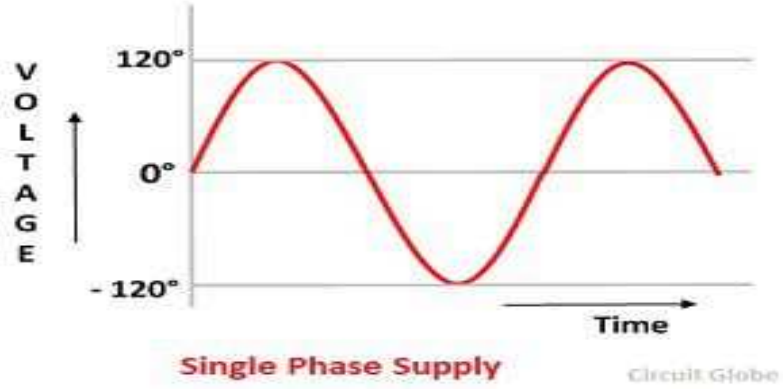
Phase Relationship of a Sinusoidal Waveform



1.1.8 Single phase and 3 phase

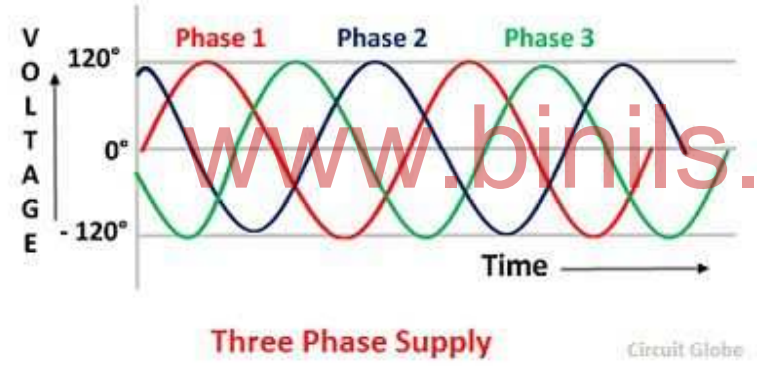
DEFINITION OF SINGLE PHASE

The single phase requires two wires for completing the circuit, i.e., the conductor and the neutral. The conductor carries the current and the neutral is the return path of the current. The single phase supplies the voltage up to 230 volts. It is mostly used for running the small appliances like a fan, cooler, grinder, heater, etc.



Definition of Three Phase

The three phase system consist four wires, three conductors and one neutral. The conductors are out of phase and space 120º apart from each other. The three phase system is also used as a single phase system. For the low load, one phase and neutral can be taken from the three phase supply.



The three phase supply is continuous and never completely drops to zero. In three phase system power can be drawn either in a star or delta configuration. The star connection is used for long distance transmission because it has neutral for the fault current.

Key Differences between Single Phase and Three Phase

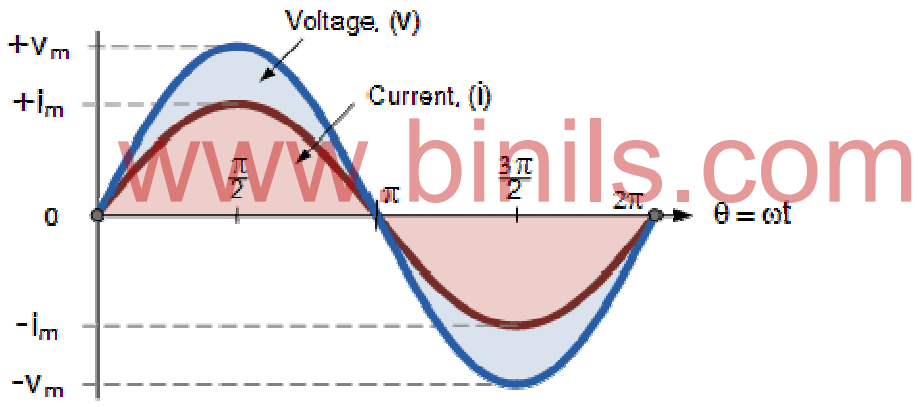
1. In single phase supply, the power flows through one conductor whereas the three phase supply consists three conductors for power supply.
2. The single phase supply requires two wires (one phase and one neutral) for completing the circuit. The three phases requires three phase wires and one neutral wire for completing the circuit.
3. The single phase supplies the voltage up to 230V whereas the three phase supply carries the voltage up to 415V.
4. The maximum power is transferred through three phases as compared to single phase supply.
5. The single phase has two wires which makes the network simple whereas the three phase network is complicated as it consists four wires.

6. The single phase system has only one phase wire, and if the fault occurs on the network, then the power supply completely fails. But in three phase system the network has three phases, and if the fault occurs on any one of the phases, the other two will continuously supply the power.
7. The efficiency of the single phase supply is less as compared to three phase supply. Because the three phase supply requires less conductor as compared to single phase supply for the equivalent circuit.
8. The single phase supply requires more maintenance and become costly as compared to three phase supply.
9. The single phase supply is mostly used in the house and for running the small loads. The three phase supply is used in large industries and for running the heavy loads.

The star connection of the three phases allows the use of two different voltages (i.e., the 230 volts and the 415 volts). The 230V is supplied by using the one phase and one neutral wire, and the three phases is supply between any two phases.

1.1.9 Meaning of lagging and leading sine wave

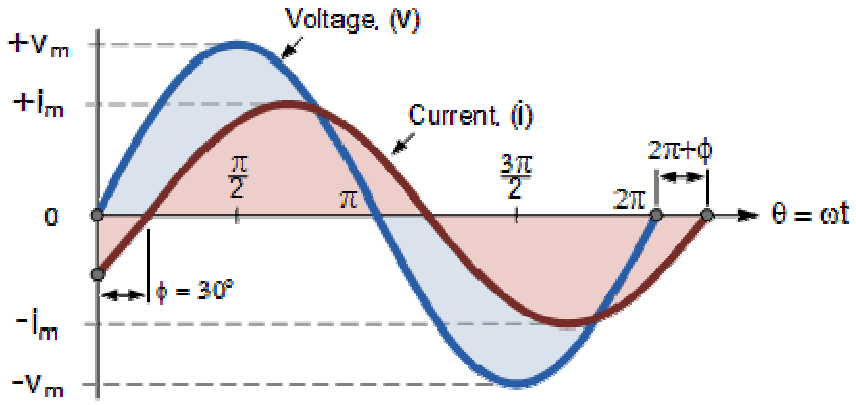
Two Sinusoidal Waveforms – "in-phase"



Both voltage and current crossing zero at 180° or π. Hence V and I are in phase or phase difference between V and I is zero.

i.e. Phase angle between V and I=0.

Phase Difference of a Sinusoidal Waveform



Here V crossing zero at 180° or π.

But I crossing zero after 180. i.e. 180+30 or π+30.

Hence I lagging V by 30° or V leading I by 30°

Phase angle 30°

. .

1.1.10 ADVANTAGES OF THREE PHASE OVER SINGLE PHASE

1. From power wave forms shown in figure (C) and (D) above it is clear that in 3-phase system, the instantaneous power is always constant over the cycle results in smooth and vibration free operation of machine. Whereas in 1-ø system the instantaneous power is pulsating hence change over the cycle, which leads to vibrations in machines.
2. Power to weight ratio of three phase induction motor is high as compare to single phase induction motor. Means for same amount of Mechanical Power, the size of three phase induction motor is small as compare to single phase induction motor. Hence, the overall cost of induction motor is reduced. Moreover, due to reduction in weight, transportation and installation of induction motor become convenient and less space is required to accommodate the induction motor.
3. 3-phase induction motor is self-started as the magnetic flux produced by 3-phase supply is rotating in nature with constant magnitude. Whereas 1-ø induction motor is not self-started as the magnetic flux produced by 1-ø supply is pulsating in nature. Hence, we have to make some arrangement to make the 1-ø induction motor self-started which further increases the cost of 1-ø induction motor.
4. 3-phase motor is having better power factor and efficiency as compare to 1-ø motor.
5. Power to weight ratio of 3-phase transformer is high as compare to 1-ø transformer. Means for same amount of Electric Power, the size of 3-phase transformer is small as compared to 1-ø transformer. Hence, the overall cost of transformer is reduced. Moreover, due to reduction in weight, transportation and installation of transformer become convenient and less space is required to accommodate the transformer.

6. If fault occurs in any winding of 3-phase transformer, the rest of two winding can be used in open delta to serve the 3-phase load which is not possible in 1-ø transformer. This ability of 3-phase transformer further increases the reliability of 3-phase transformer.
7. A 3-phase system can be used to feed a 1-ø load, whereas vice-versa is not possible.
8. DC rectified from 3-phase supply is having the ripple factor 4% and DC rectified from 1-ø supply is having the ripple factor 48.2%. Mean DC rectified from 3-ø supply contains less ripples as compare to DC rectified from 1-ø supply. Hence the requirement of filter is reduced for DC rectified from 3-phase supply. Which reduce the overall cost of converter.

From above it is clear the 3-phase system is more economical, efficient, reliable and convenient as compared to 1-ø system.

1.2 BATTERIES

1.2.1 Classification of Cells or Batteries

The Nickel Cadmium (NiCd) battery.

The Nickel-Metal Hydride (NiMH) battery.

The Lead Acid battery.

The Lithium Ion battery.

The Lithium Polymer battery.

A primary cell or battery is one that cannot easily be *recharged* after one use, and are discarded following discharge. Most primary cells utilize electrolytes that are contained within absorbent material or a *separator* (i.e. no free or liquid electrolyte), and are thus termed dry cells.

A secondary cell or battery is one that can be electrically recharged after use to their original pre-discharge condition, by passing current through the circuit in the opposite direction to the current during discharge.

The following graphic evidences the recharging process

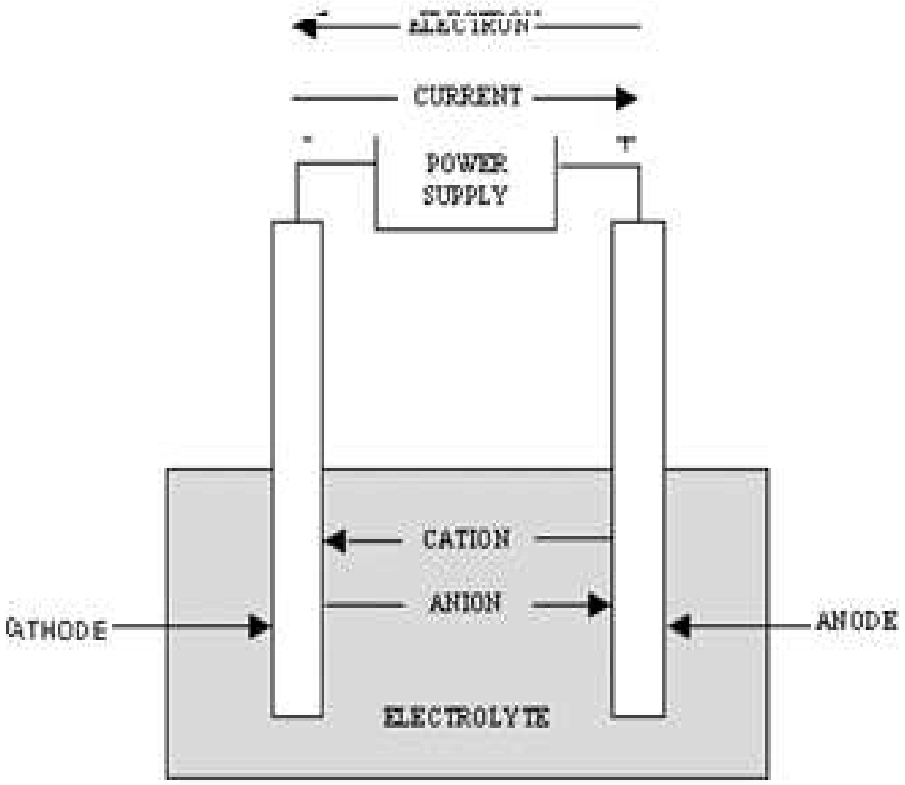


Figure 3: Recharging a Cell

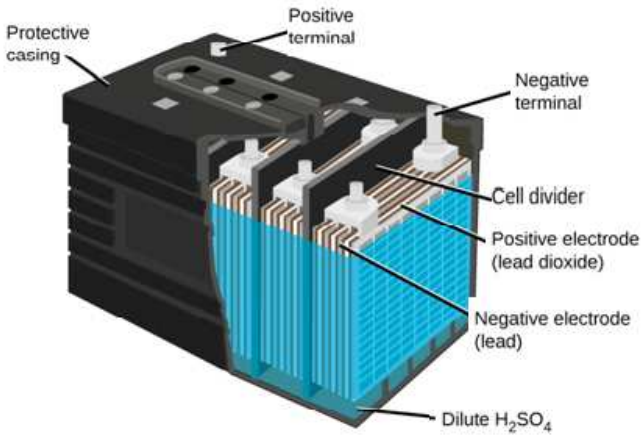
1.2.2 CONSTRUCTION OF LEAD ACID CELL

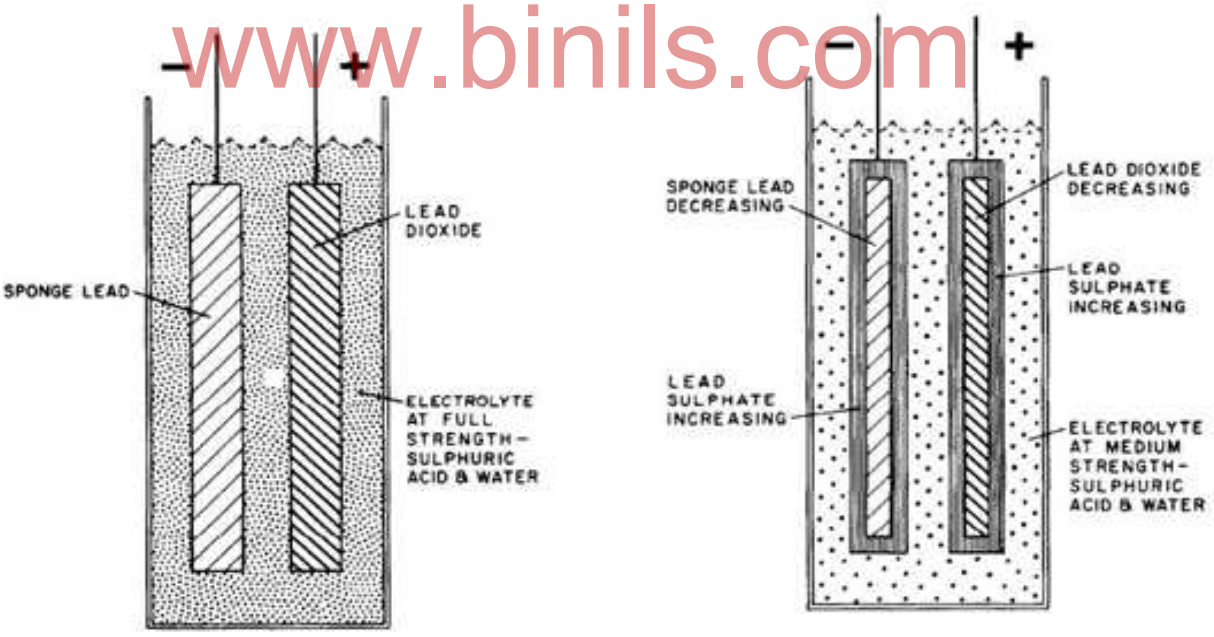
In the fully charged state, the negative plate consists of lead, and the positive plate lead dioxide, with the electrolyte of concentrated sulfuric acid. Overcharging with high charging voltages generates oxygen and hydrogen gas by electrolysis of water, which is lost to the cell.

LEAD ACID BATTERY

In lead acid battery there is a group of cells and in each cell there is one group of positive plates and one group of negative plates. The **positive plates** are made of lead peroxide **(PbO2)** and **negative plate** is made of **spongy lead**. Thus for identification the **positive plate** as the color of **dark brown**, whereas the **negative plate** as the **color of light salty.**

MAIN PARTS OF LEAD ACID BATTERY

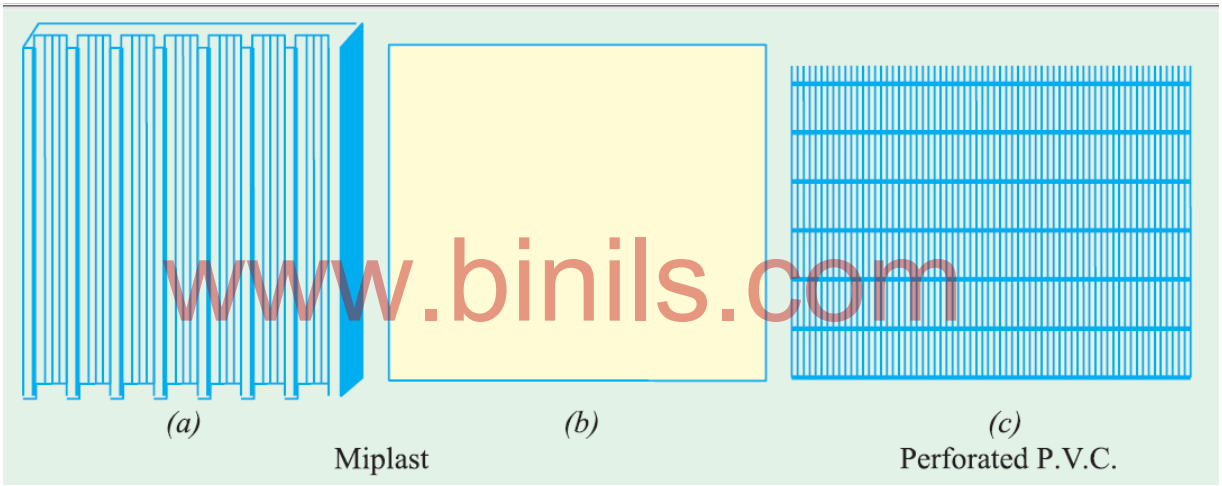




A battery consists of a number of cells and each cell of the battery-consists of (a) positive and negative plates (b) separators and (c) electrolyte, all contained in one of the many compartments of the battery container. Different parts of a lead-acid battery are as under:

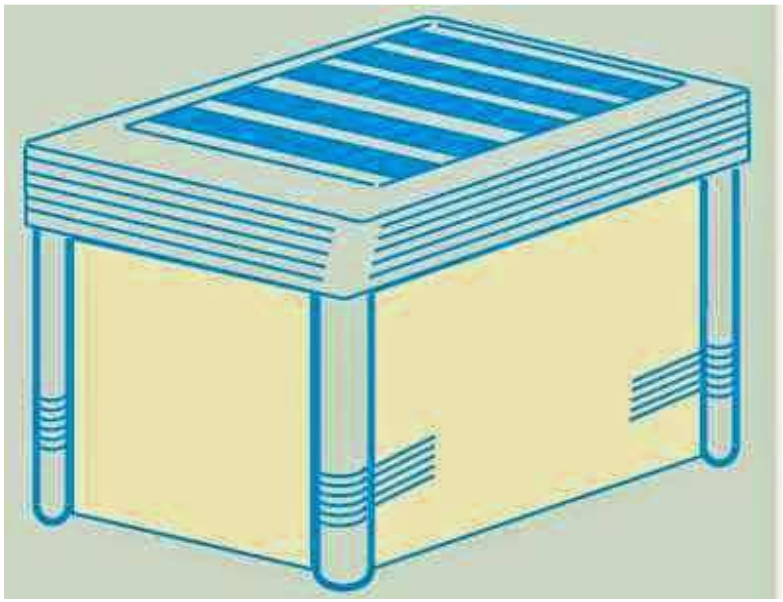
(I)PLATES: A plate consists of a lattice type of grid of cast antimonial lead alloy which is covered with active material. The grid not only serves as a support for the fragile active material but also conducts electric current. Grids for the positive and negative plates are often of the same design although negative plate grids are made somewhat lighter**.**

(II) SEPARATORS: These are thin sheets of a porous material placed between the positive and negative plates for preventing contact between them and thus avoiding internal short-circuiting of the battery. A separator must, however, be sufficiently porous to allow diffusion or circulation of electrolyte between the plates. These are made of especially-treated cedar wood, glass wool mat, micro porous rubber (mipor), micro porous plastics (plastipore, miplast) and perforated PVC, as shown in Figure In addition to good porosity, a separator must possess high electrical resistance and mechanical strength.



(III)ELECTROLYTE*:* It is dilute sulphuric acid which fills the cell compartment to immerse the plates completely**.**

(IV) CONTAINER: It may be made of vulcanized rubber or molded hard rubber (ebonite), molded plastic, ceramics, glass or celluloid. The vulcanized rubber containers are used for car service, while glass containers are superior for lighting plants and wireless sets. Celluloid containers are mostly used for portbable wireless set batteries. A single mono-block type container with 6 compartments generally used for starting batteries is shown in Figure.



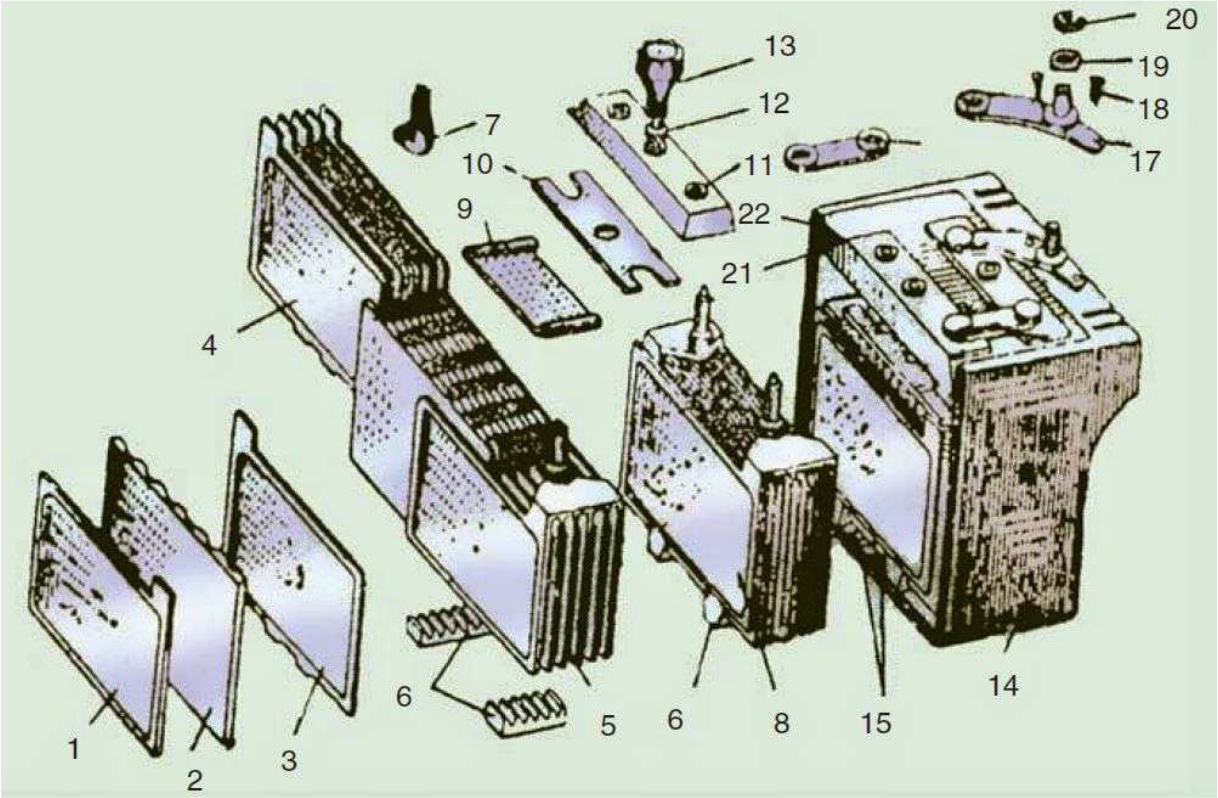
(V) BOTTOM GROOVED SUPPORT BLOCKS*:* These are raised ribs, either fitted in the bottom of the container or made with the container itself. Their function is to support the plates and hold them in position and at the same time protect them from short-**circuits that** would otherwise occur as a result of fall of the active material from the plates onto the bottom of the container**.**

(VI) CONNECTING BAR: It is the lead alloy link which joins the cells together in series connecting the positive pillar of one cell to the negative pillar of the next one.

(VII) TERMINAL POST OR PILLAR*:* It is the upward extension from each connecting bar which passes through the cell cover for cable connections to the outside circuits. For easy identification, the negative terminal post is smaller in diameter than the positive terminal post**.**

(VIII) VENT PLUGS OR FILLER CAPS*:* These are made of polystyrene or rubber and are usually screwed in the cover. Their function is to prevent escape of electrolyte but allow the free exit of the gas. These can be easily removed for topping up or taking hydrometer readings.

(IX) EXTERNAL CONNECTING STRAPS*:* These are the antimonial lead alloy flat bars which connect the positive terminal post of one cell to the negative of the next across the top of the cover. These are of very solid construction especially in starting batteries because they have to carry very heavy currents**.**



1. -ve plate
2. Separator
3. + Ve plate.
4. + ve group
5. -ve group
6. -ve group grooved support block
7. Lug
8. Plate group
9. Guard screen
10. Guard plate
11. Cell cover
12. Plug washer
13. Vent plug
14. Mono-block jar
15. Supporting prisms of + ve group
16. Inter-cell connector
17. Terminal lug
18. Screw
19. Washer
20. Nut
21. Rubber packing
22. Sealing compound.

1.2.3METHODES OF CHARGING

BASIC CHARGING METHODS

Charging Methods charging is a process of supplying direct current to the battery so as to convert it back into chemical state at high energy level, capable of delivering electric power**.**

Charging voltages have a significant effect on battery longevity. Some cells may deteriorate faster than others during operations. Deteriorated cells reduce the output voltage of the battery, and affect the usability and reliability of the circuit .

There are varieties of charging methods which can be used to charge sealed lead acid battery.

By controlling the charging process, these methods can be classified into some basic categories which are

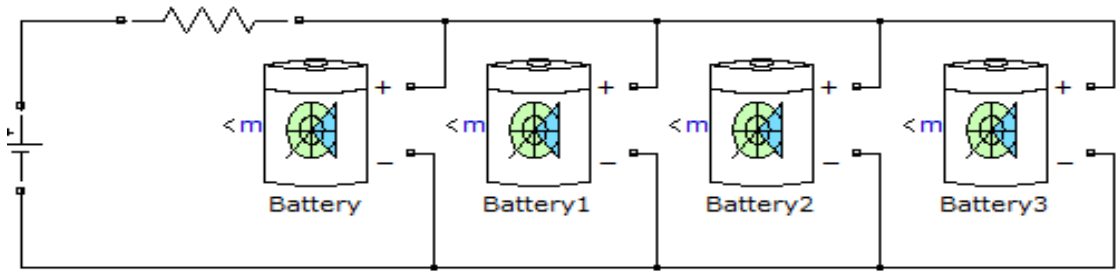
(i) constant-voltage,

(ii) constant-current,

(iii) tapered-current

(iv) Combination charge systems..

1.2.3.1CONSTANT VOLTAGE



A constant voltage charger is basically a DC power supply which in its simplest form may consist of a step down transformer from the mains with a rectifier to provide the DC voltage to charge the battery.

Such simple designs are often found in cheap car battery chargers.

The lead-acid cells used for cars and backup power systems typically use constant voltage chargers.

In addition, lithium-ion cells often use constant voltage systems, although these usually are more complex with added circuitry to protect both the batteries and the user safety.

Constant voltage charging is a methods use to restore the battery to a fully charge condition in short period of time.

This type of charging must has a very stable output voltage and high current capacity, as extremely large currents are allowed to flow in the initial stage of charge, where the battery voltage is low.

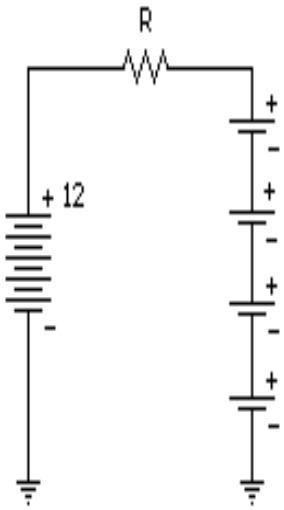
However, this type of charging method is not practical because the requirement of a high current capacity, results in high cost.

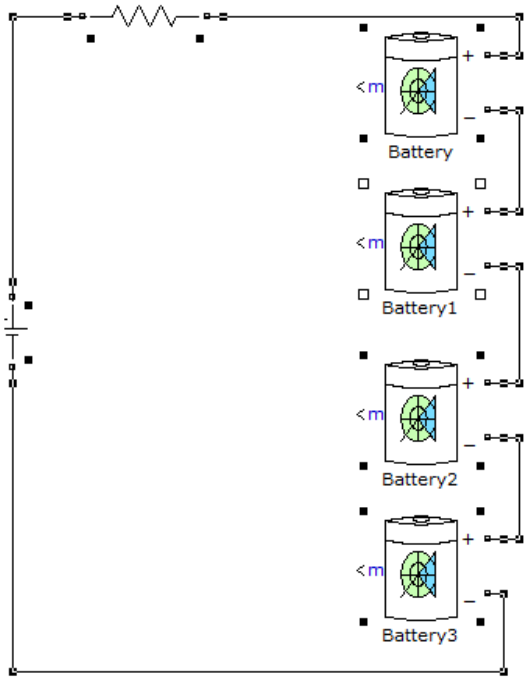
The heat generation in the battery is also high because of the high current flow in the battery causing the battery life to be short.

Generally, constant voltage charger has a device to limit initial current. This can be accomplished by a constant current regulator, or by designing the overall impedance of the circuit.

Constant voltage charger is effectively to charge the battery at short period of time, as during the final stage of charge, the current automatically decreases and the water decomposition will be minimized.

1.2.3.2CONSTANT CURRENT





Constant current charging is a method that is commonly uses for charging lead acid battery.

The advantage of using this method is it easy to determine the amount of capacity (amp hrs) supplied during charging process.

Besides that, there is no need for temperature compensation which is required in constant voltage systems.

Usually, at high-rate of charging, the battery voltage rises excessively and the water decomposes, causing heat generation at the final stage of the charge, thus, damaging the battery.

However, the constant current method relatively kept a low rate of charging process and charging time is not critical.

The constant current methods may be used as refreshing charge when many batteries is being charge at one time, as this method easily determine the amount of charge returned to the battery.

It is not recommended to use constant current charging as refreshing the battery because it will shorten the battery life.

Constant current chargers vary the voltage they apply to the battery to maintain a constant current flow, switching off when the voltage reaches the level of a full charge. This design is usually used for nickel-cadmium and nickel-metal hydride cells or batteries.

1.2.3.3TAPER CURRENT

Tapered current charging is simple and relatively inexpensive method.
This charging method requires circuit with power transformer, rectifiers and a suitable resistance for limiting current.

In this method, the charging current drops gradually as the charging proceeds. If the impedance of the circuit is low, a step current slope can be obtained.

This type for charge is generally considered to be unsuitable for charging sealed lead acid batteries because the charging current will vary with fluctuation of line voltage as well as changes in battery voltage.

These effects, however, can be minimized by using a power transformer with a secondary voltage which is considerably higher than the battery voltage and a suitably high resistance in the circuit for current limiting.

This type of charger will perform similar to a constant current charger, and can be utilized instead of a constant current charger for industrial uses; not only for recharging many batteries at one time, but also as a trickle charging system.

1.2.3. Combination Charging (Two-Step)

A combination charging uses two types of charging. It‘s called a —Two-rate or —Two-step charging.

A variety of couples can be made, such as constant – current/constant current, constant-voltage/constant-current and so on .

In general the first step uses a quick or fast charge mode, and the second uses a low charge current.

The switching from the first step to the second can be carried out by many different methods such as battery voltage sensing, a time control, charge current sensing and many more.

1.2.4 CARE AND MAINTENANCE OF LEAD ACID BATTERY

REGULAR INSPECTION AND MAINTENANCE.

Regular testing and inspection will help to maximize battery life. A routine inspection at least once a month is recommended to maintain optimum performance.

1. Ensure the battery top is clean and dry, free of dirt and grime. A dirty battery can discharge across the grime on top of the battery casing.

2. Inspect the terminals, screws, clamps and cables for breakage, damage or loose connections. These should be clean, tight and free of corrosion.

3. Apply a thin coating of high temperature grease to posts and cable connections for added protection.

4. Inspect the battery case for obvious signs of physical damage or war page. This usually indicates the battery has overheated or has been overcharged.

5. If the battery is maintainable, check electrolyte levels to ensure that fluid levels are over the top of battery plates. If necessary top up using distilled or demine rallied water. Never top up fluid levels with acid.

6. Test the battery using either a hydrometer or voltmeter and charge if necessary.

7. Keep vent caps in place.

8. Charge in well ventilated area.

9 .Apply petroleum products or Vaseline (both are use corrosion precaution)

10. Watering

Watering is the single most important step in maintaining a flooded lead acid battery; a requirement that is all too often neglected. The frequency of watering depends on usage, charge method and operating temperature. Over-charging also leads to water

consumption.

A new battery should be checked every few weeks to estimate the watering requirement. This assures that the top of the plates are never exposed. A naked plate will sustain irreversible damage through oxidation, leading to reduced capacity and lower performance.

If low on electrolyte, immediately fill the battery with distilled or de-ionized water. Tap water may be acceptable in some regions. Do not fill to the correct level before charging as this could cause an overflow during charging. Always top up to the desired level after charging. Never add electrolyte as this would upset the specific gravity and promote corrosion. Watering systems eliminate low electrolyte levels by automatically adding the right amount of water.

11. Specific gravity.

The specific gravity of the electrolyte may be permanently decreased due to ageing effects. This problem is generally found in old battery cells. This is mainly due to,

1. Action of sediment-at the bottom of the cell container.
2. Due to loss of acid by spray during charging.
3. Inadequate treatment after the removal short circuit.
4. Due to excessive sulphation on the plates.

If the lowering of specific gravity is not due to sulphation or short circuit, concentrated sulfuric acid may be added to restore normal value of specific gravity.

A short circuit may occur between the positive and negative plates either due to treeing or due to buckling of the plates.

Treeing is usually due to excessive gassing which tends to loosen the active materials from the plates. The particles of active materials fall into the electrolyte and may accumulate on the negative plates in such a way as to bridge the space between the positive and negative plates. This treeing can be removed by the use of scaling stick made of ebonite. By this stick it is possible to explore the space between these two types of plates of a cell and to remove loose materials or treeing.

If the short circuit is due to buckling of plates, this can be removed by inserting additional separator or by removing and straightening the plates mechanically.

After removing of short circuit, care should be taken to restore the specific gravity of the electrolyte to normal by constant charging by high current.

1.2.5Indications of a fully charge battery

There are two measures,

(I) cell voltage

(ii) Specific gravity of the electrolyte.

*Cell voltage is the simplest to measure. For most automotive, flooded cell

(Having liquid electrolyte) batteries, 12.6 volts are considered full charge,

Although it is typical to have 13 volts or a bit over.

*The specific gravity of a fully charged battery, measured with a hydrometer, is 1.265.

*If the charger has a ammeter on it then it should show close to zero which means

the battery is no longer pulling any current from the charger which would mean

the battery is fully charged.

*If it has only a voltmeter then it should show 12.5-13.5 vdc.

*When a battery is fully charged, the amount of sulfuric acid mixed with the

water is sufficient to give a specific gravity of about 1.3.

* In the fully charged condition the active material of the positive plate is lead Dioxide as the color of **dark brown**, whereas the **negative plate** sponge lead as the **Color of light salty**, indicated electrolyte is a solution of sulfuric acid and water that normally varies in specific gravity from 1.275 to 1.295.

*The combination produces a voltage of approximately 2 volts on open circuit.

*A fully charged cell should normally have an on-charge voltage of from 2.45 to 2.7

1.2.6Sealed or maintenance-free batteries

Sealed or maintenance free Batteries have the following features: -

i) Maintenance-free, no water adding required

ii) Sealed valve-regulated, spill proof and leak proof

iii) Using unilateralism exhaust (safe vent valve) design on the battery cover When the battery internal pressure have been up to the specifically value, the safe vent valve will open automatically, and will close after the pressure has been discharged, which can prevent the air to enter into battery

They are designed in such a way as to recover a large portion of the electrolyte that is normally lost through gassing of a normal wet cell.

Even so, these batteries will lose electrolyte over time, causing premature failure due to overcharging.

Use

They are suitable to be used

i) Standby or cyclical

ii) Security sector (alarm),

iii) Electronically devices,

iv) Telephone exchange and UPS.

1.3 UPS

The ever increasing importance of computers in industry and commerce will increase the need for quality, high stability and interruption free power supplies.

A clean ac power source is the fundamental to the operation of most sensitive electronic equipment, and many new and sophisticated circuits are designed to overcome the effects of disturbances normally found in the mains ac supply.

In order to protect a sensitive system from power losses and blackouts, an alternative power source is required that can switch into operation immediately when disruption occurs. Un interruptible power supply (UPS) is just such an alternative source. A UPS generally consists of a rectifier, battery charger, a battery bank and inverter circuit which converts the commercial ac input into dc suitable for input to the battery bank and the inverter. The rectifier should have its input protected and should be capable of supplying power to the inverter when the commercial supply is either slightly below the normal voltage or slightly above.

What is UPS?
An uninterruptible power supply (**UPS**) is a device that allows a computer to keep running for at least a short time when the primary power source is lost. It also provides protection from power surges.

1.3.1NEED FOR UPS

An Uninterruptible Power Supply (UPS) is used to protect critical loads from mains supply problems, including spikes, voltage dips, and fluctuations and complete power failures using a dedicated battery. A UPS system can also be used to 'bridge the gap' whilst a standby generator is started and synchronized.

1.3.2Uninterruptible Power Supply Systems.

There are two distinct types of uninterrupted power supplies, namely,

Definition

On-line UPS

In the on-line UPS, whether the mains power is on or off, the battery operated inverter is on all the time and supplies the ac output voltage. When the mains power supply goes off, the UPS will be on only until the battery gets discharged. When the main power resumes, the battery will get charged again.

UPS. (Uninterruptible Power Supply) A device that provides battery backup when the electrical power enough to power down the computer in an orderly manner, while larger systems have enough battery for several hours. fails or drops to an unacceptable voltage level. Small UPS systems provide power for a few minutes

Off-line UPS

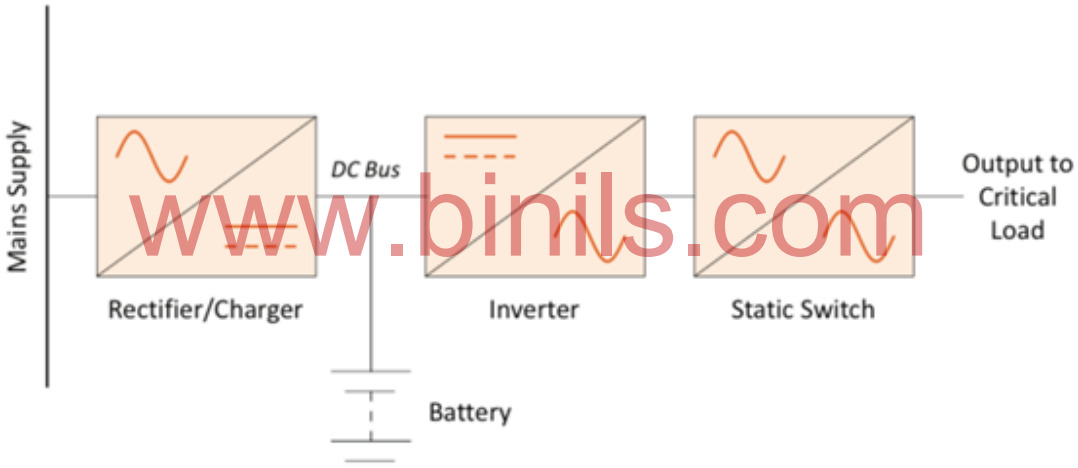
In off-line UPS and electronic generators, the inverter is off when the mains power is present and the output voltage derived directly from the mains is the same as the mains supply voltage. The inverter turns on only when the mains supply goes off.

Standby and Line Interactive. A standby UPS, also called an "offline UPS," is the most common type of UPS found in a computer or office supply store. It draws current from the AC outlet and switches to battery within a few milliseconds after detecting a power failure.

1.3.3Block Diagram

Online UPS

An online UPS comprises four main parts: A rectifier/charger block, a battery, an inverter and a static switch. To see how these components fit together, have a look at the following simple block diagram.



1.3.4Explanation of each block

Rectifier/Charger block– Although I've listed them together, the rectifier and charger can either be separate modules or combined as a single power block. They perform the same function either way, so for the sake of simplicity they are displayed in our block diagram as a single component.

The function of this combined power block is to take AC (Alternating Current) power from the mains, and convert it to DC (Direct Current) power, which is required to charge the battery. From there the charger directs power to the battery in order to maintain charge, and the rectifier provides a stable DC current directly to the inverter, all via the DC Bus.

During times of power outage or fluctuation (typically outside +10% to -20% of normal) the charger shuts down, and the battery provides DC power to the inverter instead.

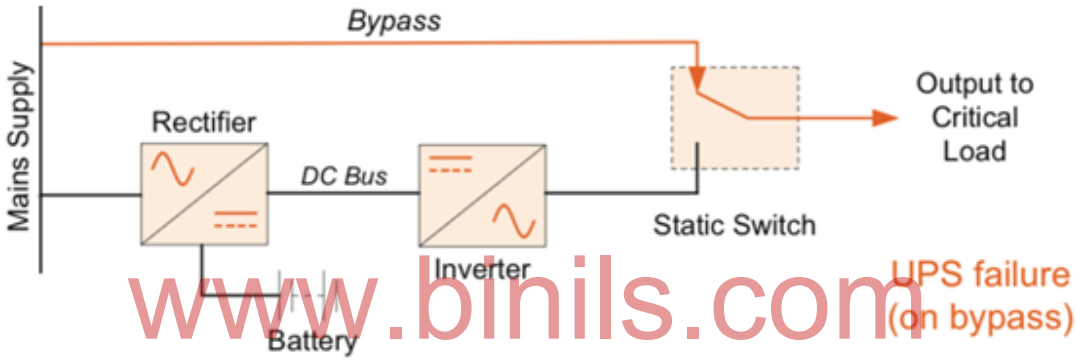
Battery– most UPS systems utilize lead-acid batteries.

Inverter– The inverter provides the second half of our double conversion process, by converting DC power from the rectifier/battery back to AC power. We needed DC power to charge the battery, but its AC power that's required by your critical loads, so this secondary conversion process is vital.

One of the main benefits of an online UPS is that it provides the greatest level of protection to your critical load from power 'events' such as spikes, sags, surges, electrical noise, and so on. This is because, unlike the other types of UPS described in our last article, all of the power supplied to your critical load has been routed through the UPS, and thus undergone the double conversion process from AC to DC and then back to AC.

Static Switch

The switch has two modes; by default the switch will accept AC power from the UPS, but it also has the option to accept AC power directly from the mains, or 'bypass'.



Switching over to mains power is far from ideal, so in the event your critical loads are transferred to raw mains power it will be accompanied by an alarm or warning condition to ensure the UPS issue is resolved as quickly as possible.

Operation:

- During normal or even abnormal line conditions, the inverter supplies energy from the mains through the rectifier, which charges the batteries continuously. In addition to that it can also provide power factor correction.
- When the line fails, the inverter still supplies energy to the loads from the batteries.
- As a consequence, no transfer time exists during the transition from normal to stored energy modes.
- In general, Online UPS system is the most reliable UPS configuration due to its simplicity (only three elements), and the continuous charge of the batteries, which means that they are always ready for the next power outage.
- This kind of UPS provides total independence between input and output voltage amplitude and frequency. So high output voltage quality can be obtained.
- When an overload occurs, the bypass switch connects the load directly to the utility mains, in order to guarantee the continuous supply of the load, thereby avoiding the damage to the UPS module (bypass operation).
- In this situation, the output voltage must be synchronized with the utility phase, otherwise the bypass operation will not be allowed.

- Typical efficiency of the online ups systems are up to 94%, which is limited due to the double conversion effect.
- Online UPS systems are typically used in environments with sensitive equipment or environments.
- Almost all commercial UPS units of 5 kVA and above are Online UPS Systems.

1.3.5Merits and demerits of online and off-line UPS

Merits of on- line ups

- It provides isolation between main supply and load.
- Since inverter is always ON, the quality of load voltage is free from distortion
- All the disturbances of supply such as blackout, brownouts, spikes etc are absent in the output.
- Voltage regulation is better
- Transfer time is practically zero since inverter is always ON.

Demerits of Online UPS:

- Overall efficiency of UPS is reduced since inverter is always ON.
- The wattage of the rectifier is increased since it has to supply power to inverter as well as charge battery
- Online UPS is costlier than other Uninterruptible Power Supply Systems.

Applications of Online UPS:

- Induction motor drives and similar other motor control applications.
- Intensive care units, medical equipments.

Merits of Offline UPS:

- Offline UPS has high efficiencies, since charger is not continuously on.
- The power handling capacity of charger is reduced.
- Offline UPS are not very costly.
- Internal control is simpler in offline Uninterruptible Power Supply.

Demerits of Offline UPS:

- Since offline UPS provides mains supply when it is present, the output contains voltage spikes, brownouts, blackouts.
- There is finite transfer time from mains to inverter when mains supply fails.
- Output of offline Uninterruptible Power Supply is not perfectly reliable.

Applications of Offline UPS:

- Computers, printers, scanners etc use offline UPS.
- Emergency power supplies, EPABX.
-

1.3.6Need of Heat sink:

The UPS carrier high current depending upon the load this current also flow throws the switching Device such as transistor, SCR used in the UPS.

They always heat up during operation since the electronic components are temperature dependent devices. The heat generated must be dissipated to the surroundings in order to keep the temperature within permissible limits. Generally these devices are fixed on a metal sheet (usually aluminum) so that additional heat is transferred to the aluminum sheet. The metal Sheet that serves to dissipate the additional heat from the power semi conductor devices is known as heat sink.

1.3.7Specification and Ratings

Sample Single Phase UPS Specification	
UPS Output:	**Specification**
Voltage	220Vac
Frequency	50Hz nominal, synchronized,
Power Rating	1000VA
Load Power Factor	0.6
Load Crest Factor	3:1
Transfer Time	5 milliseconds
Current	8.3 Amps
Overload Capability	150%
Waveform	Sine-wave
Distortion	< 3% for non-linear loads
UPS Input	
Voltage	220V
Voltage Range	+10%, -15%

Frequency	50Hz
Maximum Current	12.8 Amps
Power Factor	0.9
UPS Battery	
Type	Sealed lead-acid, maintenance free
Rating	12V, 7AH
Number of Cells	3
Diagnostics	Periodic automatic test
Autonomy Time	10 minutes at full load
Recharge Time	20 times the outage to 90% capacity.
Overall System	
Architecture	Fault-tolerant, Double Conversion, On-Line, Modular
Configuration	Single-Phase Input and Output
Bypass	Automatic operation
Efficiency	85%
Operation	Fully Automatic or Manual Operation,
Control Panel/Metering	LED Display, Button Controls, No Metering
Diagnostics & Self Test	Self test on startup and periodically

Communications	
User Interface	RS232 port and Novell style contacts
Networks	Via an Ethernet or Token Ring adapter
SNMP	Via an SNMP adapter
Modem	Via a modem adapter
Mechanical	
Input	Hardwired
Output	Hardwired
Weight	15.8 kg (35 lbs)
Dimensions (LxWxH)	499 x 134 x 226 mm (19.6 x 5.3 x 8.9 inches)
Environmental	
Audible Noise	< 50 dBA
Operating Temperature	30°c
Storage Temperature	- 20°c
Relative Humidity	5 - 95% non-condensing
Altitude	1000m without derating
Safety	UL 1778
EMC - Emissions	FCC Class A
EMC - Immunity	Not Applicable
Surge Suppression	IEEE 587 (ANSI C62.41)
CMNR	> 60dB

TMNR	> 80dB
Packaging	No CFC's, Recyclable
Options	
Battery Packs	Battery Modules and special long autonomy solutions

UPS Output Specifications

Voltage	The UPS output voltage must match the requirement of the load. In North America this voltage is 120Vac, in most of Europe 230Vac is used and the rest of the world is 220Vac.
Regulation	The regulation specification is the maximum expected deviation for the normal output voltage (e.g. 220Vac) that is expected over the entire range of operating conditions (e.g. load, temperature, altitude). For Off-Line systems the regulation spec refers to the battery backup mode.
Frequency	The frequency of the UPS output must match the requirements of the load. Switch-mode power supplies have a wide (47 - 63 Hz) range to be able to operate from either 50 or 60Hz. Other loads may require either 50 or 60Hz.
Power Rating	To completely specify a UPS, both the Volt-Ampere (VA) and wattage (Watts) rating must be known. See the section on "Understanding Watts, VA and Power Factor" for an in-depth explanation.
Load Power Factor	A power factor (p.f.) in the 0.6 to 0.8 range is typical. A p.f. rating of 0.6 to 0.7 is good for a switch-mode power supply. A p.f of 0.8 is typical for older UPS equipment designs used before the widespread use of computers.
Load Crest Factor	Most loads used in modern equipment, including computers, require a peak current that is much higher than what is required by a simple load such as a light bulb. The UPS must be able to supply this peak current. The Load Crest Factor is the ratio of the peak to the average (RMS) current.

Transfer Time	In an On-Line system the transfer time refers to a change from the bypass source to the UPS and vice-versa. A typical time is ¼ of a cycle or about 5-6 milliseconds. In an Off-Line system the transfer time refers to the change from the utility source to the inverter when there is a power outage and is about 5 to 10 milliseconds.
Current	The output current refers to the maximum current available at the normal output voltage.
Overload Capability	If more loads is added to a UPS and the new total is more than the rating, the UPS must be able to continue to function. At typical Overload specification is 1.25% for 10 minutes or 150% for 1 minute.
Waveform	Not all UPS products have a sine-wave output and most modern loads do not require a perfect sine-wave source. Lower cost UPS equipment will have a quasi square-wave or a step sine-wave output waveform.
Distortion	If the UPS has a sine-wave output a distortion figure indicates how good the wave shape is. A typical distortion value is 3% for linear loads and 5% for non-linear load.
Transient Regulation	When a load is added or removed the UPS inverter has to adjust. The maximum amount the output voltage deviates from the nominal value indicates the transient regulation. If the voltage deviates too much, some loads will fail.

UPS Input Specifications

Voltage	The input voltage specification is the nominal voltage the UPS expects to see on its input.
Voltage Range	All UPS products are designed to operate over a range of input voltages. A typical range is +10% to -15% or 102Vac to 132Vac for North America or 196Vac to 253Vac for Europe.
Frequency	Modern UPS equipment will operate on either 50 or 60Hz as long as the voltage is within the specified limits. Some UPS equipment is designed to operate only on 50 or 60Hz.
Maximum Current	The maximum current occurs when the UPS is fully loaded and the input voltage is at the minimum

	allowed for normal operation (usually about -15%).
Power Factor	The UPS input is a load on the utility power source. The UPS input power factor (p.f.) varies with how much load is on the output of the UPS and in modern UPS equipment is 0.9 or better. In large UPS equipment (e.g. 25kVA) the input power factor could be a very important part of the overall system design. In small UPS equipment, power factor is usually not a concern unless many units are being installed.

UPS Battery Specifications

Type	The most common battery used in UPS equipment is a sealed, lead-acid, maintenance free type. Ni-Cad (Nickel-Cadmium) batteries are a more expensive option. Large UPS systems often use wet, lead-acid storage batteries.
Rating	Batteries are rated by specifying an open circuit DC voltage and a Ampere-Hour (AH) rating.
Number of Cells	Battery cells are normally connected in series to form a string. Often battery strings are connected in parallel.
Diagnostics	The battery is the weakest link in a UPS system. Automatic checking and diagnostics of battery problems is now common in UPS products. Testing must not put the load in jeopardy.

1.3.8Maintenance of UPS including batteries

Regular equipment testing should be part of a facility's UPS maintenance schedule. Such a schedule might include the following elements:

Quarterly:

• Visually inspect equipment for loose connections, burned insulation or any other signs of wear.

Semiannually:

• Visually check for liquid contamination from batteries and capacitors.
• Clean and vacuum UPS equipment enclosures.
• Check HVAC equipment and performance related to temperature and humidity.

Annually:

• Conduct thermal scans on electrical connections to ensure all are tight and not generating heat, which is the first and sometimes only indication of a problem. A non-evasive diagnostic tool helps technicians identify hot spots invisible to the human eye. Technicians should retorque if thermal scan provides evidence of a loose connection.
• Provide a complete operational test of the system, including a monitored battery-rundown test to determine if any battery strings or cells are near the end of their useful lives.

Biannually:

• Test UPS transfer switches, circuit breakers and maintenance bypasses.

UNIT II TRANSFORMER AND SPECIAL MOTORS

OBJECTIVES:

- **Understand the concept of transformer**
- **Know the working and parts of a transformer**
- **Know about the stepper motors and servo motors**
- **Know the electrical safety**

2.1.1 Single phase Transformer

Definition of Transformer

Electrical power transformer is a static device which transforms electrical energy from one circuit to another without any direct electrical connection and with the help of mutual induction between two windings. It transforms power from one circuit to another without changing its frequency but may be in different voltage level.
This is a very short and simple **definition of transformer**,

2.1.2Working Principle of Transformer

The **working principle of transformer** is very simple. It depends upon **Faraday's law of electromagnetic induction**. Actually, mutual induction between two or more winding is responsible for transformation action in an electrical transformer.

Faraday's Laws of Electromagnetic Induction

According to these **Faraday's laws,**
"Rate of change of flux linkage with respect to time is directly proportional to the induced EMF in a conductor or coil".

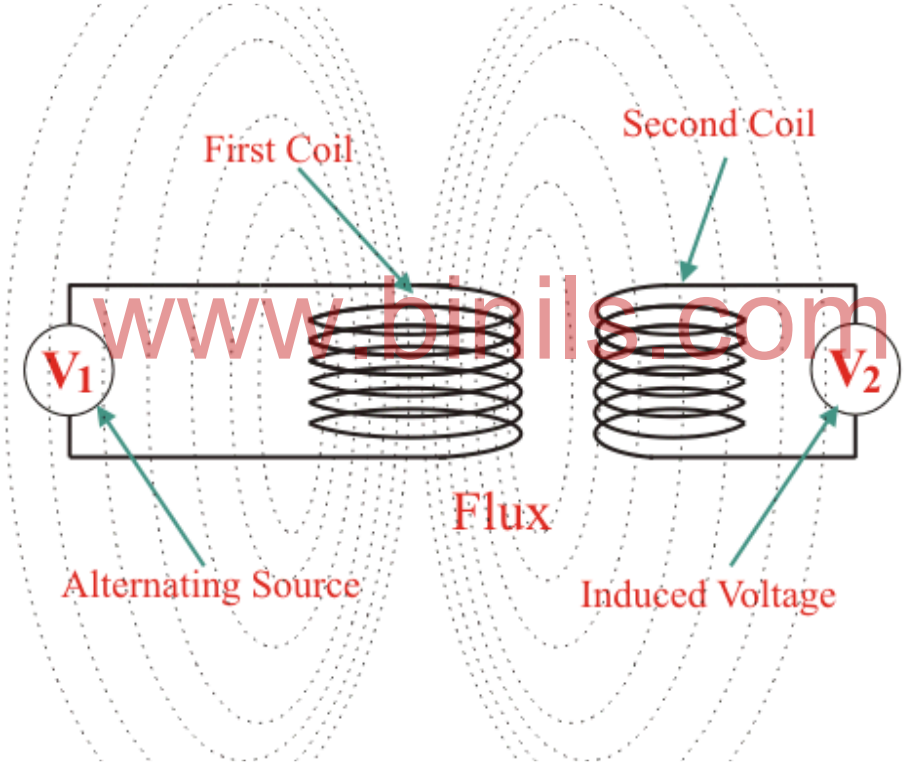
Basic Theory of Transformer

Say you have one winding which is supplied by an alternating electrical source. The alternating current through the winding produces a continually changing flux or alternating flux that surrounds the winding. If any other winding is brought nearer to the previous one, obviously some portion of this flux will link with the second. As this flux is continually changing in its amplitude and direction, there must be a change in flux linkage in the second winding or coil. According to **Faraday's Laws of Electromagnetic Induction**

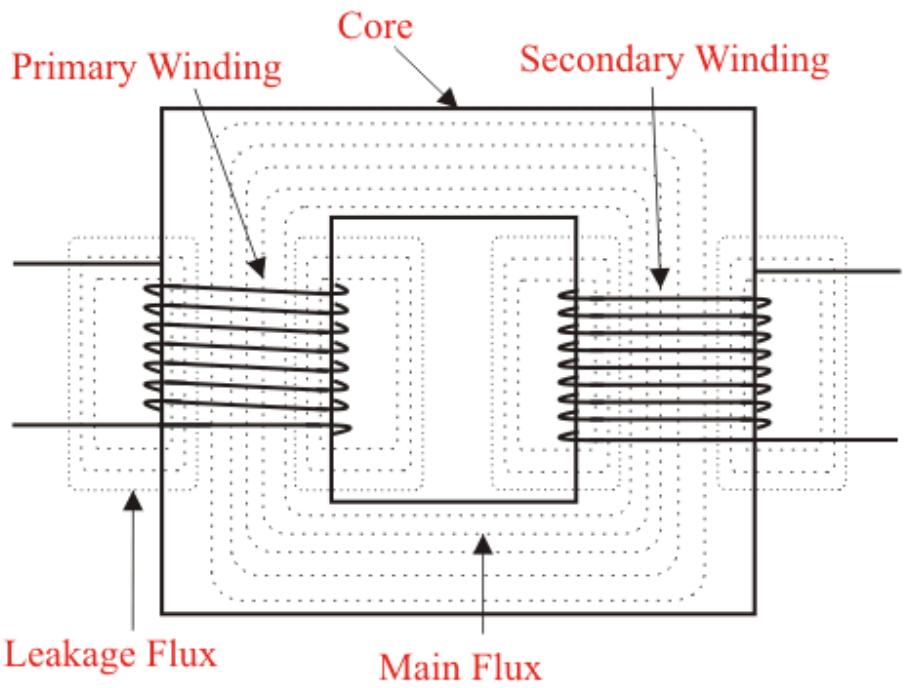
, there must be an EMF induced in the second. If the circuit of the later winding is closed, there must be an current flowing through it. This is the simplest form of electrical power transformer and this is the most basic of **working principle of transformer**.

For better understanding, we are trying to repeat the above explanation in a more brief way here. Whenever we apply alternating current to an electric coil, there will be an alternating flux surrounding that coil. Now if we bring another coil near the first one, there will be an alternating flux linkage with that second coil. As the flux is alternating, there will be obviously a rate of change in flux linkage with respect to time in the second coil. Naturally emf will be induced in it as per **Faraday's Laws of Electromagnetic Induction**

. This is the most basic concept of the **theory of transformer**.
The winding which takes electrical power from the source, is generally known as primary winding of transformer. Here in our above example it is first winding.



The winding which gives the desired output voltage due to mutual induction in the transformer, is commonly known as secondary winding of transformer. Here in our example it is second winding.



The above mentioned form of transformer is theoretically possible but not practically, because in open air very tiny portion of the flux of the first winding will link with second; so the current that flows through the closed circuit of later, will be so small in amount that it will be difficult to measure.

The rate of change of flux linkage depends upon the amount of linked flux with the second winding. So, it is desired to be linked to almost all flux of primary winding to the secondary winding. This is effectively and efficiently done by placing one low reluctance path common to both of the winding. This low reluctance path is core of transformer, through which maximum number of flux produced by the primary is passed through and linked with the secondary winding. This is the most basic **theory of transformer**.
In short, a transformer carries the operations shown below:

Transfer of electric power from one circuit to another.

Transfer of electric power without any change in frequency.

Transfer with the principle of electromagnetic induction.

The two electrical circuits are linked by mutual induction

2.1.3Main Constructional Parts of Transformer

The three main parts of a transformer are,

1. Primary Winding of Transformer-

Which produces magnetic flux when it is connected to electrical source.

2. Magnetic Core of Transformer-

The magnetic flux produced by the primary winding, that will pass through this low reluctance path linked with secondary winding and create a closed magnetic circuit.

3. Secondary Winding of Transformer-

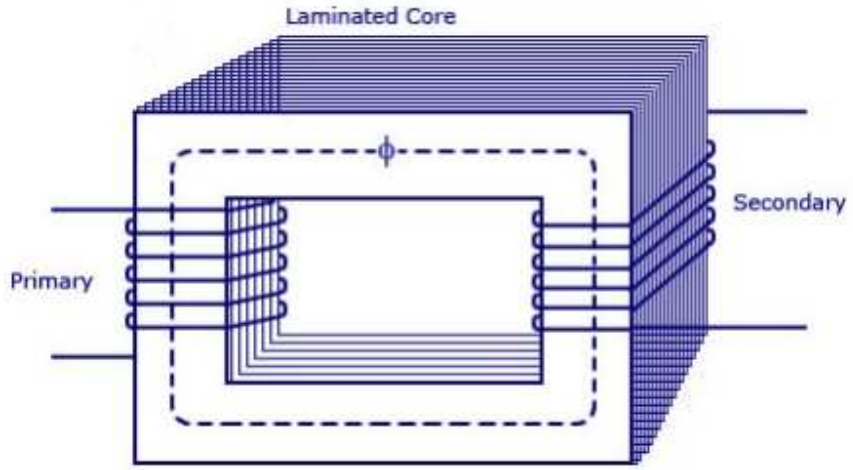
The flux, produced by primary winding, passes through the core, will link with the secondary winding. This winding also wounds on the same core and gives the desired output of the **transformer**

Two coils of wire (called windings) are wound on some type of core material. In some cases the coils of wire are wound on a cylindrical or rectangular cardboard form. In effect, the core material is air and the transformer is called an **AIR-CORE TRANSFORMER**.

Transformers used at low frequencies, such as 60 hertz and 400 hertz, require a core of low-reluctance magnetic material, usually iron. This type of transformer is called an **IRON-CORE TRANSFORMER**. Most power transformers are of the iron-core type.

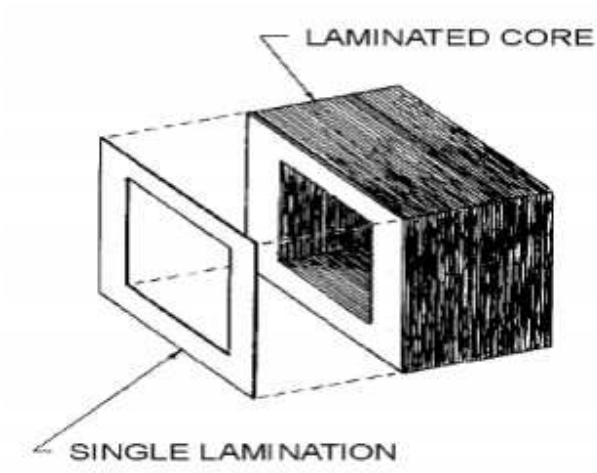
The ENCLOSURE, which protects the above components from dirt, moisture, and Mechanical damage

.



2.1.4Brief description of each part

(i)CORE



There are two main shapes of cores used in laminated-steel-core transformers. One is the HOLLOWCORE, so named because the core is shaped with a hollow square through the center. This shape of core. Notice that the core is made up of many laminations of steel it shows how the transformer windings are wrapped around both sides of the core.

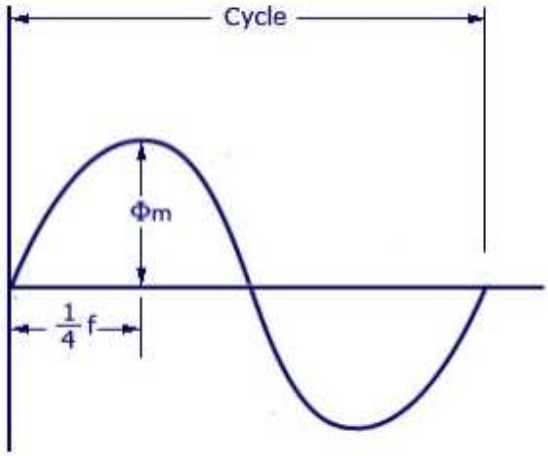
* The core is made up of silicon steel laminated iron core
* The steel cores are varnished and insulated
* Thickness of lamination is from 0.35 to 0.5 MM
* The eddy current loss is minimized by laminated core
* The core is made up of silicon steel so, hysteresis loss is reduced
* Core has different shape E I L
* All the sheets are joined together tightly by bolt
* Small transformer are rectangle in shape.
  big transformers are square in shape

(ii) WINDINGS

As stated above, the transformer consists of two coils called WINDINGS which are wrapped around a core. The transformer operates when a source of ac voltage is connected to one of the windings and a load device is connected to the other. **The winding that is connected to the source is called the PRIMARY WINDING**. **The winding that is connected to the load is called the SECONDARY WINDING**. The primary is wound in layers directly on a rectangular cardboard form.

2.1.5EMF Equation of Transformer:

Let the applied voltage V_1 applied to the primary of a transformer, with secondary open-circuited, be sinusoidal (or sine wave). Then the current I_1, due to applied voltage V_1, will also be a sine wave. The mmf, $N_1 \times I_1$ and core flux Ø will follow the variations of I_1 closely. That is the flux is in time phase with the current I_1 and varies sinusoidally.



Let,

N_1 = Number of turns in primary

N_2= Number of turns in secondary

$Ø_{max}$ = Maximum flux in the core in webers = B_{max} X A f = Frequency of alternating current input in hertz (H_Z)

As shown in figure above, the core flux increases from its zero value to maximum value $Ø_{max}$ in one quarter of the cycle , that is in ¼ frequency second.

Therefore, average rate of change of flux = $\mathbf{Ø_{max}/ ¼ f}$ = 4f $Ø_{max}$Wb/s

Now, rate of change of flux per turn means induced electro motive force in volts. Therefore,

Average electro-motive force induced/turn = 4f $Ø_{max}$volt

If flux Ø varies sinusoidally, then r.m.s value of induced e.m.f is obtained by multiplying the average value with form factor.

Form Factor = r.m.s. value/average value = 1.11
Therefore, r.m.s value of e.m.f/turn = 1.11 X 4f $Ø_{max}$ = 4.44f $Ø_{max}$
Now, r.m.s value of induced e.m.f in the whole of primary winding
= (induced e.m.f./turn) X Number of primary turns
Therefore,

E_1 = 4.44f $N_1Ø_{max}$ = 4.44fN_1B_mA
Similarly, r.m.s value of induced e.m.f in secondary is
E_2 = 4.44f N_2 $Ø_{max}$ = 4.44fN_2B_mA
In an ideal transformer on no load, V_1 = E_1 and V_2 = E_2, where V_2 is the terminal voltage

2.1.6Voltage and current ratio of a transformer

Voltage Transformation Ratio.

The ratio of secondary voltage to primary voltage is known as the voltage transformation ratio and is designated by letter K. i.e.

Voltage transformation ratio, $\mathbf{K = V_2/V_1 = E_2/E_1 = N_2/N_1}$

Current Transformation Ratio.

The ratio of secondary current to primary current is known as current ratio and is reciprocal of voltage transformation ratio in an ideal transformer.
Current transformation ratio, = $\mathbf{I_2/I_1 = N_1/N_2=1/K}$

Transformation Ratio of Transformer

The constant **K is called** transformation ratio of transformer**,**

If $T_2>T_1$, K > 1, then the transformer is step up transformer. If $T_2 < T_1$, K < 1, then the transformer is step down transformer.

.

Turns Ratio of Transformer

As the voltage in primary and secondary of transformer is directly proportional to the number of turns in the respective winding, the transformation ratio of transformer is sometime expressed in ratio of turns and referred as **turns ratio of transformer.**

2.1.7Efficiency

Efficiency of a transformer is defined as ratio of output power to input power
Efficiency=(output power/input power)*100=(output power/(output+losses))*100
Efficiency of the transformer is more than 99%.

2.1.8Losses in a Transformer

1. Copper loss or Variable loss
2. Core losses or iron loss or constant loss

1. Copper Loss in Transformer

Copper loss is I^2R loss, in primary side it is $I_1^2R_1$ and in secondary side it is $I_2^2R_2$ loss, where I_1 and I_2 are primary and secondary current of transformer and R_1 and R_2 are resistances of primary and secondary winding. As the both primary & secondary currents depend upon load of transformer, **copper loss in transformer** vary with load.

2. Core Losses in Transformer

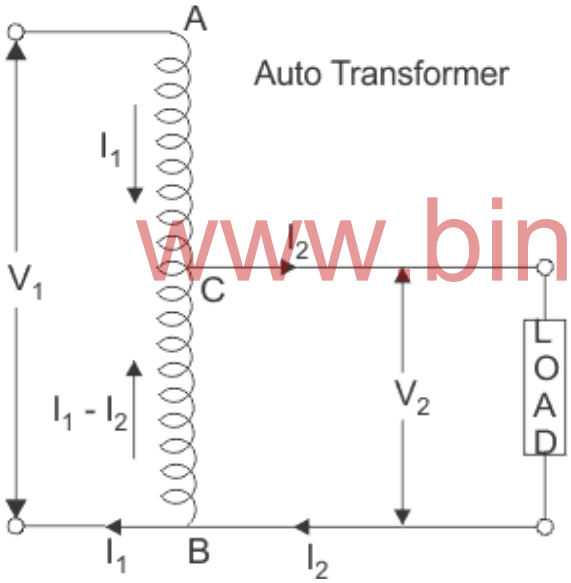
Hysteresis loss and eddy current loss both depend upon magnetic properties of the materials used to construct the core of transformer and its design. So these **losses in transformer** are fixed and do not depend upon the load current. So **core losses in transformer** which is alternatively known as **iron loss in transformer** can be considered as constant for all range of load.
Hysteresis loss in transformer is denoted as, $W_h = K_h f (B_m)^{1.6} \ \ watts$

Eddy current loss in transformer is denoted as , $W_e = K_e f^2 K_f^2 B_m^2 \, watts$
Where **K_h=Hysteresis constant**

2.1.9Auto Transformer

Auto transformer is kind of electrical transformer where primary and secondary shares same common single winding. So basically it's a one winding transformer.

Theory of Auto Transformer



In Auto Transformer, one single winding is used as primary winding as well as secondary winding. But in two windings transformer two different windings are used for primary and secondary purpose. A diagram of auto transformer is shown above. The winding AB of total turns N_1 is considered as primary winding. This winding is tapped from point 'C' and the portion BC is considered as secondary. Let's assume the number of turns in between points 'B' and 'C' is N_2.
If V_1 voltage is applied across the winding i.e. in between 'A' and 'C'.

$$So\ voltage\ per\ turn\ in\ this\ winding\ is\ \frac{V_1}{N_1}$$

Hence, the voltage across the portion BC of the winding, will be,

$$\frac{V_1}{N_1} X N_2 \text{ and from the figure above, this voltage is } V_2$$

$$Hence, \frac{V_1}{N_1} X N_2 = V_2$$

$$\Rightarrow \frac{V_2}{V_1} = \frac{N_2}{N_1} = Constant = K$$

As BC portion of the winding is considered as secondary, it can easily be understood that value of constant 'k' is nothing but turns ratio or voltage ratio of that **auto transformer**.
When load is connected between secondary terminals i.e. between 'B' and 'C', load current I_2 starts flowing. The current in the secondary winding or common winding is the difference of I_2 & I_1.

Auto transformer employs only single winding per phase as against two distinctly separate windings in a conventional transformer.

2.1.10Comparison with two winding Transformers

I).For transformation ratio = 2, the size of the **auto transformer** would be approximately 50% of the corresponding size of two winding transformer. For transformation ratio say 20 however the size would be 95 %. The saving in cost of the material is of course not in the same proportion. The saving of cost is appreciable when the ratio of transformer is low, that is lower than 2. Thus auto transformer is smaller in size and cheaper.
II).An auto transformer has higher efficiency than two winding transformer. This is because of less ohmic loss and core loss due to reduction of transformer material.
III).Auto transformer has better voltage regulation as voltage drop in resistance and reactance of the single winding is less.

Disadvantages of Using Auto Transformer

I).Because of electrical conductivity of the primary and secondary windings the lower voltage circuit is liable to be impressed upon by higher voltage. To avoid breakdown in the lower voltage circuit, it becomes necessary to design the low voltage circuit to withstand higher voltage.
II).The leakage flux between the primary and secondary windings is small and hence the impedance is low. This results into severer short circuit currents under fault conditions.
III).The connections on primary and secondary sides have necessarily needs to be same, except when using interconnected starring connections. This introduces complications due to changing primary and secondary phase angle particularly in the case of delta/delta connection.
IV).Because of common neutral in a star/star connected auto transformer it is not possible to earth neutral of one side only. Both their sides should have their neutrality either earth or isolated.
V).It is more difficult to maintain the electromagnetic balance of the winding when voltage adjustment tapping are provided. It should be known that the provision of tapping on an auto transformer increases considerably the frame size of the transformer. If the range of tapping is very large, the advantages gained in initial cost is lost to a great event.

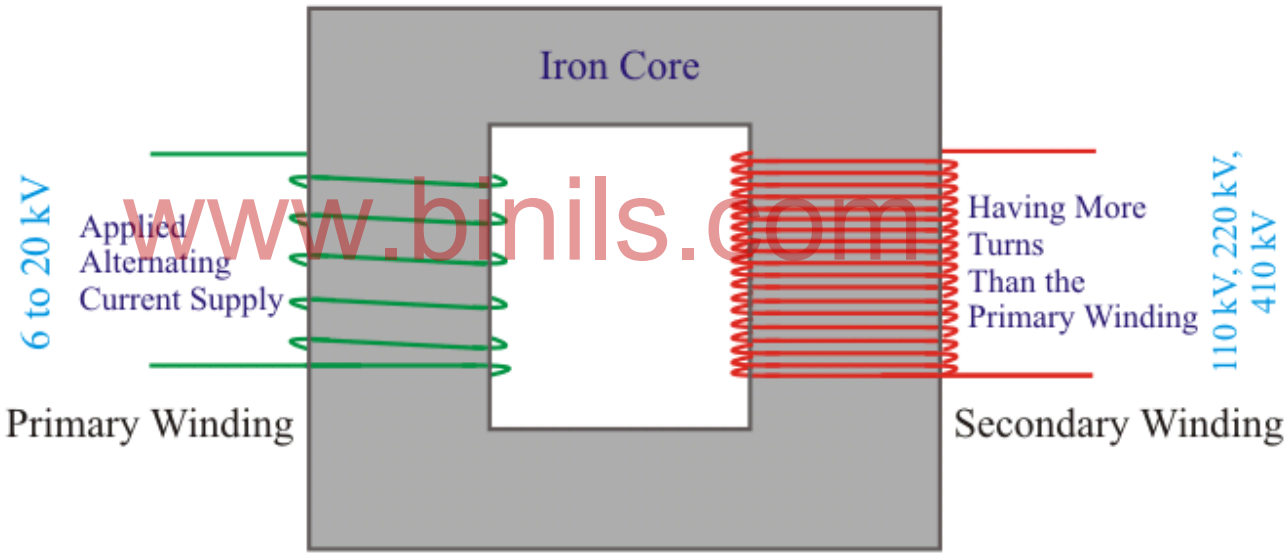
2.1.11Applications of Auto Transformers

1. Compensating voltage drops by boosting supply voltage in distribution systems.
2. Auto transformers with a number of tapping are used for starting induction and synchronous motors.
3. **Auto transformer** is used as variac in laboratory or where continuous variable over broad ranges are required.

2.1.12Step up and step down transformer

With those features, the transformer is the most important part of the electrical system and provides economical and reliable transmission and distribution of electrical energy. The transformer can transfer energy in both directions, from HV to LV side as well as inversely. That is the reason why it can work as voltage step up or step down transformer. Both transformer types have the same design and construction. Any transformer can operate as step-up or step-down type. It is only depending on the energy flows direction.

Step up transformer



Step Up Transformer

The primary side of a **step-up transformer** has a small number of turns (LV side) while the transformer secondary side has many number of turns (HV side). That means an energy flows from the LV to HV side.
. Those transformers usually have large turns ratio value.

Applications of step up transformer

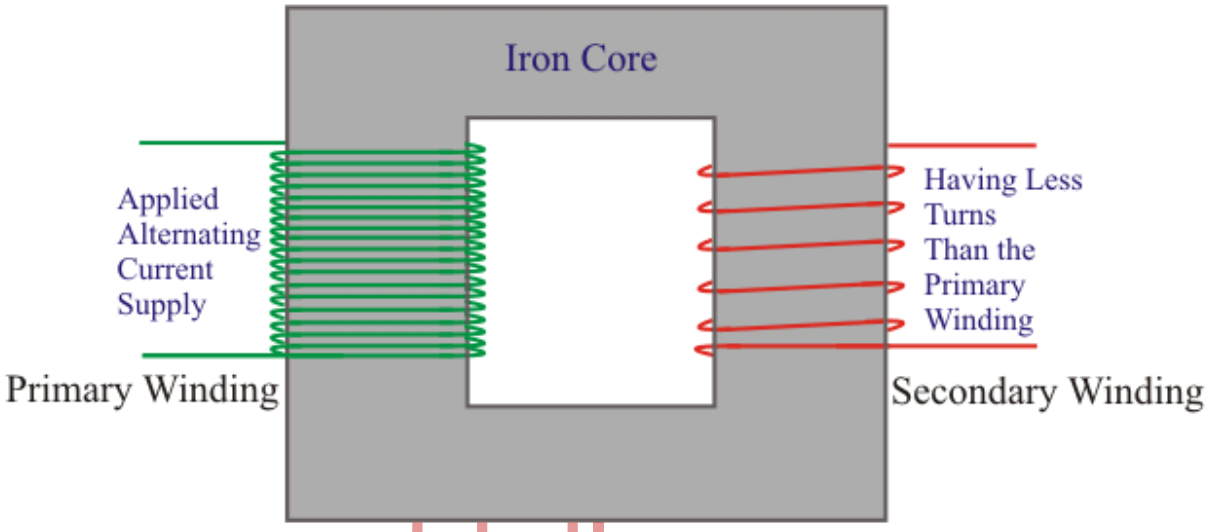
The small **step-up transformers** can be used in electronic and electrical devices where the voltage boosting is required. But nowadays in the modern electronic device, power electronic circuits are more frequently used because of weight and dimension.

Step down transformer

The primary side of a **step-down transformer** has a many number of turns (HV side) while the transformer secondary side has small number of turns (LV side). That means an energy flows from the HV to LV side.

Those transformers usually have low turns ratio value.

.



Applications of step down transformer

The step-down transformers have a very important function in power system. They lower the voltage level and adapt it for energy consumers.

Note:

if $T_2 > T_1$, K > 1, then the transformer is step up transformer.

If $T_2 < T_1$, K < 1, then the transformer is step down transformer.

2.2SPECIAL MOTOR

2.2.1 Stepper Motor

Definition:

It is a brushless electromechanical device which converts the train of electric pulses applied at their excitation windings into precisely defined step-by-step mechanical shaft rotation. The shaft of the motor rotates through a fixed angle for each discrete pulse. This rotation can be linear or angular. It gets one step movement for a single pulse input.

When a train of pulses is applied, it gets turned through a certain angle. The angle through which the stepper motor shaft turns for each pulse is referred as the step angle, which is generally expressed in degrees.

2.2.2 Working Principle of operation

Stepper motor is a specially designed DC motor that can be driven by giving excitation pulses to the phase windings. They cannot be driven by just connecting the positive and negative leads of the power supply.

They are driven by a stepping sequence which is generated by a controller. The motor moves in steps according to this sequence. This post will discuss the basic theory behind the stepper motors.

Printers are a great source for stepper motors. Old dot matrix printers have a big and a small stepper motor.

2.2.3Types and applications

Basic Classification of Stepper Motors

Based on the type of the construction, stepper motors can be classified as

1. Variable Reluctance (VR) stepper motor

2. Permanent Magnet (PM) stepper motor

3. Hybrid stepper motor

VARIABLE RELUCTANCE (VR) STEPPER MOTOR

The Variable Reluctance stepper motors are those which have a rotor made of ferromagnetic substances. Hence when the stator is excited it becomes an electromagnet and the rotor feels a pull in that direction. The ferromagnetic substance always tries to align itself in the minimum reluctance path.

By exciting the coils, a magnetic field is produced and air gap reluctance is varied. Hence it is called a variable reluctance stepper motor. In this motor, the direction of the motor is independent of the direction of the current flow in the windings.

PERMANENT MAGNET (PM) STEPPER MOTOR

Here the rotor is permanently magnetized. Hence, the movement of the motor is due to the attraction and repulsion between the stator and rotor magnetic poles.

In this motor, the direction of the motor is directly dependent on the direction of the current flow in the windings as the magnetic poles are reversed my changing the direction of the current flowing through the rotor.

HYBRID STEPPER MOTOR

The hybrid stepper motor, as the name suggest is a motor designed to provide better efficiency by combining the pros of both the permanent magnet stepper motor and variable reluctance stepper motor.

The VR and PM stepper motors are the most common type of stepper motors. The only difference is that, in the variable reluctance stepper motor, the rotor is made of a ferromagnetic substance and in the case of permanent magnet stepper motor, the rotor is permanently magnetized.

Applications:

1. **Industrial Machines** – Stepper motors are used in automotive gauges and machine tooling automated production equipments.
2. **Security** – new surveillance products for the security industry.
3. **Medical** – Stepper motors are used inside medical scanners, samplers, and also found inside digital dental photography, fluid pumps, respirators and blood analysis machinery.
4. **Consumer Electronics** – Stepper motors in cameras for automatic digital camera focus and zoom functions.

And also have business machines applications, computer peripherals applications.

2.2.4SERVO MOTOR

Definition

Servo motor works on PWM (Pulse width modulation) **principle** means its angle of rotation is controlled by the duration of applied pulse to its Control PIN. Basically **servo motor** is made up of DC**motor** which is controlled by a variable resistor (potentiometer) and some gears.

2.2.5Working principle of Servo Motors

A servo consists of a Motor (DC or AC), a potentiometer, gear assembly and a controlling circuit. First of all we use gear assembly to reduce RPM and to increase torque of motor. Say at initial position of servo motor shaft, the position of the potentiometer knob is such that there is no electrical signal generated at the output port of the potentiometer. Now an electrical signal is given to another input terminal of the error detector amplifier. Now difference between these two signals, one comes from potentiometer and another comes from other source, will be processed in feedback mechanism and output will be provided in term of error signal. This error signal acts as the input for motor and motor starts rotating. Now motor shaft is connected with potentiometer and as motor rotates so the potentiometer and it will generate a signal.

So as the potentiometer's angular position changes, its output feedback signal changes. After sometime the position of potentiometer reaches at a position that the output of potentiometer is same as external signal provided. At this condition, there will be no output signal from the amplifier to the motor input as there is no difference between external applied signal and the signal generated at potentiometer, and in this situation motor stops rotating.

2.2.6Types of Servo Motor and applications

Servo motors are classified into different types based on their application, such as

1. AC servo motor,
2. DC servo motor,
3. Brushless DC servo motor,
4. Positional rotation,
5. Continuous rotation and
6. Linear servo motor etc.

Typical servo motors comprise of three wires namely, power control and ground. The shape and size of these motors depend on their applications. RC servo motor is the most common type of servo motor used in hobby applications, robotics due to their simplicity, affordability and reliability of control by microprocessors.

Applications of Servo Motor

Servo motors are small and efficient but critical for use in applications requiring precise position control. The servo motor is controlled by a signal (data) better known as a pulse-width modulator (PWM). Here are several of the more common servo motor applications in use today.

- Robotics
- Conveyor Belt.
- Camera Auto Focus
- Robotic Vehicle
- Metal Cutting & Metal Forming Machines:
- Servo motors provide precise motion control for milling machines,
- Lathes machines

. **2.2.7FACTORS TO BE CONSIDERD FOR SELECTING A MOTOR A PARTICULAR APPLICATION**

A motor must do three things:

1. Start the equipment load
2. Drive the load once it is started
3. Survive the abuse of the surroundings in which it operates

STARTING LOAD

Motor selected must produce adequate starting torque to start the load

Commonly–used motors:

Split phase

Capacitor start-induction runs

Capacitor start-capacitor runs

Repulsion start-induction runs

Series or universal

Shaded pole

Three-phase

Capacitor start-induction run & Three-phase are the most common and produce highest starting torque

2.3Electrical safety

2.3.1ELECTRICAL SHOCK

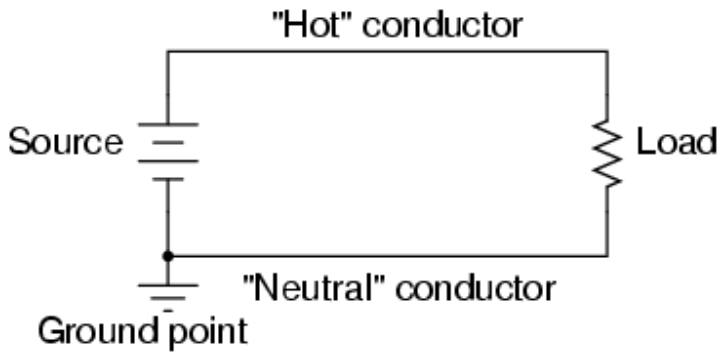
An electrical shock is received when electrical current passes through the body.

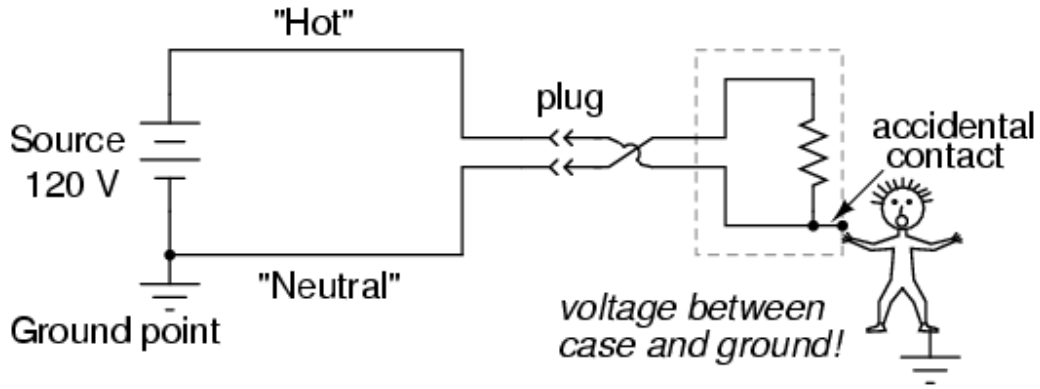
You will get an electrical shock if a part of your body completes an electrical circuit by…

Touching a live wire and an electrical ground, or

Touching a live wire and another wire at a different voltage.

. In a simple two-wire electrical power system, the conductor connected to ground is called the *neutral*, and the other conductor is called the *hot*, also known as the *live* or the *active*:





2.3.2Need for Earthling.

- To protect human lives as well as provide safety to electrical devices and appliances from leakage current.
- To keep voltage as constant in the healthy phase (If fault occurs on any one phase).
- To Protect Electric system and buildings form lighting.
- To serve as a return conductor in electric traction system and communication.
- To avoid the risk of fire in electrical installation systems.

Different Terms used in Electrical Earthling

Earth: The proper connection between electrical installation systems via conductor to the buried plate in the earth is known as Earth.

Earthed: When an electrical device, appliance or wiring system connected to the earth through earth electrode, it is known as earthed device or simple “Earthed”.

Solidly Earthed: When an electric device, appliance or electrical installation is connected to the earth electrode without a fuse, circuit breaker or resistance/Impedance, It is called “solidly earthed”.

Earth Electrode: When a conductor (or conductive plate) buried in the earth for electrical earthing system. It is known to be Earth Electrode. Earth electrodes are in different shapes like, conductive plate, conductive rod, metal water pipe or any other conductor with low resistance.

Earthing Lead: The conductor wire or conductive strip connected between Earth electrode and Electrical installation system and devices in called Earthing lead.

Earth Continuity Conductor: The conductor wire, which is connected among different electrical devices and appliances like, distribution board, different plugs and appliances etc. in other words, the wire between earthing lead and electrical device or appliance is called earth continuity conductor. It may be in the shape of metal pipe (fully or partial), or cable metallic sheath or flexible wire.

Sub Main Earthing Conductor: A wire connected between switch board and distribution board i.e. that conductor is related to sub main circuits.

Earth Resistance: This is the total resistance between earth electrode and earth in Ω (Ohms). Earth resistance is the algebraic sum of the resistances of earth continuity conductor, earthing lead, earth electrode and earth.

2.3.3Types of Earthing

1. Plate Earthing

2. Pipe Earthing

3. Rod Earthing

4. Earthing through the waterman

5. Strip or wire Earthing

2.3.4 ELECTRICAL FUSE

Definition

An electric fuse is a device that is used to protect electric circuits and electric appliances against high current caused by short - circuiting or overloading due to withdrawal of large current. A fuse is a short piece of wire made of a material of high resistance and low melting point.

Need for fuse

Electric fuse is a protective device which protects electrical equipment in the circuit by breaking the circuit when there is a short circuit.

It contains a fuse wire which has low resistance, it allows normal current pass through it safely but if there is any short circuit, fuse will blow out i.e. fuse wire cant withstand the heat produced by that current (infinite current) so it melts and breaks the circuit. Thus, protecting other electrical devices from short circuit current.

The fuse wire is made of zinc, copper, silver, aluminum, or alloys to provide stable and predictable characteristics. Fuse should be of low resistance and low melting point as per the requirement current rating for over current protection.

2.3.5TYPES OF FUSE

Fuses can be divided into two main categories according to the type of input supply voltage.

1. AC fuses
2. DC fuses

There is a little difference between AC and DC Fuses used in the AC and DC Systems.

1. One time use only Fuse

Such types of fuses can be categories on the following basis.

i) Current carrying Capacity of Fuse
ii) Breaking capacity
iii) I2t value of Fuse
IV) Response Characteristic
V) Rated voltage of Fuse
VI) Packaging Size

2) Resettable Fuses

3) CARTRIDGE FUSES

i) General purpose fuse

ii) Heavy-duty cartridge fuses

SEMICONDUCTOR DEVICES

Objectives:

At the end of this unit, students can

- Define diode and be familiar with its applications.
- Define special purpose diodes such as Zener diode, Photo diode and LED
- State the applications of Zener diode
- Define Light Dependent Resistor
- Define rectifiers, know about the types of rectifiers
- State the uses of different types of filters
- Define Transistor and its working principle
- Explain the input and output characteristics of a transistor
- Differentiate among different configurations of transistors

3.0 Introduction

Diode and Transistor play a major role in the extensive technological growth that has led to the invention of less weight electronics gadgets like laptops, tablets and mobile phones etc., Semiconductors whose resistivity lies between conductors and insulators are used in the invention of semiconductor devices called diodes and transistors. Transistors replaced bulky vacuum tubes and reduced the size of all electronic equipments.

Basic terminologies:

Semiconductor:

Silicon and Germanium are the two semiconductor materials widely used in electronic industry. At low temperature they act as insulators and application of voltage across its ends does not produce any current flow. Whereas at room temperature few free electrons will be present in the semiconductor materials. Rise in temperature increases the number of free electrons which in turn reduces the resistance. Hence, semiconductor materials act like conductors at high temperature.

Types of semiconductors

There are two types of semiconductors namely (i) Intrinsic semiconductor and (ii) extrinsic semiconductor.

Intrinsic semiconductor :

Semiconductor in its extremely pure form has equal number of electron-hole pair at room temperature. When a potential difference is applied across the ends, electrons move towards

positive terminal and holes move towards negative terminal within the semiconductor. In the external circuit current flow is due to electrons only.

Extrinsic semiconductor:

Extrinsic semiconductors are produced by the process called doping. Doping is the process of adding impurity atoms to intrinsic semiconductors to obtain new elements called p-type and n-type semiconductors.

Addition of pentavalent impurity atoms (ex. Arsenic and Antimony) to a semiconductor produces n-type semiconductor. This process gives rise to more number of free electrons. Hence majority current carriers in n-type semiconductor are electrons.

Addition of trivalent impurity atoms (ex. Gallium and Indium) to a semiconductor produces p-type semiconductor. This process gives rise to more number of free holes. Hence, majority current carriers in p-type semiconductor are due to holes.

3.1 Diodes

3.1.1 PN Junction

PN junction is formed by suitably joining P type and N type semiconductor materials together.

Depletion Region and Barrier Potential

Depletion region is formed at the PN junction, due to diffusion. Diffusion is the movement of majority carriers of holes from P to N type semiconductor and electrons from N to P type semiconductor. Because of this, positive charge region is formed in N type semiconductor and negative charge region is formed in P type semiconductor at the junction. This is called 'depletion region'. The potential across the depletion region is called 'barrier potential'. This barrier potential stops further movement of the majority charge carriers from either side. The barrier potential is 0.3 V for germanium semiconductor diode and 0.7 V for silicon semiconductor diode.

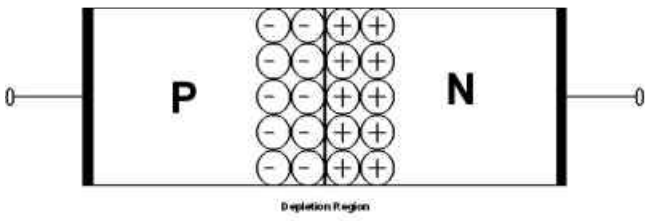


Fig 3.2 PN Junction Diode

The depletion region causes movement of minority carriers also, thereby holes from N type semiconductor move into P type semiconductor and electrons from P type semiconductor move into N type semiconductor. This movement is called drift. The current due to drift is called drift current.

The diffusion and drift currents are opposed to one another, therefore no charge carriers flow through the junction at normal condition. This condition is called equilibrium.

PN Junction diode

A PN Junction diode is a semi conductor device, which allows the flow of current in one direction only. Basically it is formed by joining P-type and N-type semiconductor materials, attached with two terminals called nodes. The positive node is called anode, denoted by the letter A and the negative node is called cathode, denoted by the letter K. The symbol of a diode is shown in Fig 3.1 below. The current flows only from anode to cathode.

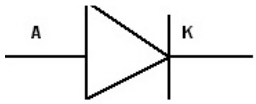


Fig 3.1 Symbol of Diode

Forward Biased Junction

> When an external d.c voltage is applied to the PN junction in such a way that reduces depletion region and causes current to flow, then the diode is said to be forward biased.

The diode is forward biased by connecting anode to the positive terminal and cathode to the negative terminal of the battery. The forward biasing causes holes in P type region and electrons in N type region to move towards the depletion region. This reduces the width of the depletion region and decreases the barrier voltage. Initially no current will flow through the diode. Further increase in the applied voltage, breaks the barrier potential which is 0.3V for germanium and 0.7V for silicon. The voltage which breaks the barrier potential is called cut-in voltage. Due to this breaking, more number of majority charge carriers flow through the junction. Hence, current starts flowing.

After cut-in voltage, further increase in the applied voltage, gives sharp rise in the flow of current though the diode. The current will be in the order of mA (milli ampere). Thus the diode allows the current to flow through after cut-in voltage in the forward bias.

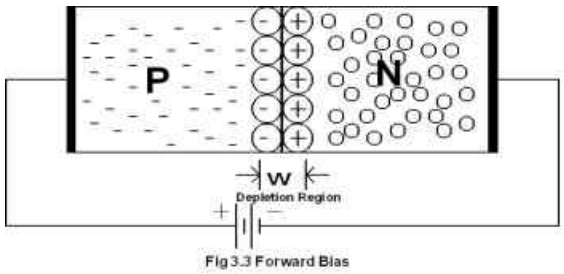
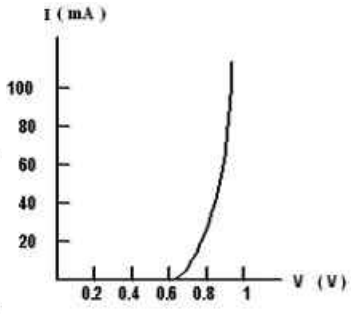


Fig 3.3 Forward Bias



3.4 Forward bias Characteristic

Reverse Biased Junction

The diode is reverse biased, by connecting anode to the negative terminal and cathode to the positive terminal of the battery.

The reverse biasing attracts the holes in P type region and electrons in N type region towards the battery. Thus majority carriers move away from the junction. This increases the width of the depletion region and increases the barrier voltage. Hence, no current will flow through the diode. Increase in the applied voltage does not have any effect on the current flow.

But, due to minority charge carriers a small negligible current flows through it which is about micro ampere. Further increase in the applied voltage breaks the barrier potential, hence large current starts flowing. This voltage is called reverse break down voltage. This reverse break down voltage destroys the diode which makes the diode unfit for further use.

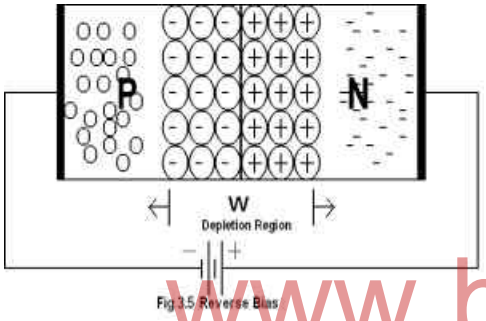
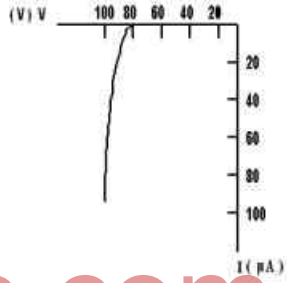


Fig 3.5 Reverse Bias



3.6 Reverse bias Characteristic

3.1.2 Applications of PN Junction Diodes

Rectifier*: PN junction diodes are used in rectifiers for converting AC into DC.*

Split Power Supply: Often electronic circuits require negative as well as positive power supply voltages. This is done by reversing the direction of the diode and capacitor in the power supply circuit.

Voltage Multiplier: *The circuit which gives two or more peak voltages is called voltage multiplier. Diodes are used in voltage multiplier circuits.*

Voltage Clamping*: In order to prevent power supply from going negative, clamper circuits are designed that does not allow the current to go below the reference level.*

Voltage Clipping: *A diode can be used to clip the part of the voltage above the reference voltage. This type of circuits are called clipping circuits.*

Diode Gate: *Diodes are used to pass the higher of two voltages without affecting the lower voltage.*

Protecting surges: *An important use of diodes is to suppress the surge voltage, when the load decreases to protect the circuits.*

3.2 Zener Diode

Zener diode is a heavily doped special purpose PN junction diode, which maintains a constant voltage in the reverse biased condition. It is named after the inventor C. Zener. Its working is same as ordinary PN junction diode when it is forward biased but different in the reverse biased condition.

Zener diode is made by heavily doped P or N type semiconductors. Because of this, the width of the depletion region is very thin. The symbol and its equivalent circuits are shown in below.

Fig 3.7 Symbol of Zener Diode

3.2.1 Working of Zener diode

Under forward biased condition, zener diode behaves like ordinary PN junction diode. Initially no current flows, after the cut-in voltage, a sudden rise in the current flow occurs. Current flow in forward biased condition is due to majority current carriers present in the P and N type materials.

Under reverse biased condition, a very small current flows due to minority current carriers present in the P and N type material. Magnitude of the current depends on the level of doping. As the reverse voltage is increased, at certain critical voltage called ‘breakdown voltage’ (also called ‘zener breakdown voltage’) sudden rise in the reverse current occurs. Further increase in applied reverse voltage, increases the current. But the voltage across the zener diode remains constant.

The breakdown or zener breakdown voltage depends on level of doping. If the diode is heavily doped the depletion layer is thin hence breakdown occurs at low reverse voltage. Lightly doped diode has higher breakdown voltage. It is clearly shown in the equivalent circuit of zener diode that in the breakdown region the zener can be replaced by a battery as the voltage across the zener is constant in this region.

In zener diode two types of breakdown occurs

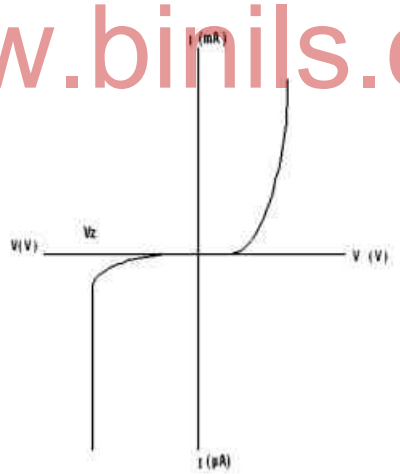
1. Zener breakdown
2. Avalanche breakdown

Zener Breakdown

When the zener diode is reverse biased due to electrostatic attraction minority current carries (ie., electrons from P and holes from N type semiconductor) drift towards the junction causing small current to flow. While moving towards the junction the minority carriers collide with electrons in the vicinity of their path. This collision causes the electrons to come out from their orbit and become free and move towards the junction. These free electrons accelerate the current flow. This increase in current is due to zener breakdown. Normally zener break down occurs below 5.5V.

Avalanche breakdown

The free electrons gain acceleration due to increase in applied reverse voltage, they collide with other atoms and knock off more electrons. These electrons then in turn accelerate and subsequently collide with other atoms. Each collision produces more electrons which lead to more collisions. Production of more no of free electrons due to such collision is called avalanche breakdown. Due to this, the current in the zener increases.



3.8 forward and reverse characteristic of Zener diode

3.2.3 Applications of Zener diode

i. It is used as voltage regulator

ii. It is used in protecting meters

iii. It is used as limiter in wave shaping circuits.

Zener diode as a voltage regulator

When the ac input voltage of rectifier fluctuates, its rectified output also fluctuates. Zener diode is added to get constant dc voltage from rectifier. The circuit diagram is shown in below.

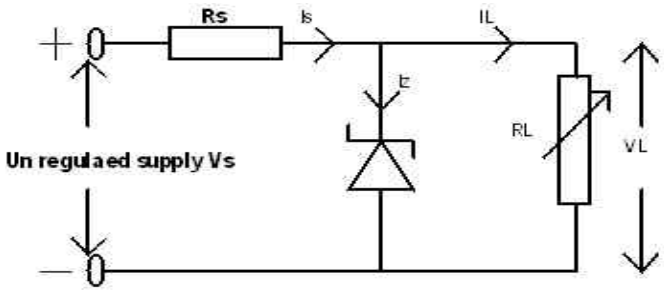


Fig 3.9 Voltage Regulator

The filtered output of the rectifier is connected to the Zener diode through a series resistor R_s. The load resistance R_L is connected in parallel with Zener diode. The zener diode is reverse biased, so that it maintains constant voltage at the output. When the input voltage increases, the excess voltage drops across the zener diode i.e., the current through it increases but voltage remains constant. A decrease in the input voltage decreases the current through the diode, but voltage remains constant. Thus increase or decrease in the applied voltage does not affect the output voltage.

Similarly when the load increases the load current also increases. The additional current is supplied by the zener diode. When the load decreases, the current through zener diode increases and load current decreases, thus maintains the output voltage constant.

Zener diode for meter protection

To protect the meter (Eg. Multimeter) from over current, zener diode is connected in parallel with multimeter. In case of any accidental overload, most of the current will pass through the zener diode, thus protecting the meter from damage.

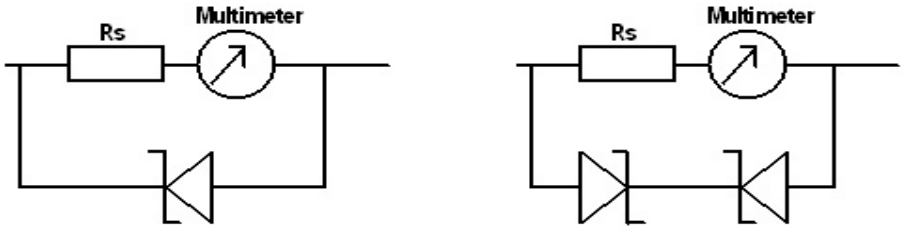


Fig 3.10 (a) for protecting DC meters (b) for protecting AC meters

Zener diode as wave shaper

To convert sine wave into square wave or clip the peak voltage of sine wave, zener diode is connected as shown in the figure.

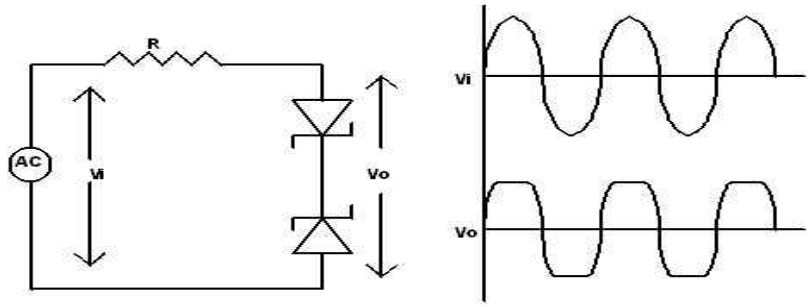
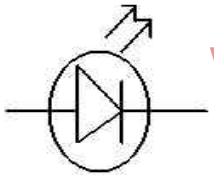


Fig 3.11 - Wave Shaper

When the input voltage is below the zener breakdown voltage, it gives high resistance path and input voltage appears across the output terminals. When input voltage is above the zener breakdown voltage, the diodes offer low resistance path, hence most of the current pass through it and only limited current is available across the output terminals.

3.3 Light Emitting Diode (LED)

Light Emitting Diode is a heavily doped optoelectronic diode, which emits visible light or invisible light when it is forward biased. The visible lights are usually red, yellow, green, blue and white. The invisible light includes the infrared light, ultraviolet. This diode is made up of semi conductors of compounds of Gallium. The symbol is as shown in below:



3.12 LED Symbol

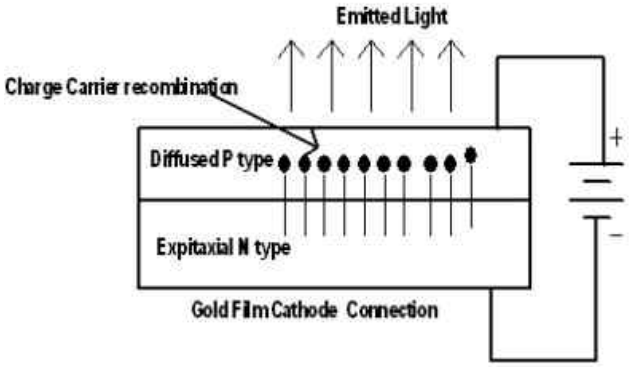


Fig 3.12 a Ciircuit Diagram of LED

Construction

One of the methods used to construct LED is to deposit three semiconductor layers on the substrate. The three semiconductor layers deposited on the substrate are n-type

semiconductor, p-type semiconductor and active region. Active region is present in between the n-type and p-type semiconductor layers.

Working Principle

Under forward biased condition, the free electrons from N type semiconductor recombine with holes in the P type semiconductors. These free electrons usually have more energy than holes. At the time of recombining, excess energy of electrons are emitted in the form of light or photons. In ordinary PN junction diodes which is made up of silicon or germanium, these excess energy is emitted in the form of heat. But, LEDs are made of compounds of Gallium. These compounds emit excess energy as light. In LED, most of the charge carriers recombine at active region. Therefore, most of the light is emitted by the active region. The active region is also called as depletion region.

When the forward current of the diode is small, the intensity of light emitted is low. As the forward current increases, intensity of light increases and reaches a maximum. Further increase in the forward current causes decrease in light intensity. LEDs are biased such that the light emitting efficiency is maximum.

The safe forward voltage rating of most of the LEDs is from 1V to 2V and forward current rating is from 200mA to100mA. When the forward voltage exceeds 2V, the LED may get damaged.

Characteristics

The forward and reverse characteristics are same as an ordinary PN Junction diode. But, its output characteristics is drawn between input forward current in milli ampere and output light in milli Watts. The amount of output light emitted by the LED is directly proportional to the amount of forward current flowing through the LED. More the forward current, greater is the emitted light intensity. The graph of forward current vs. output light is shown in the figure.

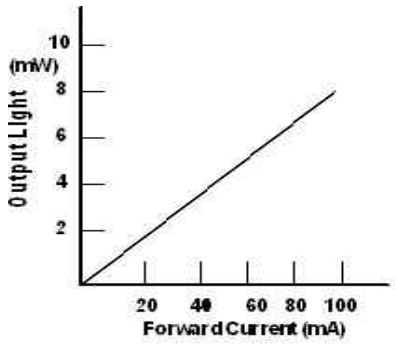


Fig 3.13 Output of LED

Compounds of LED and their corresponding Color

Compounds of LED	*Emitting Light Color*

Gallium arsenide	red and infrared
Gallium nitride	bright blue
Yttrium aluminum garnet	White
Gallium phosphide	red, yellow and green
Aluminum gallium nitride	ultraviolet light
Aluminum gallium phosphide	green light

Advantages of LED

1. It requires very low voltage of 1 to 2 V and current of 5 to 10 mA to operate
2. Output power will be 150 milli watts hence less heat.
3. The response time is very less only about 10 nanoseconds.
4. The device does not need any heating and warm up time.
5. Miniature in size and hence light weight. Have a rugged construction and hence can withstand shock and vibrations.
6. An LED has a life span of more than 20 years.

Disadvantages

1. A slight excess in voltage or current can damage the device.
2. The device is known to have a much wider bandwidth compared to the laser.
3. The temperature depends on the radiant output power and wavelength.

Applications of LED

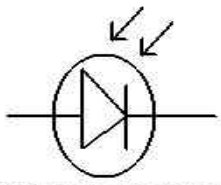
Few applications of LEDs are as follows

1. Burglar alarm systems
2. Calculators
3. Picture phones
4. Traffic signals
5. Multimeters
6. Digital watches
7. Automotive heat lamps
8. Camera flashes
9. Aviation lighting

3.4 Photo Diode

A photodiode is a p-n junction or pin semiconductor device that converts light energy to generate electric current. When light is allowed to fall on the active region of diode, current is produced in it. It is also sometimes referred as photo-detector, photo-sensor, or light detector.

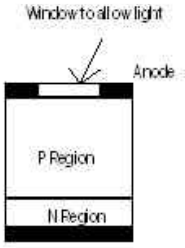
Photodiodes are specially designed to operate in reverse bias condition. The symbol of photodiode is similar to the normal p-n junction diode except that it contains arrows striking the diode. The arrows striking the diode represent light or photons.



3.14 Photodiode Symbol

Construction

Photodiode is constructed in structures 1. PN junction diode type 2. PIN (p-type, intrinsic and n-type) type. The second type is mostly used as it has fast response time. Silicon germanium and gallium arsenide can be used in the construction. The junction through which light enters the semiconductor must be thin enough to pass most of it. Intrinsic semiconductors are the pure form of semiconductors. In intrinsic semiconductor, the number of free electrons in the conduction band is equal to the number of holes in the valence band.



3.15 construction of Photodiode

Working of Photodiode

The photodiode is connected to the external power supply in the reverse biased condition. On applying reverse bias, change in the current with the change in the light intensity is shown clearly in the graph below.

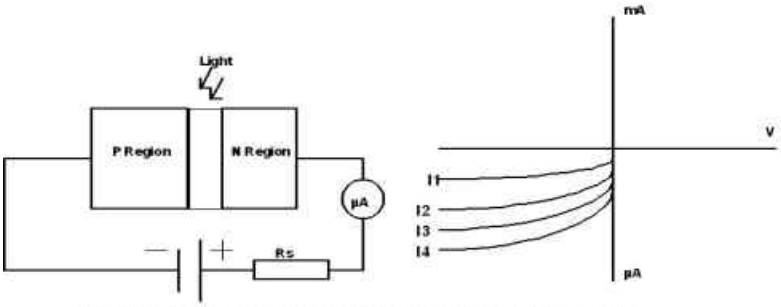


Fig. 3.16 Working and Reverse bias characteristic of Photodiode

Applications of Photodiode

The various applications of photodiodes are

1. Compact disc players
2. Smoke detectors
3. Space applications
4. Photodiodes are used in medical applications such as computed tomography instruments to analyze samples, and pulse oximeters.
5. Photodiodes are used for optical communications.
6. Photodiodes are used to measure extremely low light intensities.

3.5 Light Dependent Resistor

A light dependent resistor, LDR is a resistor whose resistance increases or decreases depending on the amount of light intensity that fall on it. LDR is a very useful tool in a light/dark circuits. The other names are photo resistor, photoconductor or photocell.

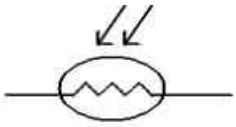


Fig 3.17 Symbol of Photoresistor

Construction

The light sensitive material is deposited on an insulating substrate such as ceramic. The material is deposited in zigzag pattern in order to obtain the desired resistance and power rating. This zigzag area separates the metal deposited areas into two regions, then the ohmic contacts are made on either sides of the area. The resistances of these contacts should be less. Materials normally used are cadmium sulphide, cadmium selenide, indium antimonite and cadmium sulphonide.

Working Principle

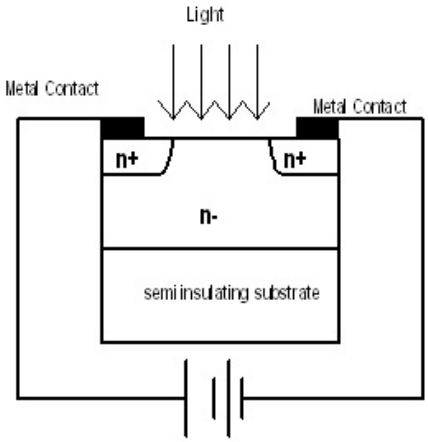


Fig 3.17a Construction of LDR

LDR are made up of many semi-conductor materials with high resistance. There are very few electrons that are free and are unable to move. When light falls on the semi conductor material it absorbs the light and the energy is transferred to the electrons, which allow them to break from valence band to conduction band. These free electrons again collide with other electrons and produce more free electrons. Presence of free electrons increases conductivity and resistance of the diode decreases. When no light falls on it, there are no free electrons available. Hence its conductivity is less and resistance becomes high.

Applications of LDR

1. They are used in light sensors to detect absence or presence of light like in a camera light meter.
2. They are used in street lamps to turn-on and turn-off the light.
3. They are used in alarm clock to detect unwanted incidents
4. They are used in conveyor belt for counting the packages moving on it.

3.6 Rectifiers

The electronic circuit used to convert alternating current into direct current is called rectifier. PN junction diodes are used in rectifiers, due to their unidirectional current conducting property.

Need for Rectifiers

Most of the electronic devices and circuits need DC power. But, power is generated in the form of AC. Hence, it is essential to convert Alternating Current into Direct Current. Since, diode conducts current in only one direction, they are used as Rectifiers.

Types of Rectifiers

The different types of rectifiers are

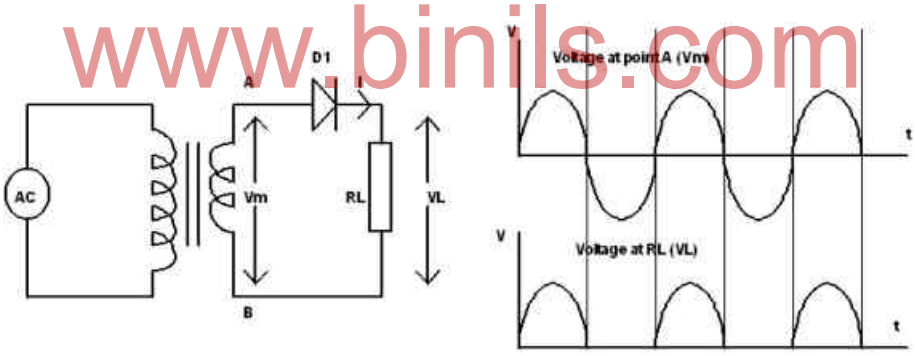
a. Half wave rectifier

b. Full wave rectifier

c. Bridge rectifier

3.6.1 Half Wave Rectifier

Half wave rectifier converts half of the ac input voltage into pulsating dc output voltage. In this circuit a step down transformer and a single PN junction diode are used. Since, the diode conducts only when it is forward biased, it allows current to flow during positive half cycle through the load. During negative half cycle as the diode is reverse biased no current flows through the circuit.



3.18 Half Wave Rectifier and its output

Operation

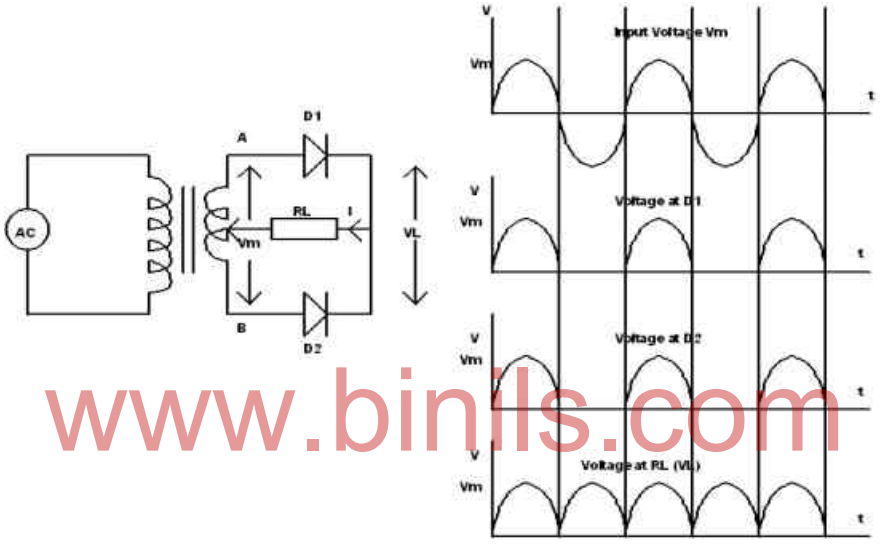
During positive half cycle of the input voltage, terminal point A is positive and B is negative. Since the diode D is forward biased, it conducts. Hence, output voltage is obtained across the Load Resistor R_L as same as the input voltage. In the waveform shown above to observe during positive half cycle, when the input voltage is rising, the output voltage is also raising and when input voltage is falling, the output voltage is also falling. Thus the positive half cycle of the input AC voltage is available across R_L.

During negative half cycle of the input voltage, terminal point A is negative and B is positive. Now the diode D is reverse biased, it does not conduct current. Hence, no output voltage is available across the Load Resistor R_L. Thus the negative half of the input AC voltage is not

available across R_L. The voltage across the Load Resistor is zero. As it converts only half of the input power, its efficiency is below 50%.

3.6.2 Full Wave Rectifier

Full wave rectifier converts full cycle of the ac input voltage into pulsating dc output voltage i.e. it converts both positive and negative half cycles of input voltage into pulsating dc output voltage. It uses a centre tapped transformer with two PN junction diodes. The centre tapped transformer produces two equal voltage at the opposite terminals A and B. The center point O is earthed. The diodes D_1 and D_2 are connected in such way that when D_1 is forward biased, D_2 is reverse biased and vice versa.



3.19 Full Wave Rectifier and its output

Operation

During positive half cycle of the input voltage, the terminal point A is positive and B is negative. The diode D_1 is forward biased and D_2 is reverser biased. The positive half of the input voltage is obtained across the Load Resistor R_L as the current flows from A, D_1, R_L ,O and A. And no current flows through D_2.

During negative half cycle of the input voltage, the terminal point A is negative and B is positive. The diode D_2 is forward biased and D_1 is reverse biased. The negative half of the input voltage is obtained across the Load Resistor R_L as the current flows from B, D_2, $R_{L.}$, O and B. No current flows through D_1.

During both positive and negative half cycles of the input voltage, the current flows through RL in the same direction. Hence, the output current is in only one direction. i.e.DC.

3.5.3 Bridge Rectifiers

Bridge rectifier converts full cycle of the input AC voltage into pulsating DC voltage. It contains a step down transformer and four diodes. The four diodes and Load Resistor are connected in the form of bridge, hence, it is called bridge rectifier. It is used to increase the Transformer Utilization Factor of the full wave rectifier.

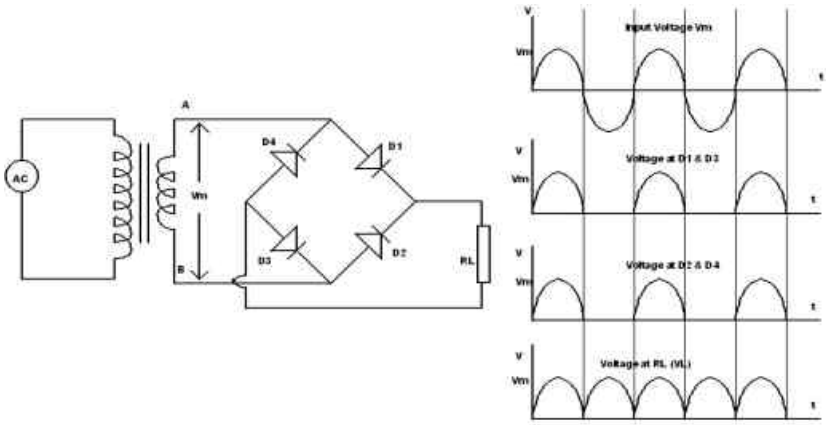


Fig 3.20 Bridge Rectifier and its output

Operation

During positive half cycle of the input ac voltage, the terminal point A is positive and B is negative. The diodes D_1 & D_3 are forward biased and D_2 & D_4 are reverse biased. Now the output current flows through A, D_1, R_L, D_3

, B, A. Now, the output voltage is obtained across R_L.

During negative half cycle of the input ac voltage, the terminal point A is negative and B is positive. The diodes D_2 & D_4 are forward biased and D_1 & D_3 are reverse biased. Now the output current flows through B,D_2,R_L,D_4, A, B. Now, the output voltage is obtained across R_L.

During both positive and negative half cycles of the input voltage, the current flows through R_L in the same direction. Hence, the output current is in only one direction. i.e. DC.

Comparison of Rectifiers

The rectifiers are compared based on the following characteristics:

a. Rectifier Efficiency (η)

Rectifier efficiency is the ratio of the output DC power to the input AC power supplied to the circuit.

$$\eta = \frac{Output\ PowerDC}{Input\ Power\ AC} \text{ X } 100$$

b. Transformer Utilization Factor (TUF)

Transformer Utilization Factor is the ratio between DC power delivered to the load and AC power rating of the transformer secondary.

$$TUF = \frac{Output\ PowerDC}{Power\ AC(rated)} \text{ X } 100$$

c. Ripple Factor

Ripple factor is the ratio between the RMS value of the input AC component and output DC component.

$$\gamma = \sqrt{\left(\frac{Irms}{Idc}\right)^2 - 1}$$

d. Peak Inverse Voltage (PIV)

Peak inverse voltage is the maximum amount of voltage drop across the diode, when it is reverse biased.

3.6.4 Comparison

Sno	Characteristics	Half Wave Rectifier	Full Wave Rectifier	Bridge Rectifier
1	No of diodes used	1	2	4
2	DC output Current	I_m/π	$2I_m/\pi$	$2I_m/\pi$
3	RMS current	$I_m/2$	$I_m/\sqrt{2}$	$I_m/\sqrt{2}$
4	Peak Inverse Voltage	V_m	$2V_m$	$2V_m$
5	Ripple factor	1.21	0.482	0.482
6	Ripple frequency	Input frequency	2 x input frequency	2 x input frequency
7	Transformer Utilization Factor	0.287	0.693	0.812
8	Efficiency	40.8 %	81.6 %	81.6 %

3.7 Filters

Even though the output current of the rectifier is unidirectional, its amplitude is not steady. The rectified output is in the form of half sinusoidal. There is a lot of variation in the amplitude of the output current so it is called pulsating current. These variations i.e. rise and fall in amplitude are called ripples. Filters are used to remove the ac ripples present in the rectified output and to give pure dc.

Capacitors and Inductors are used to get steady dc current from the pulsating dc output current of the rectifiers. Hence, capacitors and inductors are called filters. The types of filters are

1. Capacitor filter
2. Inductor filter
3. LC filter
4. pi (π) filter

Capacitor Filter

Capacitors are connected across or in parallel to the rectifiers. When the rectified current starts to rise, the capacitor gets charged to its peak value V_m. When the current starts falling, the capacitors discharge its stored energy. This reduces the ac component present in the dc output. This process is repeated for all half cycles of the rectified output. Large value capacitors are used as filters. The filtered output current value is nearer to the peak value of the input current.

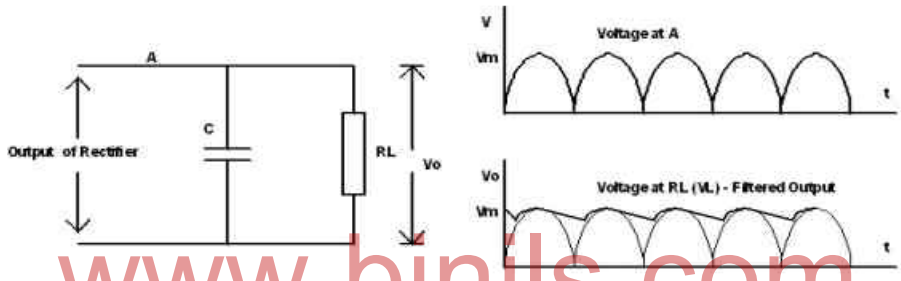


Fig 3.21 Capacitor filter and its output

Inductor Filter

Inductors are connected in series with the rectifiers. Inductors offer high resistance to the variation in the current flowing through it. Hence, the ac components are dropped across it. This process reduces the amount of ac component present in the dc output.

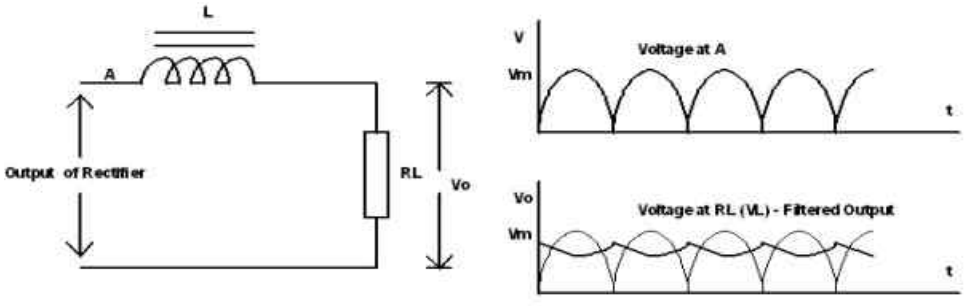


Fig 3.22 Inductor Filter

LC filter

Both capacitor and inductors are used as filters. Inductor is connected in series and capacitor is connected in parallel with the circuit. The high reactance of inductor removes the ac component. The same current flows through capacitor, which again removes the ac components. So the output contains almost only pure dc component.

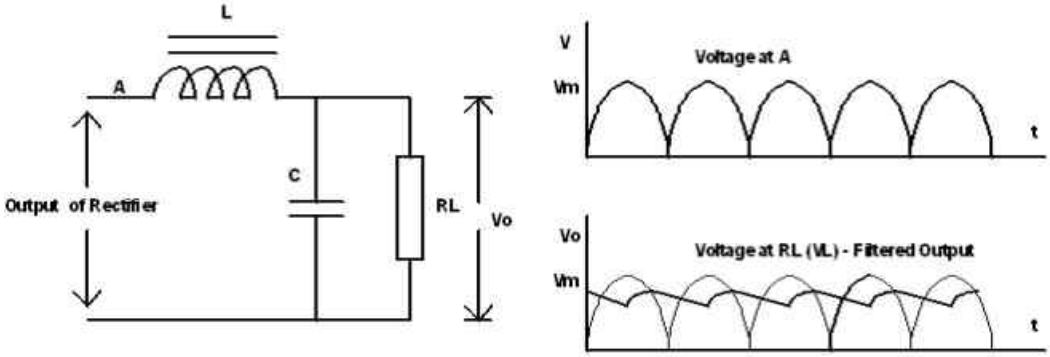


Fig 3.23 LC filter with its output

Pi (π) filter

Two capacitors and one inductor are connected in the form of pi symbol. It is also called capacitor input filter. The capacitor C_1, offers low reactance to the ac components of the rectified output. So the ac components are bypassed to ground through C_1.

The inductor L provides high reactance to the ac components. So the ac components are dropped across the inductor and dc component only is allowed to flow towards the load resistor.

The capacitor C_2, again removes the ac component present in the rectified current that comes out of inductor. Hence, the output contains only pure dc steady current.

3.8 Transistor

Definition

Transistor is a three terminal semiconductor device, formed by two junctions of three doped semiconductors. Either it is formed by one N type semiconductor sandwiched between two P type semiconductor (called PNP transistor) or it is formed by one P type semi conductor sandwiched between two N type semiconductor (called NPN transistor). It is basically used for amplification.

Three Terminals of Transistor

As transistor is formed by three doped semi conductors, it has three terminals. They are

1. Emitter 2. Base 3. Collector.

Emitter

In NPN transistor emitter is N type semiconductor and in PNP transistor it is P type semiconductor. It is named as 'emitter', because it emits charge carriers. N type semiconductor emits electrons and P type semiconductor emits holes. They pass through other two regions. Normally emitter is heavily doped and it is large in size.

Base

In NPN transistor, base is P type semiconductor and in PNP transistor it is N type semiconductor. It is named as 'base' because it is common to both emitter and collector. It is lightly doped and it is very thin in size.

Collector

In NPN transistor collector is N type semiconductor and in PNP transistor it is P type semiconductor. It is named as 'collector' because it collects the charge carriers emitted by the emitter. It is moderately doped and it is medium in size.

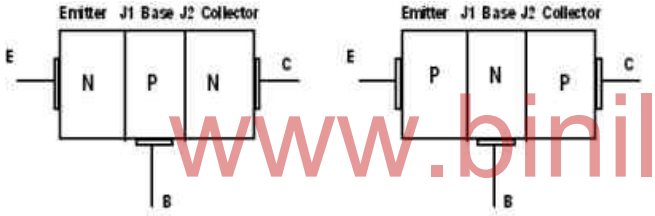


Fig 3.24 Structure of NPN and PNP Transistors

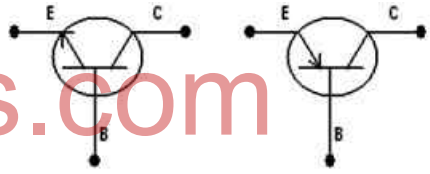


Fig 3.25 Symbol of NPN and PNP Transistor

Principle of NPN and PNP transistor

Normally emitter and base terminals are forward biased, so it has low resistance and base and collector terminals are reverse biased, so it has high resistance. When charge carriers move from emitter to base, only 10 percent of charge carriers are stay in the base, the remaining 90 percent charge carriers are moved to collector. Hence majority of current flows through the collector. Since it has high resistance, signal strength (e.g. Voltage) of the input signal is increased in the collector. Hence, we get amplified output at the output terminals. In this way, transistor works. As the input signal flow from low resistance to high resistance, it is named as TRANSfer of resISTOR.

3.8.1 Working of NPN transistor

The proper biasing of NPN transistor is shown in the figure. The emitter (N type) to base(P type) is forward biased by the battery V_{EB} and base (P type) to collector (N type) is reverse biased by the battery V_{BC}.

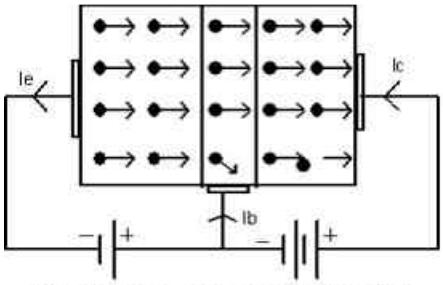


Fig 3.26 Working of NPN Transistor

The forward biased potential V_{EB} causes a lot of electrons to move from emitter to base region. It produces the emitter current I_E. The base region is lightly doped, hence a few number of electrons combined with the holes in base and produces the base current I_B. Majority of electrons moved to the collector region, which gives the collector current I_C. A small amount of reverse current also flows in the collector region.

The emitter current I_E is approximately equal to sum of I_B and I_C. The working of transistor is explained by its operation in the 3 regions. 1. Cut off region

2. Active region

3. Saturation region.

In the cut off region, V_{EB} is below the cut-in voltage and V_{CB} is reverse biased hence, no current only a very little current in the output terminal. In the Active region, V_{EB} is above the cut-in voltage and V_{CB} is reverse biased, so the output current starts to rise. In the saturation region, both V_{EB} and V_{CB} are in the forward biased. The transistor is working in the stable condition.

3.8.2 Configurations of Transistor

Out of the three terminals of a transistor, one terminal is connected as input terminal, the second one as output terminal and third terminal as common terminal. Based on this, a transistor is configured in the three different ways. There are,

1. Common Emitter configuration (CE)
2. Common Base configuration (CB)
3. Common Collector configuration (CC)

In the CE configuration, Emitter is common to both input and output, Base is the input terminal and collector is the output terminal, similarly for other configuration. The working of the transistor is determined by the following two characteristics.

1. Input characteristics
2. Output characteristics

The input characteristic is determined by taking the input voltage versus the input current with the constant output voltage. Hence,

$$\text{Input impedance} = \frac{\Delta Vi}{\Delta Ii} \text{ at constant output voltage}$$

The output characteristic is determined by taking the output voltage and the output current with the constant input current.

$$\text{output impedance} = \frac{\Delta Vo}{\Delta Ii} \text{ at constant input current}$$

3.8.3 Common Emitter Configuration of NPN transistor

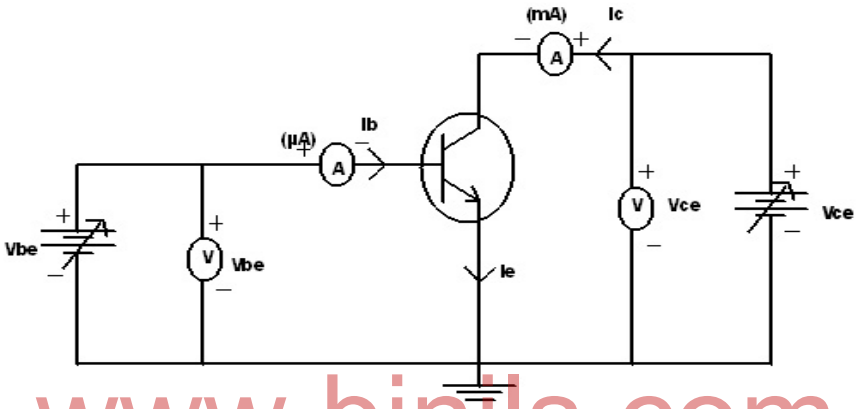


Fig. 3.27 CE Configuration

Base is the input terminal, collector is the output terminal and emitter is the common terminal. The base to emitter junction is forward biased and the emitter to collector junction is reverse biased. The working of transistor is determined by its input impedance and output impedance. In this configuration,

$$\text{Input impedance Zi} = \frac{\Delta VBE}{\Delta IB} \text{ at constant output voltage } V_{CE}$$

$$\text{output impedance Zo} = \frac{\Delta VCE}{\Delta IC} \text{ at constant input current } I_B$$

Input Characteristics

The reading is taken between the input voltage (V_{BE}) and the Input current (I_B), by keeping the output voltage (V_{EC}) at constant say 0V. This process is repeated by keeping the output voltage constant at another voltage, say 1V.

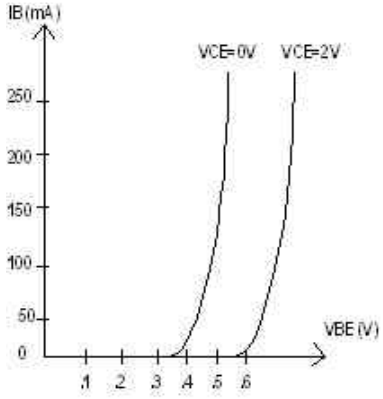


Fig 3.28 Input Characteristics

When V_{EC} is increased from 0V to 1V, the width of depletion in the reverse saturated emitter to collector junction is increased, which reduces the base current.

Output Characteristics

The reading is taken between the output voltage (V_{EC}) and the output current(I_c), by keeping the input current(I_B) at constant say 20mA.This process is repeated by keeping the input current constant at another ampere, say 40mA.

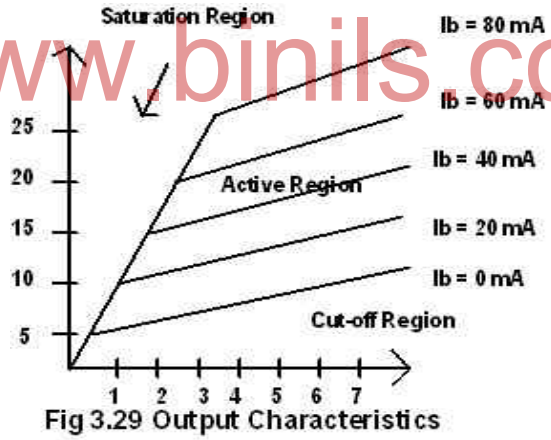


Fig 3.29 Output Characteristics

When the input current is increased, it causes increase in the output current.

3.8.4 Comparison of CB, CE, and CC Configuration

Like, CE configuration a transistor can be configured to work in common base, common collector configuration. These characteristics are varying according to their configuration.

S.No.	Characteristics	CB	CE	CC
1	Input Impedance	Low	Medium	High
2	Output Impedance	High	Medium	Low

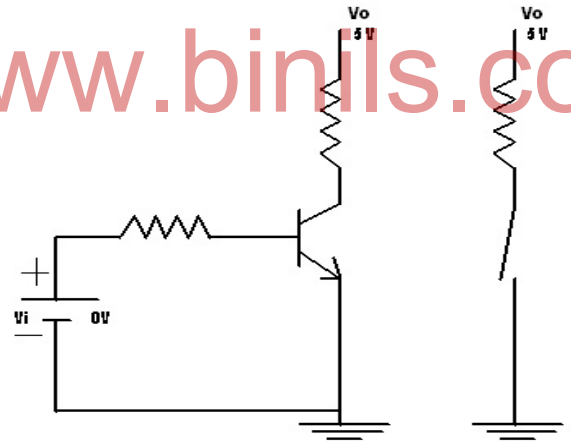
3.	Current gain	Low	High	High
4.	Voltage gain	High	High	Unity
5.	Power gain	Medium	High	Low
6.	Phase reversal	No	Yes	No
7.	Application	AF amplifier	Power amplifier	Impedance matching

3.8.5 Transistor as a Switch

A transistor can be used as a switch, by alternatively brought in saturation and cut-off conditions.

Cut-off condition (Opening the switch)

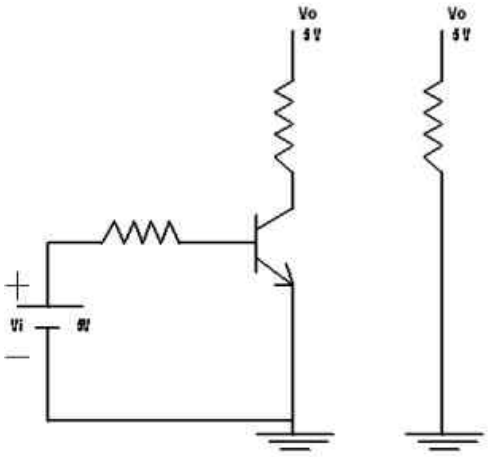
V_i is the input voltage which is kept at zero level. Hence, the transistor is not biased and not working i.e. it gives the high impedance. Therefore the voltage V_{cc} (5V) is not able to pass through the transistor to the ground. Hence the output voltage remains the same as 5V. Since the V_{cc} is not connected to the ground, the circuit is now opened i.e. the switch is opened.



Fir 3.30 Opening of Switch

Saturation condition (Closing the switch)

The input voltage V_i is given to 5V. Now the transistor is get forward biased and starts to conduct. i.e. It gives the low impedance. The V_{cc} (5V) is now flow through the transistor to the ground. Hence, the output voltage V_{cc} is now 0V. Since the V_{cc} is now connected to the ground and the circuit is closed i.e. the switch is closed.



Fir 3.31 Closing of Switch

SUMMARY

- ✓ Diode is a two terminal uni-directional device.
- ✓ Diode is used for rectification.
- ✓ Diode forms the junction between the P type and N type semi conductors.
- ✓ Diode can be biased in forward and reverse direction.
- ✓ Diode conducts in forward biasing and not conducts in reverse biasing.
- ✓ Above cut-in voltage the forward current starts to flow. Diode can be used as rectifier, voltage multiplier.
- ✓ Zener diode is a special purpose, heavily doped diode.
- ✓ In reverse bias, Zener diode maintains a constant voltage irrespective of input voltage.
- ✓ Zener diode is used for voltage regulator, protector.
- ✓ LED is a special purpose diode made up of Gallium compound.
- ✓ LED emits light under forward biased. The light may green, red, yellow etc.
- ✓ Photodiode works in just opposite direction of LED.
- ✓ It conducts current when light fall on it.
- ✓ The light gives energy to electrons to move.
- ✓ LDR is a Light Dependent Resistor.
- ✓ The resistance of LDR varies with amount of light fall on it.
- ✓ Rectifier is a circuit which converts ac signal into dc signal.
- ✓ The three types of rectifiers are a. Half wave, b. Full wave and c. Bridge.
- ✓ Half wave rectifier converts only half of the ac signal into dc.
- ✓ Full wave rectifier converts full ac signal into dc.
- ✓ The transformer utilization factor of bridge rectifier is high.

- ✓ Filter removes ac components (ripples) present in the rectifier output.
- ✓ Capacitor and Inductors are used as filters.
- ✓ LC and Pi filters are combinations of capacitor and inductor.
- ✓ Transistor is a three terminal device, used for amplification.
- ✓ The terminals are emitter, base and collector.
- ✓ Emitter emits the charge carriers, which moves through base and get collected by collector.
- ✓ Transistor can be configured in three ways 1. Common Emitter 2. Common Base and 3. Common Collector configuration
- ✓ In CE configuration emitter is common to both input and output terminal
- ✓ The working of a transistor is determined by 1. Input and 2. Output characteristics
- ✓ Input characteristic is determined by change in input current by change in input voltage at constant output voltage
- ✓ Output characteristic is determined by change in output current by the change in output voltage at constant input current
- ✓ Transistor can be used a switch, when input terminal is forward biased it closed and when no voltage is given to input terminal, it is opened

REVIEW QUESTIONS

Part A

1. What is a diode?
2. Define : Barrier voltage
3. Define : Depletion region
4. What do you mean by forward bias?
5. What do you mean by reverse bias?
6. State any two applications of diode
7. What is Zener diode?
8. Write the applications of Zener diode.
9. What is LED?
10. What is Light Dependent Resistor?
11. Define : Photo diode
12. What is rectification?

13. What are the types of rectifiers?
14. What is the use of filter?
15. Define : Ripple factor
16. Define : Efficient of a rectifier
17. What is PIV?
18. What are the terminals of a transistor?
19. What is NPN and PNP?
20. What are the three configurations of a transistor?

Part B

1. Write on forward biasing of a diode.
2. Write on reverse biasing of a diode.
3. State the three applications of a diode.
4. How zener diode works in reverse bias?
5. Write on the construction of LED.
6. How LED works?
7. How Photodiode works?
8. What is the working principle of LDR?
9. Write on the construction of LDR.
10. How a zener diode is working as meter protection?
11. How a Zener diode is used as wave shaper?
12. What is the need of rectification?
13. Write on working of Half wave rectifier.
14. Compare three types of rectifiers.
15. How capacitor is used as a filter?
16. How a inductor is used as a filter?
17. Write on pi filter?
18. How LC filter works?

19. Write on terminals of a transistor.
20. Write on input characteristics of a NPN transistor.
21. Write on output characteristics of NPN transistor.
22. Write on configurations of a transistor.

Part C

1. Write on working of PN junction diode in forward and reverse biasing.
2. Write on avalanche and zener break downs.
3. Write on working of principle of LED.
4. Explain the working principle of Photodiode.
5. Describe the working of Photo Dependent Resistor.
6. How full wave rectifier circuit works?
7. How a bridge rectifier works?
8. Write on various types of filters.
9. How a NPN transistor is working?
10. What are the input and output characteristics of a transistor?
11. How a transistor is used as switch?

- -

UNIT IV.BOOLEAN ALGEBRA, LOGIC GATES COMBINATIONAL SYSTEM
Syllabus

4.1 Number representation: Decimal, Binary, Octal and Hexadecimal number systems- Conversion of number from one number system to another (without decimal point) - BCD CODE – ASCII Codes - Parity bit – Use of a parity bit – Odd parity and even parity. [3]

4.2 Logic gates: Positive and Negative logic System - Definition, Truth table, Symbol and logical equations of AND – OR - NOT – EXOR - EXNOR (Only 2- inputs) gates – Universal gates - NAND - NOR – Symbol and truth table. [3]

4.3 Boolean Algebra: Basic laws of Boolean algebra – Demorgan's Theorem and proofs – Duality theorem - Simplification of logical equations using Boolean laws - De-Morgan's theorem – Two and three variable Karnaugh map.[3]

4.4 Arithmetic Circuits: Half Adder and full adder- Truth table, Circuit diagram – Half subtractor and Full subtractor - Truth table, Circuit diagram. [3]

4.5 Combinational logic circuits: Parity generator and checker - Multiplexer – De multiplexer – Encoder - Decoder (Definition and Basic Circuits only) – Comparator Circuit for two bit words.[2]

Rationale:

Diploma Engineers from all branches of engineering are expected to have some basic knowledge of electrical and electronics engineering. Also the technicians working in different engineering fields have to deal with various types of electrical equipments. Various types of electronic circuits are used in different electrical equipments. Hence it is necessary to study electric circuits, different types of electrical machines and electronic devices their principles and working characteristics. The basic concepts studied in this subject will be very useful for understanding of higher level subjects in further study.

Objectives:

On completion of the following units of syllabus contents, the students must be able to

- Understand the AC fundamentals
- Understand the working principle of UPS
- Know about stepper motors and servo motors
- Familiarize with semiconductor devices, rectifier circuits, transistors and its applications
- Use Binary, Octal and Hexadecimal numbers
- Define logic gates
- Significance of Boolean algebra in digital circuits
- Understand the working principles of sequential and combinational logic circuits
- Define Flip- flops and describe behaviour of various flip flops
- Know about Synchronous and Asynchronous counters
- Know about the function of shift registers

UNIT IV BOOLEAN ALGEBRA, LOGIC GATES COMBINATIONAL SYSTEM

On completion of this unit students can be able to

- Differentiate number systems like binary, octal, decimal and hexa decimal.
- Convert one number system to another.
- Represent BCD and ASCII codes
- Understand the use of parity bit.
- Differentiate between positive and negative logic levels for digital inputs and outputs.
- Draw the logic symbols and truth tables of logic gates
- Understand the laws of Boolean algebra, De Morgan's theorem and duality theorem.
- Simplify logical equations using Boolean laws.
- Understand the construction and working principle of arithmetic circuits.
- Principles of combinational logic circuits like parity generator, multiplexer, demultiplexer, encoder, decoder and comparator circuits.

4.1 Number Representation

Introduction

In our day-to-day lives we deal with the various physical quantities with numerical values. There are two basic ways of representing the numerical values of these quantities. One of the ways is to express the numerical value of the quantity as a continuous range of values between the two expected extreme values, which is referred to as ***analogue***. For example, the quantities like temperature, pressure and voltage are continuously varying and can have any of the infinite, theoretically possible values between the two extremes. This depends upon the accuracy of the measuring instrument.

Another possible way represents the numerical value of the quantity in steps of discrete values, which is referred to as ***digital***. There are fixed number of values or levels in a digital system. In general an analogue representation gives a continuous output. A digital representation produces a discrete output.

Analogue systems contain devices that process or work on various physical quantities represented in analogue form. **Digital systems** contain devices that process the physical quantities represented in digital form.

The study of ***number systems*** is important to understand how data are represented before they are processed by any digital system including a digital computer.

Different **characteristics of a number system** include the number of independent digits used in the number system, the place values of the different digits constituting the number and the maximum numbers that can be written with the given number of digits. Among the three characteristics the most fundamental is the number of independent digits or symbols used in the number system. It is known as the ***radix* or *base*** of the number system.

The number system we commonly use in our daily life is called the **decimal** number system. The decimal number system has a radix of 10 as it has 10 independent digits, i.e. 0, 1, 2, 3, 4, 5, 6, 7, 8 and 9. There are some other number systems: **binary, octal and**

hexadecimal. They are widely used in digital systems like microprocessors, logic circuits, computers, etc. The binary number system has only two independent digits, 0 and 1. The radix or base of the binary number system is 2. The octal and hexadecimal number systems have a radix (or base) of 8 and 16 respectively.

In any number system, there is an ordered set of symbols known as digits. A collection of these digits makes a number which has two parts: integer and fractional. They are separated by a radix point (for example decimal point). The place values of different digits in the integer part of the number are given by r^0, r^1, r^2, r^3 and so on, starting with the digit adjacent to the radix point. For the fractional part, these are r^{-1}, r^{-2}, r^{-3} and so on, again starting with the digit next to the radix point. Here, r is the radix of the number system. Also, maximum numbers that can be written with n digits in a given number system are equal to r^n.

Table 4.1 Characteristics of commonly used number systems

Number system	Base or radix	Symbols used (d_i or d_{-f})	Weight assigned to position	
			i (integer part)	*-f (Fractional part)*
Binary	2	0,1	2^i	2^{-f}
Octal	8	0,1,2,3,4,5,6,7	8^i	8^{-f}
Decimal	10	0,1,2,3,4,5,6,7,8,9	10^i	10^{-f}
Hexadecimal	16	0,1,2,3,4,5,6,7,8,9 A,B,C,D,E,F	16^i	16^{-f}

4.1.1 Number systems

Decimal Number System

- The number system that we use in our day-to-day life is the decimal number system.
- Decimal number system has base 10 as it uses 10 digits from 0 to 9. In decimal number system, the successive positions to the left of the decimal point represent units, tens, hundreds, thousands and so on.
- Each position represents a specific power of the base (10). For example, the decimal number 5263 consists of the digit 3 in the units position, 6 in the tens position, 2 in the hundreds position, and 5 in the thousands position, and its value can be written as

  $(5\times1000) + (2\times100) + (6\times10) + (3\times1)$
  $(5\times10^3) + (2\times10^2) + (6\times10^1) + (3\times10^0)$
  $5000 + 200 + 60 + 3$
  5263

The place values of different digits in a mixed decimal number, starting from the decimal point, are 100, 101, 102 and so on (for the integer part) and 10−1, 10−2, 10−3 and so on (for the fractional part).

Binary Number System

- Uses two digits, 0 and 1. [They are called as *bits* – binary digits]
- Also called base 2 number system
- Each position in a binary number represents a power of the base (2). Example: 2^0
- Last position in a binary number represents an x power of the base (2). Example: 2^x where x represents the last position - 1.

The binary number system is a radix-2 number system with '0' and '1' as the two independent digits. All larger binary numbers are represented in terms of '0' and '1'. The procedure for writing higher order binary numbers after '1' is similar to the one explained in the case of the decimal number system. For example, the first 16 numbers in the binary number system would be 0, 1, 10, 11, 100, 101, 110, 111, 1000, 1001, 1010, 1011, 1100, 1101, 1110 and 1111. The next number after 1111 is 10000, which is the lowest binary number with five digits. This also proves the point made earlier that a maximum of only 16 (= 24_ numbers could be written with four digits. Starting from the binary point, the place values of different digits in a mixed binary number are 20, 21, 22 and so on (for the integer part) and 2−1, 2−2, 2−3 and so on (for the fractional part).

Advantages of binary number system

The concept of binary number system was introduced by George Boole to study the mathematical theory of LOGIC which was developed as Boolean Algebra.

In digital circuits, two discrete signal levels HIGH and LOW can be represented by the binary digits 1 and 0 respectively. Since the digital signal can have only one of the two possible levels 1 or 0, the binary number system can be used for the analysis and design of digital systems.

Logic operations are the backbone of any digital computer, although solving a problem on computer could involve an arithmetic operation too. The introduction of the mathematics of logic by George Boole laid the foundation for the modern digital computer. He reduced the mathematics of logic to a binary notation of '0' and '1'. As the mathematics of logic was well established and had proved itself to be quite useful in solving all kinds of logical problem, and also as the mathematics of logic (also known as Boolean algebra) had been reduced to a binary notation, the binary number system had a clear edge over other number systems for use in computer systems.

Another significant advantage of this number system was that all kinds of data could be conveniently represented in terms of 0s and 1s. Also, basic electronic devices used for hardware implementation could be conveniently and efficiently operated in two distinctly different modes. For example, a bipolar transistor could be operated either in cut-off or in saturation very efficiently. Lastly, the circuits required for performing arithmetic operations such as addition, subtraction, multiplication, division, etc., become a simple affair when the data involved are represented in the form of 0s and 1s.

Example

Binary Number: 10101_2

Calculating Decimal Equivalent

Step	Binary Number	Decimal Number
Step 1	10101_2	$((1 \times 2^4) + (0 \times 2^3) + (1 \times 2^2) + (0 \times 2^1) + (1 \times 2^0))_{10}$
Step 2	10101_2	$(16 + 0 + 4 + 0 + 1)_{10}$
Step 3	10101_2	21_{10}

Note: 10101_2 is normally written as 10101.

Octal Number System

- Uses eight digits, 0,1,2,3,4,5,6,7.
- The largest single digit is 7. (one less than the base)
- Also called base 8 number system
- Each position in an octal number represents a power of the base (8). Example: 8^0
- Last position in an octal number represents an x power of the base (8). Example: 8^x where x represents the last position - 1.

Example

Octal Number 12570_8

Calculating Decimal Equivalent −

Step	Octal Number	Decimal Number
Step 1	12570_8	$((1 \times 8^4) + (2 \times 8^3) + (5 \times 8^2) + (7 \times 8^1) + (0 \times 8^0))_{10}$
Step 2	12570_8	$(4096 + 1024 + 320 + 56 + 0)_{10}$
Step 3	12570_8	5496_{10}

Note: 12570_8 is normally written as 12570.

Hexadecimal Number System

- Uses 16 symbols. There are 10 digits and 6 letters, 0,1,2,3,4,5,6,7,8,9,A,B,C,D,E,F.
- Letters represents numbers starting from 10. A = 10, B = 11, C = 12, D = 13, E = 14, F = 15.
- Also called base16 number system.
- Each position in a hexadecimal number represents a power of the base (16). Example 16^0.
- Last position in a hexadecimal number represents an x power of the base (16). Example 16^x where x represents the last position - 1.

The decimal number system is not used internally in computers. The values are stored as hexadecimal numbers in computer memory. The binary notation appears too long and inconvenient to handle. The hexadecimal number system provides a condensed way of representing large binary numbers stored and processed inside the computer. Each hex digit represents 4 bits of binary. One byte (8 bits) of data can be written as a two digit hexadecimal number. One such example is in representing addresses of different memory locations. In the hexadecimal number system, 65536 different addresses can be expressed with four hex digits from 0000 to FFFF. It is convenient to represent data in memory in hexadecimal form.

Example

Hexadecimal Number: $19FDE_{16}$

Calculating Decimal Equivalent

Step	Binary Number	Decimal Number
Step 1	$19FDE_{16}$	$((1 \times 16^4) + (9 \times 16^3) + (F \times 16^2) + (D \times 16^1) + (E \times 16^0))_{10}$
Step 2	$19FDE_{16}$	$((1 \times 16^4) + (9 \times 16^3) + (15 \times 16^2) + (13 \times 16^1) + (14 \times 16^0))_{10}$
Step 3	$19FDE_{16}$	$(65536 + 36864 + 3840 + 208 + 14)_{10}$
Step 4	$19FDE_{16}$	106462_{10}

Note – $19FDE_{16}$ is normally written as 19FDE.

Number Systems – Some Common Terms

In this section we will describe some commonly used terms with reference to different number systems.

Binary Number System

Bit is an abbreviation of the term 'binary digit' and is the smallest unit of information. It is either '0' or '1'. A *byte* is a string of eight bits. The byte is the basic unit of data operated upon as a single unit in computers. A *computer word* is again a string of bits whose size, called the 'word length' or 'word size', is fixed for a specified computer, although it may vary from computer to computer. The word length may equal one byte, two bytes, four bytes or be even larger.

The ***1's complement*** of a binary number is obtained by complementing all its bits, i.e. by replacing 0s with 1s and 1s with 0s. For example, the 1's complement of (10010110)2 is (01101001)2. The ***2's complement*** of a binary number is obtained by adding '1' to its 1's complement. The 2's complement of (10010110)2 is (01101010)2.

Decimal Number System

Corresponding to the 1's and 2's complements in the binary system, in the decimal number system we have the 9's and 10's complements. The ***9's complement*** of a given decimal number is obtained by subtracting each digit from 9. For example, the 9's complement of (2496)10 would be (7503)10. The ***10's complement*** is obtained by adding '1' to the 9's complement. The 10's complement of (2496)10 is (7504)10.

Octal Number System

In the octal number system, we have the 7's and 8's complements. The ***7's complement*** of a given octal number is obtained by subtracting each octal digit from 7. For example, the 7's complement of (562)8 would be (215)8. The ***8's complement*** is obtained by adding '1' to the 7's complement. The 8's complement of (562)8 would be (216)8.

Hexadecimal Number System

The 15's and 16's complements are defined with respect to the hexadecimal number system. The ***15's complement*** is obtained by subtracting each hex digit from 15. For example, the 15's complement of (3BF)16 would be (C40)16. The ***16's complement*** is obtained by adding '1' to the 15's complement. The 16's complement of (2AE)16 would be (D52)16.

Finding the Decimal Equivalent

The decimal equivalent of a given number in another number system is given by the sum of all the digits multiplied by their respective place values. The integer and fractional parts of the given number should be treated separately. Binary-to-decimal, octal-to-decimal and hexadecimal-to-decimal conversions are illustrated below with the help of examples.

4.1.2 Conversion between number systems

There are many methods or techniques which can be used to convert numbers from one base to another. The following types of conversions are usually required in many applications.

Decimal to Other Base System
Other Base System to Decimal
Other Base System to Non-Decimal

The following shortcut methods are also discussed
Shortcut method − Binary to Octal
Shortcut method − Octal to Binary
Shortcut method − Binary to Hexadecimal
Shortcut method − Hexadecimal to Binary

Conversion from Decimal to Other Base System

Steps for converting decimal number into other (other base) number systems.

Step 1 − Divide the decimal number to be converted by the value of the new base.

Step 2 − Get the remainder from Step 1 as the rightmost digit *least significant digit* of new base number.

Step 3 − Divide the quotient of the previous divide by the new base.

Step 4 − Record the remainder from Step 3 as the next digit *to the left* of the new base number.

Repeat Steps 3 and 4, getting remainders from right to left, until the quotient becomes zero in Step 3.

The last remainder thus obtained will be the Most Significant Digit *MSD* of the new base number.

Example −
Decimal Number: 29_{10}

Calculating Binary Equivalent

Step	Operation	Result	Remainder
Step 1	29 / 2	14	1
Step 2	14 / 2	7	0
Step 3	7 / 2	3	1
Step 4	3 / 2	1	1
Step 5	1 / 2	0	1

As mentioned in Steps 2 and 4, the remainders have to be arranged in the reverse order so that the first remainder becomes the Least Significant Digit *LSD* and the last remainder becomes the Most Significant Digit *MSD*.

Decimal Number − 29_{10} = Binary Number − 11101_2.

Conversion from other Base System to Decimal System

Steps
Step 1 − Determine the column *positional* value of each digit *this depends on the position of the digit and the base of the number system*.

Step 2 – Multiply the obtained column values *inStep*1 by the digits in the corresponding columns.

Step 3 − Sum the products calculated in Step 2. The total is the equivalent value in decimal.

Example

Binary Number − 111012

Calculating Decimal Equivalent −

Step	Binary Number	Decimal Number
Step 1	11101_2	$((1 \times 2^4) + (1 \times 2^3) + (1 \times 2^2) + (0 \times 2^1) + (1 \times 2^0))_{10}$
Step 2	11101_2	$16 + 8 + 4 + 0 + 1_{10}$
Step 3	11101_2	29_{10}

Binary Number 11101_2 = Decimal Number 29_{10}

Other Base System to Non-Decimal System

Steps
Step 1 − Convert the original number to a decimal number *base*10.
Step 2 − Convert the decimal number obtained to the new base number.

Example
Converting octal number 25_8 binary equivalent

Step 1 − Convert to Decimal

Step	Octal Number	Decimal Number
Step 1	25_8	$((2 \times 8^1) + (5 \times 8^0))_{10}$
Step 2	25_8	$16 + 5_{10}$
Step 3	25_8	21_{10}

Octal Number 25_8 = Decimal Number = 21_{10}

Binary-to-Decimal Conversion

The decimal equivalent of the binary number (1001.0101)2 is determined as follows:
• The integer part = 1001
• The decimal equivalent = $1 \times 2^0 + 0 \times 2^1 + 0 \times 2^2 + 1 \times 2^3 = 1 + 0 + 0 + 8 = 9$
• The fractional part = .0101
• Therefore, the decimal equivalent = $0 \times 2^{-1} + 1 \times 2^{-2} + 0 \times 2^{-3} + 1 \times 2^{-4} = 0 + 0.25 + 0 + 0.0625 = 0.3125$
• Therefore, the decimal equivalent of $(1001.0101)_2 = 9.3125$

Octal-to-Decimal Conversion

The decimal equivalent of the octal number (137.21)8 is determined as follows:
• The integer part = 137
• The decimal equivalent = $7 \times 8^0 + 3 \times 8^1 + 1 \times 8^2 = 7 + 24 + 64 = 95$

The fractional part = .21
• The decimal equivalent = $2 \times 8^{-1} + 1 \times 8^{-2} = 0.265$
• Therefore, the decimal equivalent of $(137.21)_8$
$= (95.265)_{10}$

Hexadecimal-to-Decimal Conversion

The decimal equivalent of the hexadecimal number (1E0.2A)16 is determined as follows:

• The integer part = 1E0
• The decimal equivalent = $0 \times 16^0 + 14 \times 16^1 + 1 \times 16^2 = 0 + 224 + 256 = 480$
• The fractional part = 2A
• The decimal equivalent = $2 \times 16^{-1} + 10 \times 16^{-2} = 0.164$
• Therefore, the decimal equivalent of (1E0.2A)16
= $(480.164)_{10}$

Shortcut method for Binary to Octal
Steps

Step 1 − Divide the binary digits into groups of three ***starting from the right***.

Step 2 − Convert each group of three binary digits to one octal digit.

Example
Converting binary number 10101_2 to octal equivalent

Step	**Binary Number**	**Octal Number**
Step 1	10101_2	010 101
Step 2	10101_2	2_8 5_8
Step 3	10101_2	25_8

Binary Number 10101_2 = Octal Number 25_8

Shortcut method for Octal to Binary

Steps

Step 1 − Convert each octal digit to a 3 digit binary number.

Step 2 − Combine all the resulting binary groups of 3 digits each into a single binary number.

Example

Converting octal number 25_8 to binary equivalent

Step	**Octal Number**	**Binary Number**
Step 1	25_8	2 5
Step 2	25_8	010_2 101_2

Shortcut method for Binary to Hexadecimal

Steps

Step 1 − Divide the binary digits into groups of four ***starting from the right***.

Step 2 − Convert each group of four binary digits to one hexadecimal symbol.

Example

Converting binary number 10101_2 to hexadecimal equivalent

Step	Binary Number	Hexadecimal Number
Step 1	10101_2	0001 0101
Step 2	10101_2	1_{16} 5_{16}
Step 3	10101_2	15_{16}

Binary Number 10101_2 = Hexadecimal Number 15_{16}

Shortcut method for Hexadecimal to Binary

Steps

Step 1 − Convert each hexadecimal digit to a 4 digit binary number

Step 2 − Combine all the resulting binary groups *of* 4 *digits each* into a single binary number.

Example

Converting hexadecimal number 15_{16} to binary equivalent

Step	Hexadecimal Number	Binary Number
Step 1	15_{16}	1_{16} 5_{16}
Step 2	15_{16}	0001_2 0101_2
Step 3	15_{16}	00010101_2

Hexadecimal Number 15_{16} = Binary Number 10101_2

Number Representation in Binary

Different formats used for binary representation of both positive and negative decimal numbers include the sign-bit magnitude method, the 1's complement method and the 2's complement method.

Sign-Bit Magnitude

In the sign-bit magnitude representation of positive and negative decimal numbers, the MSB represents the 'sign', with a '0' denoting a plus sign and a '1' denoting a minus sign. The remaining bits represent the magnitude. In eight-bit representation, while MSB represents the sign, the remaining seven bits represent the magnitude. For example, the eight-bit representation of +9 would be 00001001, and that for −9 would be 10001001. An

n−bit binary representation can be used to represent decimal numbers in the range of −(2n−1−1) to +(2n−1−1). That is, eight-bit representation can be used to represent decimal numbers in the range from −127 to +127 using the sign-bit magnitude format.

1's Complement

In the 1's complement format, the positive numbers remain unchanged. The negative numbers are obtained by taking the 1's complement of the positive counterparts. For example, +9 will be represented as 00001001 in eight-bit notation, and −9 will be represented as 11110110, which is the 1's complement of 00001001. Again, n-bit notation can be used to represent numbers in the range from −(2n−1−1) to +(2n−1−1) using the 1's complement format. The eight-bit representation of the 1's complement format can be used to represent decimal numbers in the range from −127 to +127.

2's Complement

In the 2's complement representation of binary numbers, the MSB represents the sign, with a '0' used for a plus sign and a '1' used for a minus sign. The remaining bits are used for representing magnitude. Positive magnitudes are represented in the same way as in the case of sign-bit or 1's complement representation. Negative magnitudes are represented by the 2's complement of their positive counterparts. For example, +9 would be represented as 00001001, and −9 would be written as 11110111. Please note that, if the 2's complement of the magnitude of +9 gives a magnitude of −9, then the reverse process will also be true, i.e. the 2's complement of the magnitude of −9 will give a magnitude of +9. The n-bit notation of the 2's complement format can be used to represent all decimal numbers in the range from +(2n−1−1) to −(2n−1_. The 2's complement format is very popular as it is very easy to generate the 2's complement of a binary number and also because arithmetic operations are relatively easier to perform when the numbers are represented in the 2's complement format.

Decimal-to-Binary Conversion

As outlined earlier, the integer and fractional parts are worked on separately. For the integer part, the binary equivalent can be found by successively dividing the integer part of the number by 2 and recording the remainders until the quotient becomes '0'. The remainders written in reverse order constitute the binary equivalent. For the fractional part, it is found by successively multiplying the fractional part of the decimal number by 2 and recording the carry until the result of multiplication is '0'. The carry sequence written in forward order constitutes the binary equivalent of the fractional part of the decimal number. If the result of multiplication does not seem to be heading towards zero in the case of the fractional part, the process may be continued only until the requisite number of equivalent bits has been obtained. This method of decimal–binary conversion is popularly known as the double-dabble method. The process can be best illustrated with the help of an example.

Example

Find the binary equivalent of (13.375)10.

Solution

• The integer part = 13

Divisor	Dividend	Remainder
2	13	—
2	6	1
2	3	0
2	1	1
—	0	1

• The binary equivalent of (13)10 is therefore (1101)2
• The fractional part = .375
• 0.375 × 2 = 0.75 with a carry of 0
• 0.75 × 2 = 0.5 with a carry of 1
• 0.5 × 2 = 0 with a carry of 1
• The binary equivalent of (0.375)10
= (.011)2
• Therefore, the binary equivalent of (13.375)10
= (1101.011)2

Decimal-to-Octal Conversion

The process of decimal-to-octal conversion is similar to that of decimal-to-binary conversion. The progressive division in the case of the integer part and the progressive multiplication while working on the fractional part here are by '8' which is the radix of the octal number system. Again, the integer and fractional parts of the decimal number are treated separately. The process can be best illustrated with the help of an example.

Example

We will find the octal equivalent of (73.75)10

Solution

• The integer part = 73

Divisor	Dividend	Remainder
8	73	—
8	9	1
8	1	1
—	0	1

The octal equivalent of (73)10
= (111)8
• The fractional part = 0.75
• 0.75 × 8 = 0 with a carry of 6
• The octal equivalent of (0.75)10
= (.6)8
• Therefore, the octal equivalent of (73.75)10

= (111.6)8

Decimal-to-Hexadecimal Conversion

The process of decimal-to-hexadecimal conversion is also similar. Since the hexadecimal number system has a base of 16, the progressive division and multiplication factor in this case is 16. The process is illustrated further with the help of an example.

Example 1.5

*Let us determine the hexadecimal equivalent of (82.25)10_*

Solution
• The integer part = 82

Divisor Dividend Remainder

16 82 —
16 5 2
— 0 5

• The hexadecimal equivalent of (82)10
= (52)16

• The fractional part = 0.25
• 0.25 × 16 = 0 with a carry of 4
• Therefore, the hexadecimal equivalent of (82.25)10
= (52.4)16

Binary to Octal and Octal to Binary Conversions

An octal number can be converted into its binary equivalent by replacing each octal digit with its three-bit binary equivalent. We take the three-bit equivalent because the base of the octal number system is 8 and it is the third power of the base of the binary number system, i.e. 2. All we have then to remember is the three-bit binary equivalents of the basic digits of the octal number system. A binary number can be converted into an equivalent octal number by splitting the integer and fractional parts into groups of three bits, starting from the binary point on both sides. The 0s can be added to complete the outside groups if needed.

Example

*Let us find the binary equivalent of (374.26)8 and the octal equivalent of (1110100.0100111)2_*

Solution
• The given octal number = (374.26)8
• The binary equivalent = (011 111 100.010 110)2
= (011111100.010110)2
Any 0s on the extreme left of the integer part and extreme right of the fractional part of the equivalent

binary number should be omitted. Therefore, (011111100.010110)2
= (11111100.01011)2
• The given binary number = (1110100.0100111)2
• (1110100.0100111)2
= (1 110 100.010 011 1)2
= (001 110 100.010 011 100)2
= $(164.234)_8$

Hexadecimal to Binary and Binary to Hexadecimal Conversions

A hexadecimal number can be converted into its binary equivalent by replacing each hex digit with its four-bit binary equivalent. We take the four-bit equivalent because the base of the hexadecimal number system is 16 and it is the fourth power of the base of the binary number system. All we have then to remember is the four-bit binary equivalents of the basic digits of the hexadecimal number system. A given binary number can be converted into an equivalent hexadecimal number by splitting the integer and fractional parts into groups of four bits, starting from the binary point on both sides. The 0s can be added to complete the outside groups if needed.

Example 1.7
Let us find the binary equivalent of (17E.F6)16 and the hex equivalent of (1011001110.011011101)2.
Solution
• The given hex number = (17E.F6)16
• The binary equivalent = (0001 0111 1110.1111 0110)2
= (000101111110.11110110)2
= (101111110.1111011)2

• The 0s on the extreme left of the integer part and on the extreme right of the fractional part have
been omitted.
• The given binary number = (1011001110.011011101)2
= (10 1100 1110.0110 1110 1)2
• The hex equivalent = (0010 1100 1110.0110 1110 1000)2
= (2CE.6E8)16

Hex–Octal and Octal–Hex Conversions

For hexadecimal–octal conversion, the given hex number is firstly converted into its binary equivalent which is further converted into its octal equivalent. An alternative approach is firstly to convert the given hexadecimal number into its decimal equivalent and then convert the decimal number into an equivalent octal number. The former method is definitely more convenient and straightforward. For octal–hexadecimal conversion, the octal number may first be converted into an equivalent binary number and then the binary number transformed into its hex equivalent. The other option is firstly to convert the given octal number into its decimal equivalent and then convert the decimal number into its hex equivalent. The former approach is definitely the preferred one. Two types of conversion are illustrated in the following example.

Example 1.8
*Let us find the octal equivalent of (2F.C4)16 and the hex equivalent of (762.013)8_*

Solution

• The given hex number = (2F.C4)16.
• The binary equivalent = (0010 1111.1100 0100)2
= (00101111.11000100)2
= (101111.110001)2
= (101 111.110 001)2
= (57.61)8.
• The given octal number = (762.013)8.
• The octal number = (762.013)8
= (111 110 010.000 001 011)2
= (111110010.000001011)2
= (0001 1111 0010.0000 0101 1000)2
= (1F2.058)16.

4.1.3 Binary Coded Decimal (BCD)

The binary coded decimal (BCD) is a type of binary code used to represent a given decimal number in an equivalent binary form. In BCD code, each decimal digit of the number is represented by its 4 bit binary equivalent. The BCD code is not a number system but it is an encoding system.

Decimal Digit	BCD Code (8421)
0	0000
1	0001
2	0010
3	0011
4	0100
5	0101
6	0110
7	0111
8	1000
9	1001

The BCD code described above is known as the 8421 BCD code, with 8, 4, 2 and 1 representing the weights of different bits in the four-bit groups, starting from MSB and proceeding towards LSB.

For example the BCD code for the decimal number 6257 is

```
  6       2       5       7       Decimal
0110    0010    0101    0111      BCD
```

BCD-to-decimal and decimal-to-BCD conversions are very easy and straightforward. It is also easier to represent a given decimal number in an equivalent BCD code than to represent it in the equivalent binary.

Advantage of the BCD: It is easy to convert from decimal to binary and binary to decimal.

Packed and Unpacked BCD Numbers

In the case of unpacked BCD numbers, each four-bit BCD group corresponding to a decimal digit is stored in a separate register inside the machine. In such a case, the registers are eight bits or wider, the register space is wasted. In the case of packed BCD numbers, two BCD digits are stored in a single eight-bit register.

The process of combining two BCD digits so that they are stored in one eight-bit register involves shifting the number in the upper register to the left 4 times and then adding the numbers in the upper and lower registers. The process is illustrated by showing the storage of decimal digits '5' and '7':

• Decimal digit 5 is initially stored in the eight-bit register as: 0000 0101.
• Decimal digit 7 is initially stored in the eight-bit register as: 0000 0111.
• After shifting to the left 4 times, the digit 5 register reads: 0101 0000.
• The addition of the contents of the digit 5 and digit 7 registers now reads: 0101 0111.

BCD-to-Binary Conversion

A given BCD number can be converted into an equivalent binary number by first writing its decimal equivalent and then converting it into its binary equivalent. The first step is straightforward, and the second step was explained in the previous chapter. As an example, we will find the binary equivalent of the BCD number 0010 1001.0111 0101:

• BCD number: 0010 1001.0111 0101.
• Corresponding decimal number: 29.75.
• The binary equivalent of 29.75 can be determined to be 11101 for the integer part and .11 for the fractional part.
• Therefore, (0010 1001.0111 0101)BCD =(11101.11)2.

Binary-to-BCD Conversion

The process of binary-to-BCD conversion is the same as the process of BCD-to-binary conversion executed in reverse order. A given binary number can be converted into an equivalent BCD number by first determining its decimal equivalent and then writing the corresponding BCD equivalent. As an example, we will find the BCD equivalent of the binary number 10101011.101:

• The decimal equivalent of this binary number can be determined to be 171.625.
• The BCD equivalent can then be written as 0001 0111 0001.0110 0010 0101.

4.1.4 ASCII code

The **ASCII** stands for **American Standard Code for Information Interchange**. It is pronounced as 'ask-ee'. It is a seven-bit code based on the English alphabet.

ASCII codes are used to represent alphanumeric data in computers, communication equipments and other related devices.

The code was first published as a standard in 1967.

Since it is a seven-bit code, it can at the most represent 128 characters.

It currently defines 95 printable characters including 26 upper-case letters (A to Z), 26 lower-case letters (a to z), 10 numerals (0 to 9) and 33 special characters including mathematical symbols, punctuation marks and space character.

In addition, it defines codes for 33 nonprintable control characters that affect how text is processed. For example, new line character, tab characters, backspace, form feed, carriage return and cursor control characters.

An eight-bit version of the ASCII code, known as US ASCII-8 or ASCII-8, has also been developed. The eight-bit version can represent a maximum of 256 characters.

ASCII Codes in Decimal	In Hexadecimal	Characters
0-31	00h-1Fh	Control characters
32	20h	Space (Blank)
33-47	21-2F	! " # $ % & ' ( ) * + , - . /
48-57	30h-39h	0 1 2 3 4 5 6 7 8 9
58-64	3Ah-40h	: ; < = > ? @
65-90	41h-5Ah	A-Z
91-96	5Bh-60h	[\ ] ^ _ `
97-122	61h-7Ah	a-z
123-127	7Bh-7Fh	{ \ } ~ DEL

The alphanumeric ASCII code is the modern code for getting information into and out of microcomputers. ASCII is used when interfacing computer keyboards, printers, and video displays. ASCII has become the standard input/output code for microcomputers.

The ASCII code is used extensively in small computer systems to translate from the keyboard characters to computer language. The alphanumeric ASCII code is the modern code for getting information into and out of microcomputers. ASCII is used when interfacing computer keyboards, printers, and video displays. ASCII has become the standard input, output code for microcomputers.

4.1.5 Parity Bit

A parity bit is an extra bit added to a group of data bits in order to detect any single bit error while it was being stored or processed and transmitted from one place to another in a digital system.

Use of a parity bit

Parity bit is used to detect a single bit error in data transmission. When a binary data is transmitted and processed, it is susceptible to noise that can distort its contents. The 1's may get changed to 0s and 0s to 1. Several schemes are used to detect the occurrence of a single bit error in a binary word and correct the binary word and transmit it. The simplest technique for detecting errors is that of adding an extra bit to each word being transmitted. This extra bit is known as the **parity bit**.

Odd Parity and Even Parity

There are two types of parity, odd parity and even parity. In an *even parity*, the added bit is such that the total number of 1s in the data bit string becomes even. In an *odd parity*, the added bit makes the total number of 1s in the data bit string odd.

For odd parity, the parity bit is set to a 0 or a 1 at the transmitter such that the total number of 1s in the word including the parity bit is an odd number. For even parity, the parity bit is set to a 0 or a 1 at the transmitter such that the total number of 1s in the word including the parity bit is an even number.

Error detection with parity bits

An error occurs if odd number of 1s appears in the received data word coded for even parity. Single or odd number bit errors can be detected using parity bit. Two or even number bit errors will not be detected. This simple parity code suffers from these limitations.

Error Correction

. Parity bit allows us only to detect the presence of one bit error in a group of bits
. It does not enable us to exactly locate the bit that changed
. Parity bit scheme can be extended to locate the faulty bit in a block of information

4.2 Logic Gates

Introduction

The logic gate is the basic building block in digital systems. The logic gate is a digital circuit with one or more inputs and one output. Logic gates can be operated with binary numbers. Gates are therefore referred to as binary logic gates. All the voltages used with logic gates will be either HIGH or LOW. A HIGH voltage will mean a binary 1. A LOW voltage will mean a binary 0. Logic gates are electronic circuits. These circuits will respond only to HIGH voltages (called 1s) or LOW (ground) voltages (called 0 s)**.**

All digital systems are constructed by using only three basic logic gates. There are three basic logic gates, namely the AND gate, the OR gate and the NOT gate. Other logic gates that are derived from these basic gates are the NAND gate, the NOR gate, the EXCLUSIVE-OR gate and the EXCLUSIVE-NOR gate.

These basic gates are called the AND gate, the OR gate, and the NOT gate. This chapter deals with these very important basic logic gates or functions.

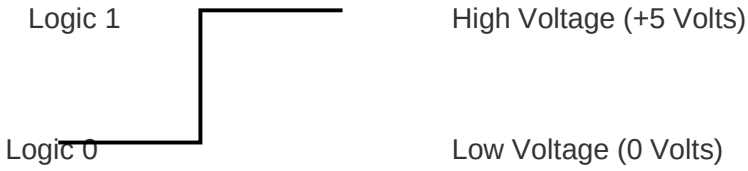
4.2.1 Positive and Negative Logic System

The binary variables can have either of the two states, i.e. the logic '0' state or the logic '1' state. These logic states in digital systems such as computers are represented by two different voltage levels or two different current levels. Depending on how these signal levels are represented as logic values, the digital systems are classified into **positive logic** and **negative logic.**

In ***positive logic system***, the more positive of the two voltage or current levels represents a logic '1' and the less positive of the two levels represents a logic '0'.

In ***negative logic system*** the more positive of the two voltage or current levels represents a logic '0' and the less positive of the two levels represents a logic '1'.

Positive Logic



Negative Logic

If the two voltage levels are 0 V and +5 V, then in the positive logic system the 0 V represents a logic '0' and the +5 V represents a logic '1'. In the negative logic system, 0 V represents logic '1' and 5 V represents logic '0'.

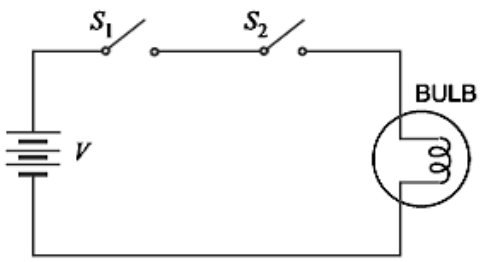
If the two voltage levels are 0 V and −5 V, then in the positive logic system the 0 V represents a logic '1' and the −5 V represents a logic '0'. In the negative logic system, 0 V represents logic '0' and −5 V represents logic '1'.

It is interesting to note that, a positive OR is a negative AND. That is, OR gate hardware in the positive logic system behaves like an AND gate in the negative logic system. The reverse is also true. Similarly, a positive NOR is a negative NAND, and vice versa.

4.2.2 Logic Gates

A digital circuit with one or more input signals but only one output signal is called a **logic gate**. Since logic gate is a switching circuit (*i.e*. a digital circuit), its output can have only one of the two possible states *viz.*, either a high voltage (1) or a low voltage (0). It is either *ON* or *OFF.* Whether the output voltage of a logic gate is high (1) or low (0) will depend

upon the conditions at its input. Fig. 4.1 shows the basic idea of a logic gate using switches.



(i)

S_1	S_2	Bulb
open	open	OFF
open	closed	OFF
closed	open	OFF
closed	closed	ON

(ii)

Truth Table

S_1	S_2	Output
0	0	0
0	1	0
1	0	0
1	1	1

(iii)

Fig. 4.1 Basic idea of logic gate using switches

The four possible combinations of switches *S*1 and *S*2 are shown in the table on the previous page. It is clear that when either of the switches (*S*1 or *S*2) or both are open, the bulb is *OFF*. In binary language, when either of the inputs or both the inputs are low (0), the output is low. When both switches are closed, the bulb is *ON*. In terms of binary language, when both the inputs are high (1), the output is high. It is usual practice to show the conditions at the input and output of a logic gate in the binary form as shown in the table on the previous page. Such a table is called **truth table**.
The term "logic" is usually used to refer to a decision-making process. A logic gate makes logical decisions regarding the existence of output depending upon the nature of the input. Hence, such circuits are called logic circuits.

Truth Table

A truth table lists all possible combinations of input binary variables and the corresponding outputs of a logic system. The logic system output can be found from the logic expression, often referred to as the Boolean expression that relates the output with the inputs of the logic system.

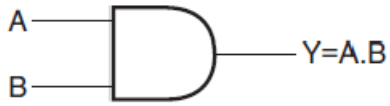
AND Gate

The AND gate is called the **"all or nothing"** gate. The schematic in Fig. 4-1(a) shows the idea of AND gate using switching circuit. The bulb will light only when both input switches (***S_1*** and ***S_2***) are closed. All the possible combinations for switches **S_1** and **S_2** are shown in Fig. 4.1.b. The table in this figure is called a truth table. The truth table shows that the output is enabled (lit) only when both switches are closed.

An AND gate is a logic circuit having two or more inputs and one output. The output of an AND gate is HIGH only when all of its inputs are in the HIGH state. In all other cases, the output is LOW. When interpreted for a positive logic system, this means that the output of the AND gate is a logic '1' only when all of its inputs are in logic '1' state. In all other cases, the output is logic '0'.

The logic symbol and truth table of a two-input AND gate are shown in Fig 4.2(a) and (b) respectively. The AND operation on two independent logic variables A and B is written as

Y=A▪B and reads as Y equals A AND B and not as A multiplied by B. Here, A and B are input logic variables and Y is the output.



(a)

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

(b)

Fig. 4.2 Two input AND gate. (a) Logic symbol (b) Truth table

A - B = Y

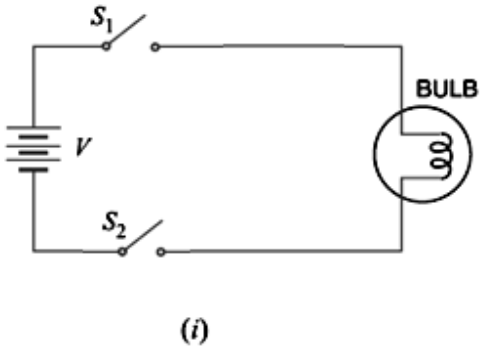
The Boolean expression is read as ***A*** AND (. means AND) ***B*** equals the output ***Y.*** The dot means the logic function AND in Boolean algebra, ***not*** multiplies as in regular algebra, Sometimes the dot (.) is left out of the Boolean expression. The Boolean expression for the 2-input AND gate is then:

A B = Y

The Boolean expression reads ***A*** AND ***B*** equals the output ***Y.***

OR Gate

The OR gate is called the **"any or all"** gate. The schematic in Fig. 4.3 (i) shows the idea of the OR gate. The bulb will glow when either switch S1 ***or*** switch S2 is closed. The bulb will also glow when both switches are closed. The bulb will *not* glow when both switches are open. All the possible switch combinations are shown in Fig. 4.3.(ii). The truth table details the *OR* function of the switch and lamp circuit. The output of the OR circuit will be enabled (lamp lit) when any or all input switches are closed.



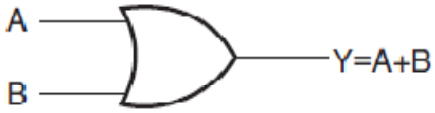
S_1	S_2	Bulb
open	open	OFF
open	closed	ON
closed	open	ON
closed	closed	ON

(i) (ii)

Fig. 4.3.(i) OR circuit using switches (ii) Truth table of OR circuit

An OR gate performs a logical OR operation on two or more than two logic variables. The OR operation on two independent logic variables A and B is written as Y = A+B and reads as Y equals A OR B and not as A plus B. An OR gate is a logic circuit with two or more inputs and one output. The output of an OR gate is LOW only when all of its inputs are LOW. For all other possible input combinations, the output is HIGH. This statement when interpreted for a positive logic system means the following. The output of an OR gate is a logic '0' only when all of its inputs are at logic '0'. For all other possible input combinations, the output is logic '1'. Figure 4.4 shows the logic symbol and the truth table of a two-input OR gate. The operation of a two-input OR gate is explained by the logic expression

Y = A+B

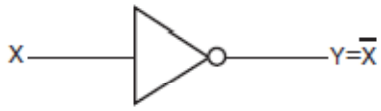


A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

Fig.4.4 The logic symbol, logical equation and the truth table of two Input OR gate

NOT Gate

A NOT gate is also called an inverter. A NOT gate, or inverter, is an unusual gate. The NOT gate has only one input and one output. Figure 4.5.a. illustrates the logic symbol for the inverter, or NOT gate. The process of inverting is simple. Figure 4.5.b is the truth table for the NOT gate. The input is always changed to its opposite. If the input is 0, the NOT gate will give its ***complement,*** or opposite, which is 1. If the input to the NOT gate is a 1, the circuit will complement it to give a 0**.** This inverting is also called ***complementing*** or ***negating.*** The terms negating, complementing, and inverting all mean the same thing.



(a)

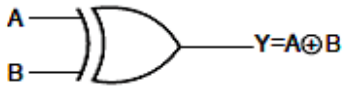
X	Y
0	1
1	0

(b)

Fig.4.5 (a) Symbol of NOT gate (b) Truth table of NOT gate

XOR (EXCLUSIVE-OR) Gate

The EXCLUSIVE-OR gate, commonly written as XOR gate, is a two-input, one-output gate. Figures 4.6 (a) and (b) respectively show the logic symbol and truth table of a two-input XOR gate. As can be seen from the truth table, the output of an XOR gate is a logic '1' when the inputs are unlike and a logic '0' when the inputs are like. The output of a multiple-input XOR logic function is logic '1' when the number of 1s in the input sequence is odd and logic '0' when the number of 1s in the input sequence is even, including zero.



(a)

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

(b)

Fig.4.6 (a) Symbol of two input XOR gate (b) Truth table of two input XOR gate

The output of a two-input XOR gate is expressed by

$$Y = (A \oplus B) = \overline{A}B + A\overline{B}$$

The truth table is similar to the OR truth table except that, when both inputs are **1,** the **XOR** gate generates a 0. The **XOR** gate is enabled ***only when an odd number*** of *1s* ***appear at the inputs.*** Lines 2 and **3** of the truth table have odd numbers of **1s,** and therefore the output is enabled with a 1. Lines **1** and **4** of the truth table contain even

numbers (0, 2) of **1s,** and therefore the **XOR** gate is disabled and a 0 appears at the output. The XOR gate could be referred to as an odd-bits check circuit. Figure 4.6 shows the logic circuit of XOR gate using AND, OR and NOT gates.

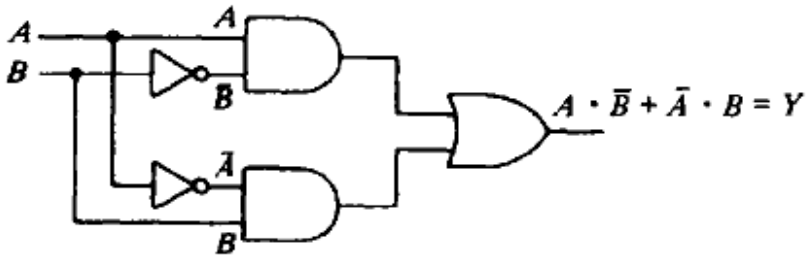
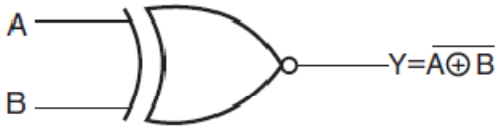


Fig 4.7. The logic circuit that performs XOR operation.

EXCLUSIVE-NOR Gate

EXCLUSIVE-NOR (commonly written as EX-NOR) means NOT of EX-OR, i.e. the logic gate that we get by complementing the output of an EX-OR gate. Figure 4.8 shows its logic symbol along with its truth table. The truth table of an EX-NOR gate is obtained from the truth table of an EX-OR gate by complementing the output entries. Logically,

$$Y = \overline{(A \oplus B)} = \overline{(A.B + \bar{A}.\bar{B})}$$



(a)

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

(b)

Fig 4.8 (a) Logic symbol of a two-input EXCLUSIVE-NOR gate and (b) the truth table of a two-input EXCLUSIVE-NOR gate.

The output of a two-input EX-NOR gate is logic '1' when the inputs are like and logic '0' when they are unlike. In general, the output of a multiple-input EX-NOR logic function is a logic '0' when the number of 1s in the input sequence is odd and a logic '1' when the number of 1s in the input sequence is even including zero. That is, an all 0s input sequence also produces a logic '1' at the output.

4.2.3. Universal gates

OR, AND and NOT gates are the three basic logic gates as they together can be used to construct the logic circuit for any given Boolean expression. NOR and NAND gates have the property that they individually can be used to hardware-implement a logic circuit corresponding to any given Boolean expression. That is, it is possible to use either only NAND gates or only NOR gates to implement any Boolean expression. This is so because a combination of NAND gates or a combination of NOR gates can be used to perform functions of any of the basic logic gates. For this reason the **NAND** and **NOR** gates are called **universal gates**. The use of universal gate minimizes the number of different gates in a logic circuit.

NAND Gate

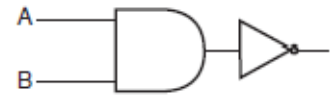
NAND stands for NOT AND. An AND gate followed by a NOT circuit makes it a NAND gate as shown in Fig 4.9(a). Fig 4.9(b) shows the logic symbol of a two-input NAND gate. The truth table of a NAND gate is obtained from the truth table of an AND gate by complementing the output entries as shown in Fig.4.9(c). The output of a NAND gate is logic '0' when all its inputs are logic '1'. For all other input combinations, the output is logic '1'. NAND gate operation is logically expressed as

$$Y = \overline{A.B}$$

In general, the Boolean expression for a NAND gate with more than two inputs can be written as

$$Y = \overline{(A.B.C.D...)}$$

The NAND symbol is an AND symbol with a small bubble at the output. The bubble is sometimes called an *invert bubble.* The invert bubble provides a simplified method of representing the NOT gate.



(a)

(b)

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

(c)

Fig.4.9 (a) NAND implementation using NOT with AND (b) Logic symbol (c) truth table of NAND gate

NOR Gate

NOR stands for NOT OR. An OR gate followed by a NOT circuit makes it a NOR gate Fig. 4.10(a) shows the implementation of NOR using OR and NOT gates. The truth table of a NOR gate is obtained from the truth table of an OR gate by complementing the output values. The output of a NOR gate is a logic '1' when all its inputs are logic '0'. For all other input combinations, the output is logic '0'. The output of a two-input NOR gate is logically expressed as

$$Y = \overline{(A + B)}$$

In general, the Boolean expression for a NOR gate with more than two inputs can be written as

$$Y = \overline{(A + B + C + D...)}$$

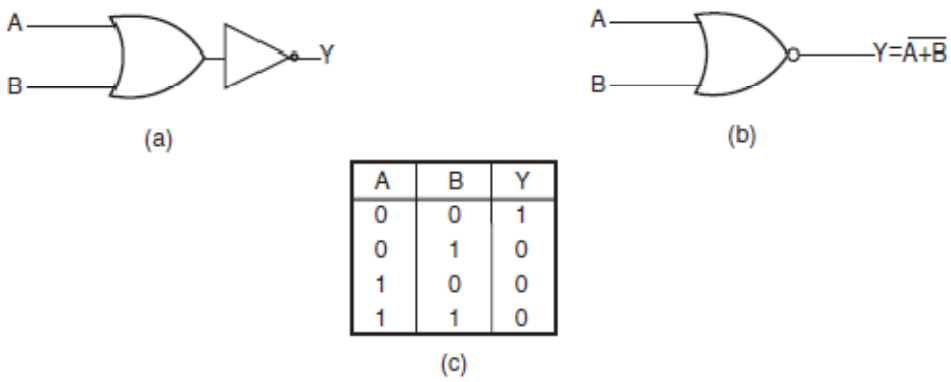
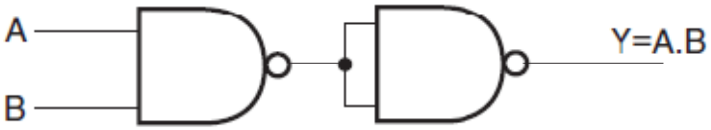


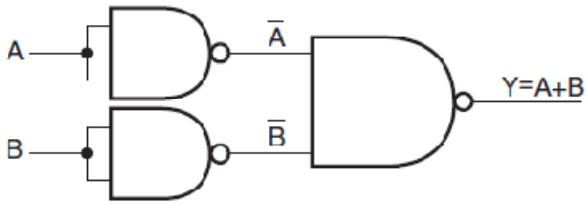
Fig.4.10 (a) Two-input NOR implementation using an OR gate (b) Symbol of two-input NOR gate and (c) Truth table of two-input NOR gate.

NAND Gate as universal gate

(a) NOT gate using NAND



(b) AND gate using NAND



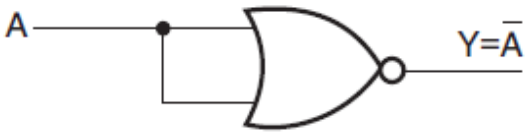
(c) OR gate using NAND

Figure 4.11 shows the implementation of basic logic gates (a) NOT (b) AND (c) OR using only NAND gates.

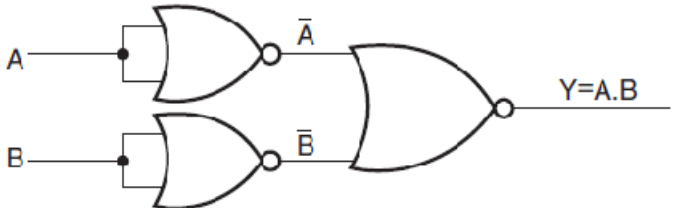
As an illustration, Fig. 4.11 shows how two-input NAND gates can be used to construct a NOT circuit, a two-input AND gate and a two-input OR gate.

NOR Gate as universal gate

The following Fig.4.12 shows the implementation of basic gates using NOR.



(a) NOT gate using NOR



(b) AND gate using NOR

(c) OR gate using NOR

Figure 4.12. Implementation of basic logic gates (a) NOT (b) AND (c) OR using only NOR gates.

4.3 Boolean Algebra

Introduction

Boolean algebra is mathematics of logic. It is one of the most basic tools available to the logic designer and can be used for simplification of complex logic expressions.

An English mathematician, George Boole, introduced the idea of examining the truth or falsehood of language statements through a special algebra of logic. His work was published in 1854, in a book entitled ***"An Investigation of the Laws of Thought***". Boole's algebra was applied to statements that are either completely correct or completely false. A value 1 is assigned to those statements that are completely correct and a value 0 is assigned to statements that are completely false. As these statements are given numerical values 1 or 0, they are referred to as digital variables. In digital systems, the words switching variables, logical variables, and digital variables are used interchangeably. Boole's algebra is referred to as Boolean algebra. Originally Boolean algebra was applied to establish the **validity** or **falsehood** of logical statements.

In 1938, Claude Shannon of Department of Electrical Engineering at Massachusetts Institute of Technology in (his master's thesis) provided the first applications of the principles of Boolean algebra to the design of electrical switching circuits. The title of the paper, which was an abstract of his thesis, is “A Symbolic Analysis of Relay and Switching Circuits”. Shannon established Boole's algebra to switching circuits is what ordinary algebra is to analogue circuits. Logic designers of today use Boolean algebra to functionally design a large variety of electronic equipment such as

- Hand-held calculators
- Traffic light controllers
- Personal computers
- Super computers
- Communication systems
- Aerospace equipment etc.

Boolean operator or an expression of George Boole’s(1847) algebra

Boolean variable or signal can assume only two values: TRUE or FALSE. This concept has been ported in the field of electronic circuits by Claude Shannon (1938). He had the idea to use the Boole’s algebra for coding the status of circuit: TRUE/FALSE as HIGH/LOW as CLOSE/OPEN, etc.

Boolean expression: An expression of the Boole’s algebra, in which Boolean variables/signals and Boolean operators can appear. Boolean expressions are used for describing the behavior of digital equipments or stating properties/conditions in programs.

Boolean function: A binary function of binary variables.

Boolean logic: The set of rules for logical operations on binary numbers.

Boolean operator: The classical Boolean operators are AND, OR, NOT. Other operators such as XOR, NAND, NOR, etc., can be easily obtained based on the fundamental ones. In hardware these are implemented with gates, see for example AND gate.

In Boolean algebra as applied to the switching circuits, all variables and relations are two-valued. The two values are normally chosen as 0 and 1, with 0 representing *false* and 1 representing *true*. If x is a Boolean variable, then x = 1 means x is true x = 0 means x is false.

When we apply Boolean algebra to digital circuits we will find that the qualifications “*asserted”* and “*not-asserted”* are better names than “true” and “false”. That is when x = 1 we say x is asserted, and when x = 0 we say x is not-asserted. You are expected to be familiar with

- Concept of a set
- Meaning of equivalence relation
- The principle of substitution

Boolean algebra

Digital circuits perform the binary arithmetic operations with binary digits 1 and 0. These operations are called logic functions or logical operations. *The algebra used to symbolically describe logic functions is called* **Boolean algebra.** Boolean algebra is a set of rules and theorems by which logical operations can be expressed symbolically in equation form and be manipulated mathematically. As with the ordinary algebra, the *letters of alphabet (*e.g. A*, *B*, *C* etc.) can be used to represent the variables. Boolean algebra differs from ordinary algebra in that Boolean constants and variables can have only two values ; 0 and 1. There are four connecting symbols used in Boolean algebra *viz*.

(*i*) equals sign (=) **(*ii*)** plus sign (+)
(*iii*) multiply sign (·) **(*iv*)** bar (–)

(*i*) Equals sign (=). The equals sign in Boolean algebra refers to the standard mathematical equality. In other words, the logical value on one side of the sign is identical to the logical value on the other side of the sign. Suppose we are given two logical variables such that $A = B$. Then if $A = 1$, then $B = 1$ and if $A = 0$, then $B = 0$.

(*ii*) Plus sign (+). The plus sign in Boolean algebra refers to the logical *OR operation*. If the statement $A + B = 1$ appears in Boolean algebra, it means A ORed with B equals 1. Consequently, either $A = 1$ or $B = 1$ or both equal 1.

(*iii*) Multiply sign (·). The multiply sign in Boolean algebra refers to *AND operation*. When the statement $A \cdot B = 1$ appears in Boolean algebra, it means A ANDed with B equals 1. Consequently, $A = 1$ and $B = 1$. The function $A \cdot B$ is often written as AB, omitting the dot for convenience.

(*iv*) Bar sign (–). The bar sign in Boolean algebra refers to *NOT operation*. The NOT has the effect of inverting (complementing) the logical value. Thus, if $A = 1$, then $\overline{A} = 0$.

4.3.1 Basic Laws of Boolean algebra

Boolean Theorems

Basic laws of Boolean algebra are useful in manipulating and simplifying Boolean expressions. These laws or theorems can be divided into two groups:

(*i*) Single variable theorems
(*ii*) Multivariable theorems

(*i*) Single variable theorems. These theorems refer to the condition when only one input to the logic gate is variable. The following 9 theorems are single variable Boolean theorems.

Theorem 1: $A + 0 = A$
Theorem 2: $A \cdot 1 = A$
Theorem 3: $A + A = 1$
Theorem 4: $A \cdot A = 0$
Theorem 5: $A + A = A$

Theorem 6: $A \cdot A = A$
Theorem 7: $A + 1 = 1$
Theorem 8: $A \cdot 0 = 0$

Theorem 9: $\overline{\overline{A}} = A$

(*ii*) Multivariable theorems. These theorems refer to the condition when more than one input to the logic gate is variable. The following theorems from 10 to 18 are multivariable Boolean theorems.

Theorem 10	:	$A + B = B + A$	*Commutative Law*
Theorem 11	:	$A \cdot B = B \cdot A$	
Theorem 12	:	$A + (B + C) = (A + B) + C$	*Associative Law*
Theorem 13	:	$A \cdot (B \cdot C) = (A \cdot B) \cdot C$	
Theorem 14	:	$A \cdot (B + C) = A \cdot B + A \cdot C$	*Distributive Law*
Theorem 15	:	$(A + B) \cdot (C + D) = A \cdot C + B \cdot C + A \cdot D + B \cdot D$	
Theorem 16	:	$A + A \cdot B = A$	
Theorem 17	:	$\overline{(A + B)} = \overline{A} \cdot \overline{B}$	*De Morgan's Theorems*
Theorem 18	:	$\overline{(A \cdot B)} = \overline{A} + \overline{B}$	

Commutative law: *This law states that the order in which the variables are ORed or ANDed makes no difference.* Theorems 10 and 11 obey this law.

Theorem 10: $A + B = B + A$
Theorem 11: $A \cdot B = B \cdot A$

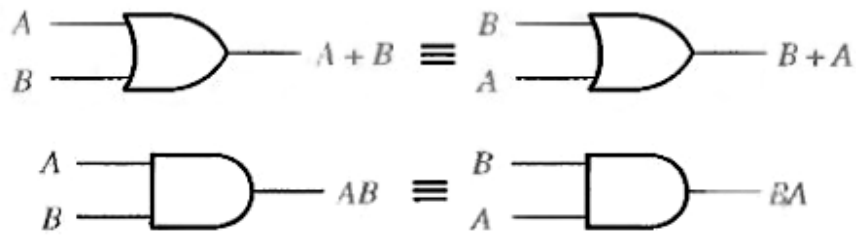


Fig. 4.13

Associative law: *This law states that in the ORing or ANDing of several variables, the result is the same regardless of the grouping of the variables.* Theorems 12 and 13 obey associative law.

Theorem 12: $A + (B + C) = (A + B) + C$
Theorem 13: $A \cdot (B \cdot C) = (A \cdot B) \cdot C$

Distributive law: *This law states that a Boolean expression can be expanded by multiplying term-by-term just the same as in ordinary algebra.* Theorems 14 and 15 obey **distributive law**.

Theorem 14: $A \cdot (B + C) = A \cdot B + A \cdot C$

Theorem 15: $(A + B) \cdot (C + D) = A \cdot C + B \cdot C + A \cdot D + B \cdot D$

Theorem 16: $A + A \cdot B = A$

Theorem 16 can be proved by factoring and using Theorems 2, 7, 10 and 14.
$A + A \cdot B = A \cdot 1 + A \cdot B$ ...Theorem 2
$= A \cdot (1 + B)$ ...Theorem 14
$= A \cdot (B + 1)$ ...Theorem 10
$= A \cdot 1$ ...Theorem 7
$= A$ ...Theorem 2

Theorem 17: $\overline{(A + B)} = \overline{A} \cdot \overline{B}$

Theorem 18: $\overline{(A \cdot B)} = \overline{A} + \overline{B}$

Theorems 17 and 18 are the two most important theorems of Boolean algebra and were contributed by the great mathematician named ***De Morgan***. Therefore, these theorems are called DeMorgan's theorems.

4.3.2. De Morgan's theorem

De Morgan's theorems are extremely useful in simplifying expressions in which a product or sum of variables is inverted. The two theorems are:

(*i*) $\overline{(A + B)} = \overline{A} \cdot \overline{B}$

(*ii*) $\overline{(A \cdot B)} = \overline{A} + \overline{B}$

(*i*) The first De Morgan's theorem may be stated as under:

When the OR sum of two variables is inverted, this is equal to inverting each variable individually and then ANDing these inverted variables i.e.,

$$\overline{(A + B)} = \overline{A} \,.\, \overline{B}$$

In this expression, *A* and *B* are the two variables. The L.H.S. is the complement of the OR sum of the two variables. The R.H.S. is the AND product of individual inverted variables.

"According to the first theorem the complement of a sum equals the product of complements"

A	B	A+B	$\overline{A+B}$	$\overline{A}$	$\overline{B}$	$\overline{A} \,.\, \overline{B}$
0	0	0	1	1	1	1
0	1	1	0	1	0	0
1	0	1	0	0	1	0
1	1	1	0	0	0	0

(*ii*) The second De Morgan's theorem may be stated as under:

When the AND product of two variables is inverted, this is equal to inverting each variable individually and then ORing them i.e.,

$$\overline{(A.B)} = \overline{A} + \overline{B}$$

In this expression, *A* and *B* are the two variables. The L.H.S. is the complement of the AND product of the two variables. The R.H.S. is the OR sum of the individual inverted variables.

"According to the second theorem the complement of a product equals the sum of complements"

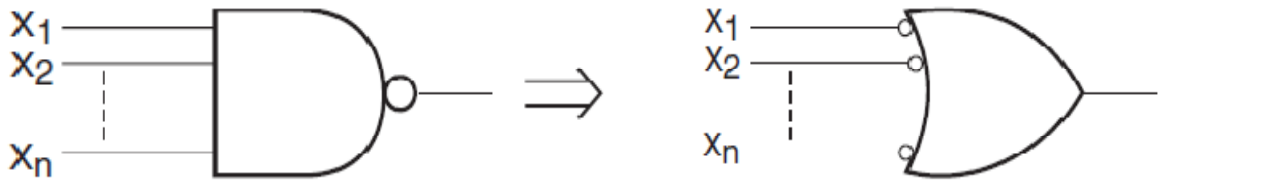
A	B	A.B	$\overline{A.B}$	$\overline{A}$	$\overline{B}$	$\overline{A} + \overline{B}$
0	0	0	1	1	1	1
0	1	0	1	1	0	1
1	0	0	1	0	1	1
1	1	1	0	0	0	0

Proofs

DeMorgan's theorem can be proved as follows. Let us assume that all variables are in a logic '0'
state. In that case

$$\text{LHS} = [\overline{X_1 + X_2 + X_3 + \cdots + X_n}] = [\overline{0+0+0+\cdots+0}] = \overline{0} = 1$$

$$\text{RHS} = \overline{X_1}.\overline{X_2}.\overline{X_3}.\ldots.\overline{X_n} = \overline{0}.\overline{0}.\overline{0}.\ldots.\overline{0} = 1.1.1.\ldots.1 = 1$$



(b)

(a)

Fig. 4.14

Therefore, LHS = RHS.

Now, let us assume that any one of the n variables, say X1, is in a logic HIGH state:

Therefore, again LHS = RHS.
The same holds good when more than one or all the variables are in the logic '1' state. Therefore, theorem (i) stands proved. Since theorem (ii) is the dual of theorem (i), the same also stands proved.

DeMorgan's law

- bridges the AND and OR operations
- establishes a method for converting one form of a Boolean function into another
- allows the formation of complements of expressions with more than one variable
- can be extended to expressions of any number of variables through substitution

4.3.3 Duality theorem

Duality Principle is an important property of Boolean algebra. It is stated below:

The duality principle states that a Boolean expression remains valid if operators OR and AND are interchanged and 1's and 0's in the expression are also interchanged.

That is from one Boolean expression to another expression can be derived by

- Changing each OR operation with AND operation.
- Changing each AND operation with OR operation.
- Complementing any 0 to 1 and 1 to 0 in the expression.

The dual of a Boolean expression is obtained by replacing all '.' operations with '+' operations, all '+' operations with '.' operations, all 0s with 1s and all 1s with 0s and leaving all literals unchanged. The examples below give some Boolean expressions and the corresponding dual expressions:

For the given Boolean expressions

$$\overline{A}.B + A.\overline{B}$$

$$(A + B).(\overline{A} + \overline{B})$$

Corresponding duals are

$$(\overline{A} + B).(A + \overline{B})$$

$$A.B + \overline{A}.\overline{B}$$

In order to understand this principle, consider the Boolean Theorem 1

$A + 0 = A$

According to duality principle, this Boolean expression remains valid if OR function is replaced by AND function and 0 by 1. In that case, the Boolean expression becomes:

$A \cdot 1 = A$

Note that this is Boolean Theorem No. 2. Therefore, Boolean Theorem 2 is dual of Boolean Theorem 1 and *vice-versa*. Applying duality principle, Theorem 4 is dual of Theorem 3 and *vice-versa,* Theorem 6 is dual of Theorem 5 and *vice-versa*, Theorem 8 is dual of Theorem 7 and *vice-versa*. To apply duality principle to a Boolean expression, we simply interchange OR and AND operator and replace 1's by 0's and 0's by 1's.

Useful Identities of Boolean algebra

Complementation	$x.\bar{x} = 0$
	$x + \bar{x} = 1$
0 - 1 law	$x.0 = 0$
	$x+1 = 1$
	$x+0 = x$
	$x.1 = x$
Idempotency	$x.x = x$
	$x+x = x$
Involution	$\bar{\bar{x}} = x$
Commutative law	$x \cdot y = y \cdot x$
	$x + y = y + x$
Associative law	$(x \cdot y).z = x.(y.z)$
	$(x + y) + z = x + (y+z)$
Distributive law	$x + (y.z) = (x+y).(x+z)$
	$x.(y+z) = x.y + x.z$
Adjacency law	$x.y + x.\bar{y} = x$
	$(x + y).(x + \bar{y}) = x$
Absorption law	$x + x \cdot y = x$
	$x \cdot (x+y) = x$
	$x + \bar{x}.y = x + y$
	$x.(\bar{x} + y) = x.y$
Consensus law	$x.y + \bar{x}.z + y.z = x.y + \bar{x}.z$
	$(x + y).(\bar{x} + z).(y + z) = (x + y).(\bar{x} + z)$
DeMorgan's law	$\overline{x + y} = \bar{x}.\bar{y}$
	$\overline{x.y} = \bar{x} + \bar{y}$

Basic Laws of Boolean algebra

Definition: A Boolean algebra consists of a finite set of elements S.

• Equivalence relation "=",
• One unary operator “not” (symbolized by an over bar),
• Two binary operators "." and "+",
• For every element x and y ∈ S the operations x (not x), x.y and x +y are uniquely defined.

The unary operator ‘*not*’ is defined by the relation
Not of 1= 0; not of 0 = 1. The *not* operator is also called the **complement**, and consequently $\overline{x}$ is the complement of x.

The binary operator ‘*and*’ is symbolized by a dot. The ‘*and*’ operator is defined by the relations
0 . 0 = 0
0 . 1 = 0
1 . 0 = 0
1 . 1 = 1
The binary operator ‘or’ is represented by a plus (+) sign. The ‘or’ operator is defined by the relations
0 + 0 = 0
0 + 1 = 1
1 + 0 = 1
1 + 1 = 1

Huntington's postulates apply to the Boolean operations

Postulates

A + 0 = A
A + 1 = 1
A . (B + C)= A.B + A.C
A + A = 1
A . 0 = 0
A . 1 = A
A + (B . C) = (A+B) . (A+C)
A . A = 0

Theorems

A + A = A
A + A = 1
A . A = A
A . A = 0

Examples:

1. $1.1 = 1, 0+0 = 0.$
2. $1.0 = 0.1 = 0, 0+1 = 1+0 = 1.$
3. $0.0 = 0, 1+1 = 1.$
4. $\overline{1} = 0$ and $\overline{0} = 1.$

4.3.4 Simplification of logical equations using Boolean laws

The form of Boolean expression determines how many and which types of logic gates are needed as well as how they are connected together. For the more complicated Boolean expression, the logic circuit will also be complex. It is desirable to simplify an expression as much as possible to get the simplest logic circuit. Note that the new expression can be used to implement a logic circuit that is equivalent to the original logic circuit but contains fewer gates and connections.

The application of laws and theorems of Boolean algebra can be used for simplifying or minimizing a given complex Boolean expression. The primary objective of all simplification procedures is to obtain an expression that has the minimum number of terms. If there is more than one possible solution with the same number of terms, the one having the minimum number of literals is the choice. The given Boolean expression will be in either of the two forms: **sum-of-products** and **product-of-sums.** The objective will be to find a minimized expression in the same or the other form.

While simplifying a Boolean expression, the following two steps may be very helpful:

(*i*) Put the original expression into the sum-of-products form by the repeated use of rules, theorems and techniques of Boolean algebra.
(*ii*) Once it is in this form, the product terms are checked for common factors and factoring is performed wherever possible.

Illustration

Fig. 4.15 shows the logic circuit. The Boolean expression for this circuit is

$$X = AC\overline{D} + \overline{A}B\,(CD + BC)$$

We require *five AND gates*, *two OR gates* and *two inverters* to implement this expression. In all, nine gates are needed. We shall now use laws, rules and techniques of Boolean algebra to get the simplest expression for the given function.

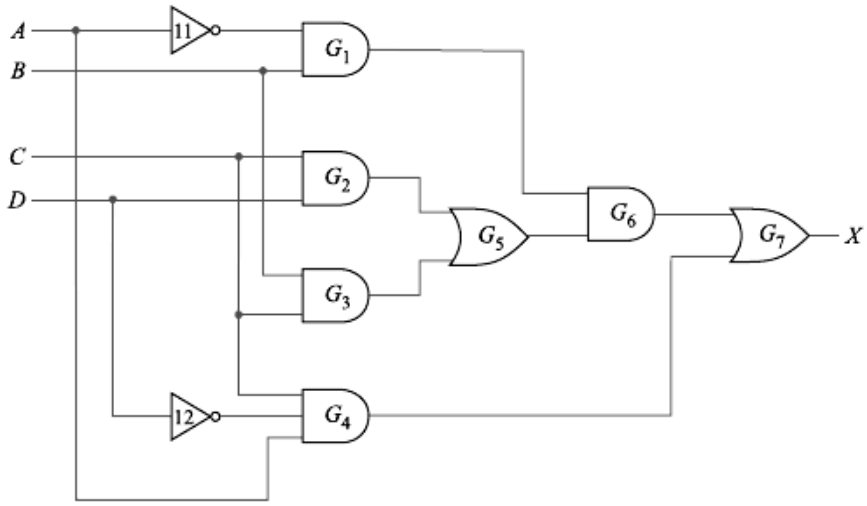


Fig. 4.15

Step 1. Apply distributive law to the second term by multiplying the term $CD + BC$ by $\bar{A}B$. The result is :

$$X = AC\bar{D} + \bar{A}BCD + \bar{A}BBC$$

Step 2. Applying the rule $BB = B$ to the third term, we have,

$$X = AC\bar{D} + \bar{A}BCD + \bar{A}BC$$

Step 3. Note that C is common to every term so that it can be factored out using distributive law.

$$\therefore \quad X = C(A\bar{D} + \bar{A}BD + \bar{A}B)$$

The Fig.4.16 shows the logic circuit for the simplified logical expression.

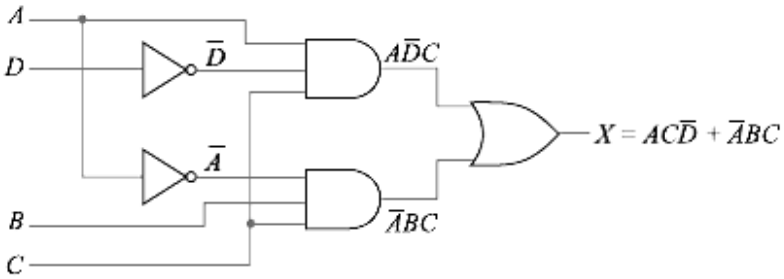


Fig. 4.16

Example 1

Using Boolean techniques, simplify the following expression :

$$Y = AB + A(B + C) + B(B + C)$$

Solution. $Y = AB + A(B + C) + B(B + C)$

Step 1 : Apply Theorem 14 (distributive law) to second and third terms:

$$Y = AB + AB + AC + BB + BC$$

Step 2 : Apply Theorem 6 ($B \cdot B = B$) :

$$Y = AB + AB + AC + B + BC$$

Step 3 : Apply Theorem 5 ($AB + AB = AB$) :

$$Y = AB + AC + B + BC$$

Step 4 : Factor B out of last 2 terms :

$$Y = AB + AC + B(1 + C)$$

Step 5 : Apply commutative law and Theorem 7 ($1 + C = C + 1 = 1$) :

$$Y = AB + AC + B \cdot 1$$

Step 6 : Apply Theorem 2 ($B \cdot 1 = B$) :

$$Y = AB + AC + B$$

Step 7 : Factor B out of first and third terms :

$$Y = B(A + 1) + AC$$

Step 8 : Apply Theorem 7 ($A + 1 = 1$) :

$$Y = B \cdot 1 + AC$$

Step 9 : Apply Theorem 2 ($B \cdot 1 = B$) :

$$Y = B + AC$$

Example 2

Using Boolean algebraic techniques, simplify the following expression

$$Y = A \cdot B \cdot \overline{C} \cdot \overline{D} + \overline{A} \cdot B \cdot \overline{C} \cdot \overline{D} + \overline{A} \cdot B \cdot C \cdot \overline{D} + A \cdot B \cdot C \cdot \overline{D}$$

$$Y = A \cdot B \cdot \overline{C} \cdot \overline{D} + \overline{A} \cdot B \cdot \overline{C} \cdot \overline{D} + \overline{A} \cdot B \cdot C \cdot \overline{D} + A \cdot B \cdot C \cdot \overline{D}$$

Solution. $Y = A \cdot B \cdot \overline{C} \cdot \overline{D} + \overline{A} \cdot B \cdot \overline{C} \cdot \overline{D} + \overline{A} \cdot B \cdot C \cdot \overline{D} + A \cdot B \cdot C \cdot$

Step 1 : Take out the common factors as below :

$$Y = B\,\overline{C}\,\overline{D}(A + \overline{A}) + B\,C\,\overline{D}(A + \overline{A})$$

Step 2 : Apply Theorem 3 $(A + \overline{A} = 1)$:

$$Y = B\,\overline{C}\,\overline{D} + B\,C\,\overline{D}$$

Step 3 : Again factorise :

$$Y = B\,\overline{D}(C + \overline{C})$$

Step 4 : Apply Theorem 3 $(C + \overline{C} = 1)$:

$$Y = B\,\overline{D} \cdot 1 = B\overline{D}$$

Example 3

Simplify the following Boolean expressions to a minimum number of literals.

(*i*) $Y = A + \overline{A}B$ (*ii*) $Y = AB + \overline{A}C + BC$

Solution. (*i*) $Y = A + \overline{A}B$

$= A + AB + \overline{A}B$ [$\because A = A + AB$ from Theorem 16]

$= A + B(A + \overline{A})$

$= A + B$ [$\because A + \overline{A} = 1$ from Theorem 3]

$\therefore Y = A + B$

(*ii*) $Y = AB + \overline{A}C + BC$

$= AB + \overline{A}C + BC \cdot (A + \overline{A})$

$= AB + \overline{A}C + ABC + \overline{A}BC$

$= AB(1 + C) + \overline{A}C\ (1 + B)$

$= AB + \overline{A}C$

$\therefore Y = AB + \overline{A}C$

Example 4

Determine the output expression for the circuit shown below and simplify it using De Morgan's theorem

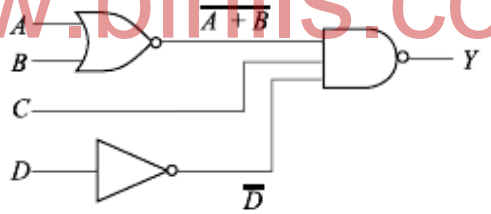


Fig. 4.17

Solution. The output expression for the circuit shown above is :

$$Y = [\overline{(\overline{A+B}) \cdot C \cdot \overline{D}}]$$

Using De Morgan's theorem :

$$Y = (A + B) + \overline{C} + D$$

$$\therefore Y = A + B + \overline{C} + D$$

Example 5

Simplify the following Boolean expressions

(*i*) $Y = (A + B + C) \cdot (A + B)$

(*ii*) $Y = AB + ABC + AB\overline{C}$

(*iii*) $Y = 1 + A(B \cdot \overline{C} + BC + \overline{B}\,\overline{C}) + A\overline{B}C + AC$

(*iv*) $Y = \overline{(A + \overline{B} + C) + (B + \overline{C})}$

Solution. (*i*) $Y = (A+B+C)\cdot(A+B)$

$= A\cdot A + A\cdot B + B\cdot A + B\cdot B + C\cdot A + C\cdot B$

Using $A\cdot A = A$, we get,

$Y = A + AB + AB + B + AC + BC$

$= A + AB + B + AC + BC \quad [\because AB + AB = AB]$

$= A + B + AC + BC \quad [\because A + AB = A]$

$= A(1+C) + B(1+C)$

$= A\cdot 1 + B\cdot 1 \quad [\because 1 + C = 1]$

$\therefore \quad Y = A + B$

(*ii*) $Y = AB + ABC + AB\overline{C}$

$= AB + AB\,(C + \overline{C})$

$= AB + AB \quad [\because C + \overline{C} = 1]$

$\therefore \quad Y = AB$

(*iii*) $Y = 1 + A(B\cdot\overline{C} + BC + \overline{B}\,\overline{C}) + A\overline{B}C + AC$

Using $1 + A = 1$, we get,

$Y = 1 + A\overline{B}C + AC \quad [\because 1 + A(B\overline{C} + BC + \overline{B}\,\overline{C}) = 1]$

$= 1 + AC$

$\therefore \quad Y = 1$

Thus, because of the first term Y reduces to 1. Therefore, any Boolean expression ORed with 1, results in 1.

(*iv*) $Y = \overline{(A+\overline{B}+C)\cdot(B+\overline{C})}$

Applying De Morgan's theorem :

$Y = \overline{(A+\overline{B}+C)}\cdot\overline{(B+\overline{C})}$

Again applying De Morgan's theorem :

$Y = (\overline{A}\cdot B\cdot\overline{C})\cdot(\overline{B}\cdot C) = 0 \quad [\because B\cdot\overline{B} = 0,\ C\cdot\overline{C} = 0]$

Example 6

Simplify the following Boolean expressions.

$Y = A\overline{B}D + A\overline{B}\,\overline{D}$

Solution. $Y = A\overline{B}D + A\overline{B}\,\overline{D}$

Factoring out the common variables $A\overline{B}$ (using Theorem 14), we get ,

$Y = A\overline{B}(D + \overline{D})$

Using Theorem 3, $D + \overline{D} = 1$.

$\therefore \quad Y = A\overline{B}\cdot 1$

Using Theorem 2, we get,

$Y = A\overline{B}$

Example 7

Simplify the following Boolean expression

$Y = (\overline{A} + B)(A + B)$

Solution. $Y = (\overline{A} + B)(A + B)$

The expression can be expanded by multiplying out the terms [Theorem 15].

$$Y = \overline{A} \cdot A + \overline{A} \cdot B + B \cdot A + B \cdot B$$

Using Theorem 4, $\overline{A} \cdot A = 0$. Also $B \cdot B = B$ [Theorem 6].

$$\therefore \quad Y = 0 + \overline{A} \cdot B + B \cdot A + B$$

$$= \overline{A} \cdot B + AB + B$$

Factoring out the variable B [Theorem 14], we have,

$$Y = B(\overline{A} + A + 1)$$

Using Theorem 7, $A + 1 = 1$.

$$\therefore \quad Y = B(\overline{A} + 1)$$

Again using Theorem 7, $\overline{A} + 1 = 1$.

$$\therefore \quad Y = B \cdot 1$$

Finally, using Theorem 2, we have,

$$Y = B$$

Example 8

Simplify the expression :

$$X = \overline{A}\overline{B}C + A\overline{B}C + AB\overline{C} + ABC$$

Solution.

$$X = \overline{A}\overline{B}C + A\overline{B}C + AB\overline{C} + ABC$$

Step 1. Note that the first two terms have $\overline{B}C$ as common factors while the last two terms have AB as common factors.

$$\therefore \quad X = \overline{B}C(A + \overline{A}) + AB(C + \overline{C})$$

Step 2. $A + \overline{A} = 1$ and $C + \overline{C} = 1$ so that :

$$X = \overline{B}C \cdot 1 + AB \cdot 1$$

Step 3. Since $\overline{B}C \cdot 1 = \overline{B}C$ and $AB \cdot 1 = AB$ so that :

$$X = AB + \overline{B}C$$

Example 9

Simplify the expression :

$$X = AB + A(B + C) + B(B + C)$$

Solution.

$$X = AB + A(B + C) + B(B + C)$$

Step 1. Applying distributive law to the second and third terms, we have,

$$X = AB + AB + AC + BB + BC$$

Step 2. Now $BB = B$ and $AB + AB = AB$ so that :

$$X = AB + AC + B + BC$$

Step 3. $B + BC = B(1 + C) = B \cdot 1 = B$

$\therefore$ $X = AB + AC + B$

Step 4. Factoring B out, we have,

$$X = B(A + 1) + AC$$

Step 5. $A + 1 = 1$ so that $B(A + 1) = B \cdot 1 = B$.

$\therefore$ $X = B + AC$

Example 10

Simplify the following circuit

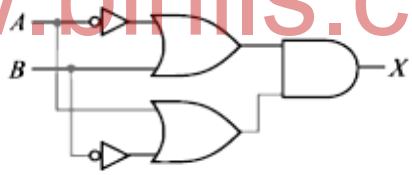


Fig. 4.18

The Boolean expression for the above circuit shown in Fig. 4.18 is

$$X = (\overline{A} + B)(A + \overline{B})$$

Step 1. Multiplying out to get the sum-of-products form, we have,

$$X = \overline{A}A + \overline{A}\overline{B} + BA + B\overline{B}$$

Step 2. Now $\overline{A}A = 0$ and $B\overline{B} = 0$ so that :

$$X = \overline{A}\overline{B} + AB$$

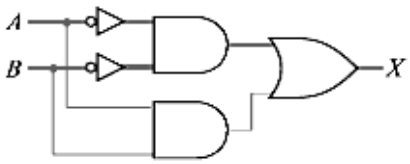


Fig. 4.19

This expression is implemented in Fig.4.19. If you compare the circuit with the original circuit, you see that both circuits contain the same number of gates and connections. *Therefore, the simplification process has not produced a simpler circuit but it has produced an alternative circuit.*

4.3.5 Karnaugh's Map

M. Karnaugh introduced (1953) a map to pictorially represent a logical expression. It is known as Karnaugh Map abbreviated as K-map. K-Map is a pictorial form of the truth-table. A Karnaugh map provides a systematic method for simplifying Boolean expressions and will produce the simplest Sum-Of-Products (SOP) or Product-Of-Sums (POS) expression possible, known as the minimum expression. The effectiveness of algebraic simplification depends on the use of laws, rules, and theorems of Boolean algebra and on your ability to apply them.

A Karnaugh map is similar to a truth table because it presents all of the possible values of input variables and the resulting output for each value. Instead of being organized into columns and rows like a truth table, the Karnaugh map is an array of cells in which each cell represents a binary value of the input variables. The cells are arranged in a way so that simplification of a given expression is simply a matter of properly grouping the cells. Karnaugh maps can be used for expressions with two, three, four and five variables. Another method, called the Quine-McClusky method can be used for higher numbers of variables. The number of cells in a Karnaugh map is equal to the total number of possible input variable combinations as is the number of rows in a truth table. For two variables, the number of cells is 2^2=4, for three variables, the number of cells is 2^3 = 8.

Cell Adjacency

The cells in a Karnaugh map are arranged so that there is only a single variable change between adjacent cells. Adjacency is defined by a single variable change. In the 3-variable map the 010 cell is adjacent to the 000 cell, the 011 cell, and the 110 cell. The 010 cell is not adjacent to the 001 cell, the 111 cell, the 100 cell, or the 101 cell. The cells in the top and bottom rows are adjacent and cells in the first column and the last column are adjacent. Binary representations for the numbers of two adjacent squares differ in exactly one position.

Two variables K-Map

The arrangement of cells for two variables K-Map is shown in Fig.4.20. Two variables are written in their normal (logic 1) and complemented (logic 0) forms. There are 4 cells in a two variable map.

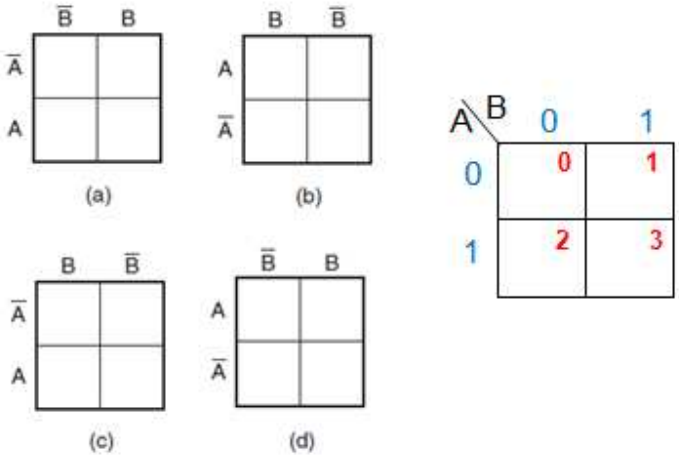
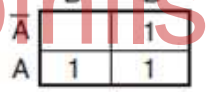


Fig. 4.20 Arrangement of cells in a two variable K-Map

The Fig. 4.21 shows the sum-of-product K-Map for the sample truth table.

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1



Sum-of-products K-map

Fig. 4.21 Two variable Karnaugh Map for the given truth table

The arrangement of cells for three variables K-Map is shown in Fig.4.22.

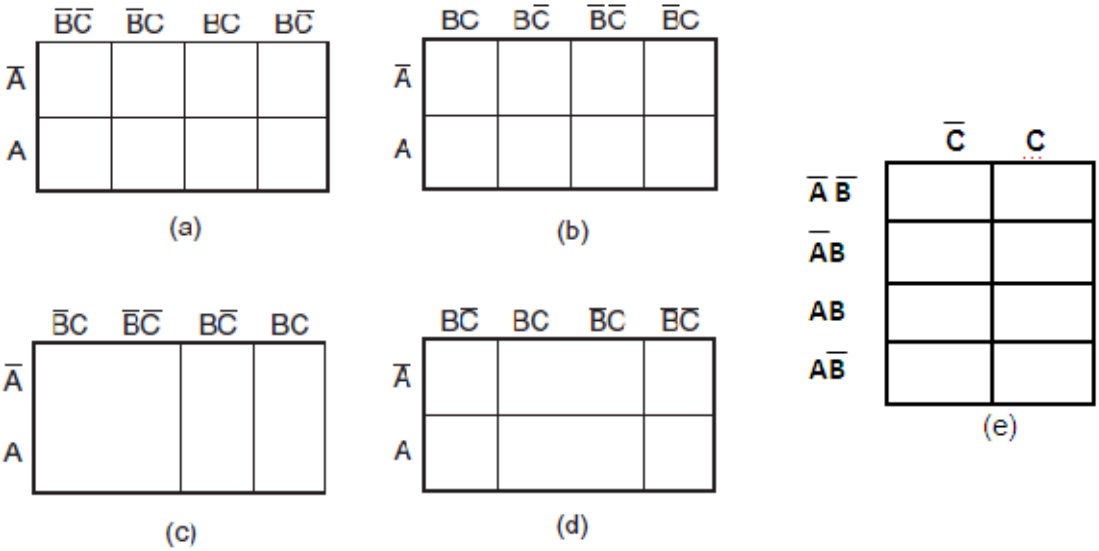


Fig. 4.22 Arrangement of cells in a three variable K-Map

The 3-variable Karnaugh map is an array of eight cells. In this case, A, B, and C are used as variables. These eight cells can be arranged in 2 X 4 or 4 X 2 arrays. In a 4X2 arrangement, the rows can be labeled using the values of A B as 0 0, 0 1, 1 1, 1 0. The columns can be labeled with the values of C as 0 , 1. These binary values differ by only one bit.

The Fig. 4.23 shows the sum-of-product K-Map for the sample truth table.

A	B	C	Y
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

	$\overline{B}\overline{C}$	$\overline{B}C$	BC	$B\overline{C}$
$\overline{A}$	1			1
A	1			1

Sum-of-products K-map

Fig.4.23 Three variable Karnaugh Map

Logical Adjacency

. Two terms are logically adjacent if they differ with respect to any one variable.
. ABC is logically adjacent to $\overline{A}BC$, $A\overline{B}C$ and $AB\overline{C}$
. ABC is not logically adjacent to $A\overline{B}\,\overline{C}$, $\overline{A}\,\overline{B}C$, $A\overline{B}\,\overline{C}$, ABC
. The entries that are adjacent in a truth-table are not necessarily logically adjacent
. K-map arranges the logically adjacent terms to be physically adjacent

It is possible to express the logical equations or Boolean functions using sum of products and product of sums.

Construction of a Karnaugh Map

An n-variable Karnaugh map has 2^n squares, and each possible input is allotted a square. In the case of a minterm Karnaugh map, '1' is placed in all those squares for which the output is '1', and '0' is placed in all those squares for which the output is '0'. 0s are omitted for simplicity. An 'X' is placed in squares corresponding to 'don't care' conditions. In the

case of a maxterm Karnaugh map, a ‘1’ is placed in all those squares for which the output is ‘0’, and a ‘0’ is placed for input entries corresponding to a ‘1’ output. Again, 0s are omitted for simplicity, and an ‘X’ is placed in squares corresponding to ‘don’t care’ conditions.

Looping

The grouping of adjacent 1’s in the Karnaugh map is called looping. The two (pair), four(quad) or eight (octet) adjacent squares that contain 1's are looped to create a simplified boolean expression (note the number of adjacent squares in a power of 2). The expression for the loop will eliminate one or more variables that appear in both normal and complemented form. The pair eliminates one variable. The quad eliminates 2 variables. The octet eliminates 3 variables.

Minimization of Karnaugh maps (Sum-of-products form)

Karnaugh map can be drawn for the given switching function (logical function) using the following guidelines.

Construction of K-Map

- All the squares (cells) should be drawn adjacent to each other.
- Assignment of variables should be done in such a way that two adjacent squares differ in only one literal. Thus a cyclic pattern is reflected among adjacent squares.
- Each square (cell) represents a standard term and assigned a unique decimal value as per the min-term (or max-term). These numbers are shown on upper-left hand corner of each cell.
- Enter ‘1’ for each minterm.
- If there are don’t-care-combinations enter ‘x’ in the corresponding cells.
- For the rest of the cells enter ‘0’.

Grouping of adjacent cells

- For the minterm representation of n-variable functions, adjacent 1’s on the map can be grouped into the multiples of 2 (eg. 2, 4, 8 etc.). Group of 2, 4, and 8 adjacent 1’s are called as **pairs**, **quads** and **octets** respectively.
- Find out all the cells that cannot be grouped with any other cell. Encircle each such square.
- Examine the squares with 1’s and form the groups of quads and octets if possible.
- Identify all 1’s that can be grouped with only one other adjacent square and form the pair.
- Some squares may be simultaneously accounted in pairs, quads and octets.
- Some groups may overlap with other groups.
- Check that all squares with 1’s entry have been grouped or accounted as isolated squares.

- If don't-care-combinations are given, then these should be entered as 'x' in corresponding squares. If these 'x' entries form pairs, quads or octets, these should be included. If these 'x' do not help in forming groups, these should be avoided.
- Always try to form the largest possible groups. This will eliminate maximum number of variables.
- Write the product s involving common literals of each pairs, quad and octet and sum them to obtain minimal function.

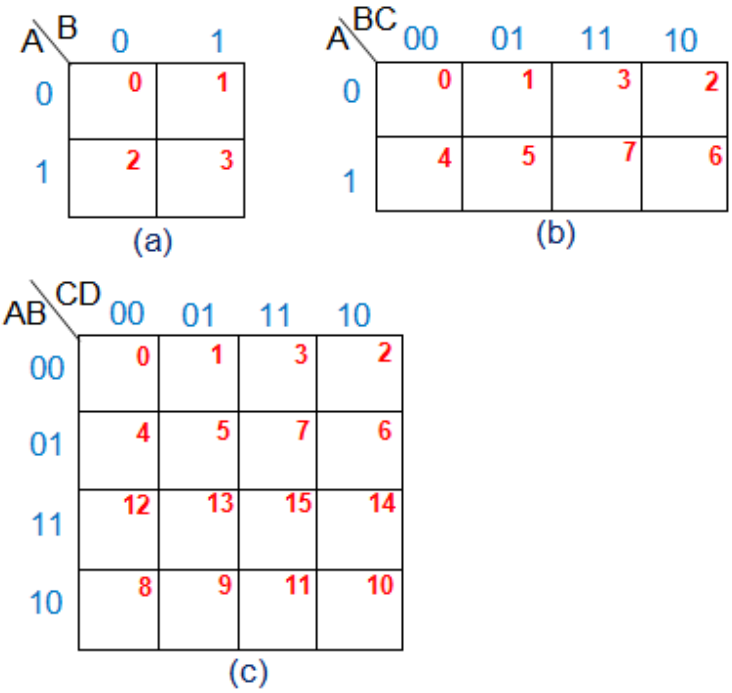
Advantages of Karnaugh Map

1. K-map simplification does not demand for the knowledge of Boolean algebraic theorems
2. Usually it requires less number of steps when compared to algebraic minimization technique

Disadvantages of Karnaugh Map

1. Complexity of **K-map** simplification process increases with the increase in the number of variables
2. The minimum expression obtained might not be unique.

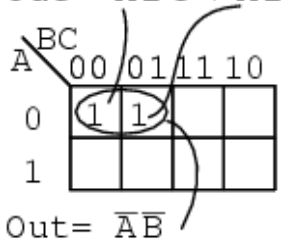
Numbering of cells in 2, 3 and 4 variable Karnaugh maps



Simplification of 3 variable logical expressions

1.

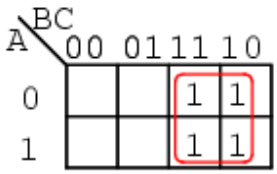
$Out = \overline{A}\,\overline{B}\,\overline{C} + \overline{A}\,\overline{B}\,C$



$Out = \overline{A}\,\overline{B}$

2.

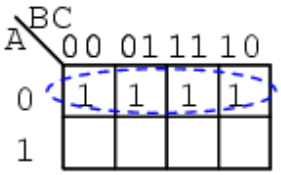
$Out = \overline{A}\,B\,C + \overline{A}\,B\,\overline{C} + A\,B\,C + A\,B\,\overline{C}$



$Out = B$

3.

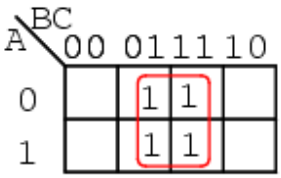
$Out = \overline{A}\,\overline{B}\,\overline{C} + \overline{A}\,\overline{B}\,C + \overline{A}\,B\,C + \overline{A}\,B\,\overline{C}$



$Out = \overline{A}$

4.

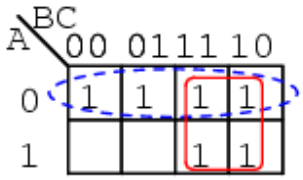
$Out = \overline{A}\,\overline{B}\,C + \overline{A}\,B\,C + A\,\overline{B}\,C + A\,B\,C$



$Out = C$

5.

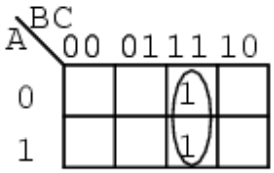
$$Out = \overline{A}\,\overline{B}\,\overline{C} + \overline{A}\,\overline{B}C + \overline{A}BC + \overline{A}B\overline{C} + ABC + AB\overline{C}$$



$$Out = \overline{A} + B$$

6.

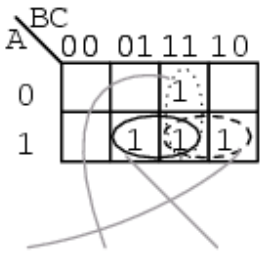
$$Out = \overline{A}BC + ABC$$



$$Out = BC$$

7.

$$Output = \overline{A}BC + A\overline{B}C + AB\overline{C} + ABC$$



$$Output = AB + BC + AC$$

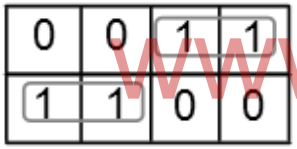
Complete Simplification Process

1. Construct the K map and place 1s and 0s in the squares according to the truth table.
2. Group the isolated 1s which are not adjacent to any other 1s. (single loops)
3. Group any pair which contains a 1 adjacent to only one other 1. (double loops)
4. Group any octet even if it contains one or more 1s that have already been grouped.
5. Group any quad that contains one or more 1s that have not already been grouped, making sure to use the minimum number of groups.
6. Group any pairs necessary to include any 1s that have not yet been grouped, making sure to use the minimum number of groups.
7. Form the OR sum of all the terms generated by each group.

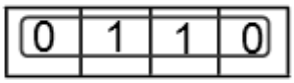
Minterm Solution of K Map

The following are the steps to obtain simplified minterm solution using K-map.
Step 1: Initiate
Write the given expression in its canonical form
Step 2: Populate the K-map
Enter the value of 'one' for each product-term into the K-map cell, while filling others with zeros.
Step 3: Form Groups

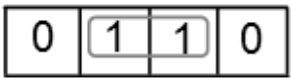
- Consider the consecutive 'ones' in the K-map cells and group them.



- Each group should contain the largest number of 'ones' and no blank cell.



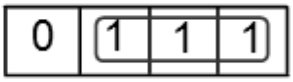
Incorrect



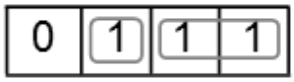
Correct

- The number of 'ones' in a group must be a power of 2 i.e. a group can contain

$$16(=2^4)\ or\ 8(=2^3)\ or\ 4(=2^2)\ or\ 2(=2^1)\ or\ 1(=2^0)\ cells$$

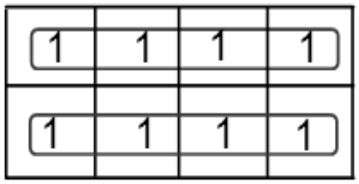


Incorrect



Correct

- Grouping has to be carried-on in decreasing order meaning, one has to try to group for 8 (octet) first, then for 4 (quad), followed by 2 and lastly for 1 (isolated 'ones').



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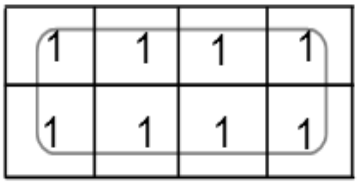
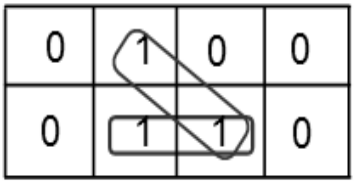


Correct

- Grouping is to done either horizontally or vertically or in terms of squares or rectangles. Diagonal grouping of 'ones' is not permitted.



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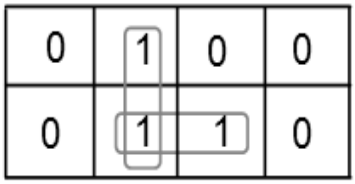
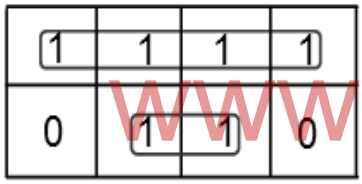
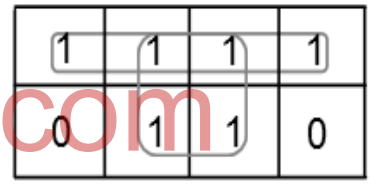


Correct

- The same element(s) may repeat in multiple groups only if this increases the size of the group.

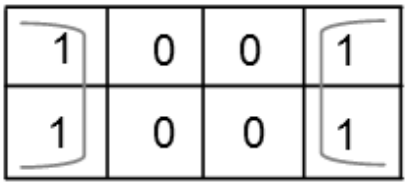


Incorrect

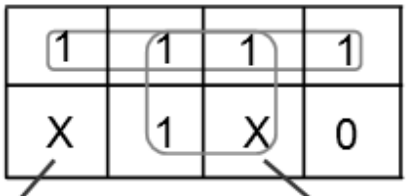


Correct

- The elements around the edges of the table are considered to be adjacent and can be grouped together.



- Don’t care conditions are to be considered only if they aid in increasing the group-size (else neglected).

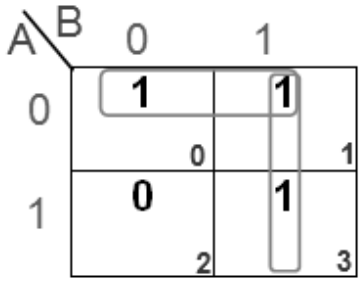


Neglect Consider

Simplify the logical expression using K-Map

1.

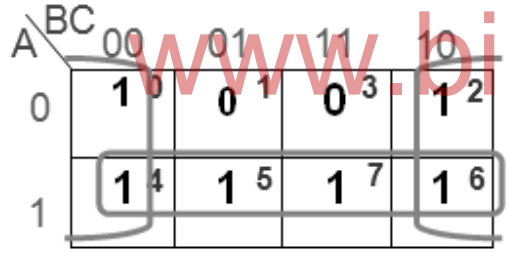
$$Y = \overline{A}\,\overline{B} + \overline{A}B + AB$$



$$Simplified\ Expression : Y = \overline{A} + B$$

2.

$$Y = \overline{A}\,\overline{B}\,\overline{C} + \overline{A}B\,\overline{C} + A\overline{B}\,\overline{C} + A\overline{B}C + AB\overline{C} + ABC$$



$$Simplified\ Expression : Y = A + \overline{C}$$

4.4 Arithmetic circuits

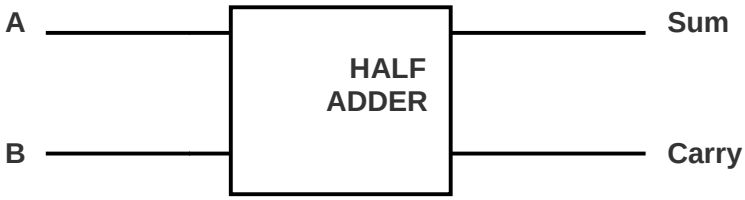
Logic circuits that perform arithmetic functions like addition, subtraction, multiplication and division are called arithmetic circuits. Arithmetic circuits are combinational circuits. More complex combinational circuits such as adders and subtractors, multiplexers and demultiplexers, magnitude comparators, etc., can be implemented using a combination of logic gates. Addition and subtraction are the two most commonly used arithmetic operations, as the other two, namely multiplication and division, are respectively the processes of repeated addition and repeated subtraction.

Adder

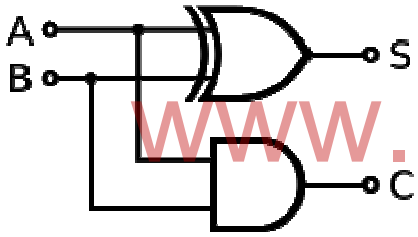
A logic circuit that performs the function of binary addition is called **electronic adder** or **adder.** The adder circuit consists of properly connected logic gates. There are usually two forms of the adder in common applications: (i) half adder (ii) full adder.

Half Adder

The **half adder** adds two single bits (binary digits) *A* and *B*. It has two outputs, sum (*S*) and carry (*C*). The carry signal represents an overflow into the next bit of a multi-bit addition. The value of the sum is 2*C* + *S*. The input variables of half adder are called the augend and addend bits. The output variables are the sum and carry. The simplest half-adder design incorporates an XOR gate for *Sum* and an AND gate for *Carry*. The block diagram, logic diagram and the truth table of the half adder are shown in Fig. 4.24.



(a) Block Diagram



(a) Logic diagram

Inputs		Outputs	
A	B	Sum	Carry
0	0	0	0
1	0	1	0
0	1	1	0
1	1	0	1

(b) Truth Table

Fig.4.24 Half Adder

From the truth table, the *sum-of-product* form of outputs can be expressed as

$$Sum = A\bar{B} + \bar{A}B = A \oplus B$$

$$Carry = AB$$

The sum column is the output of XOR gate. Remember that XOR gate has HIGH output when either input is HIGH but not when both inputs are the same.

The carry column is the output of the AND gate. Both inputs must be HIGH for this carry to be a HIGH in the output.

Thus we can produce half adder using a two-input AND gate and a two-input XOR gate as shown in Fig. 4.24 (b). The half adder circuit adds only the LSB column (1s column) in a binary addition problem. The reason is that it has no input for a carry-in.

K-map simplification for carry and sum of half adder

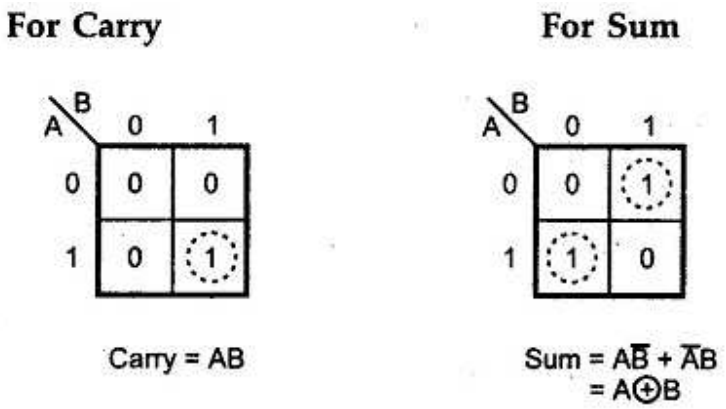
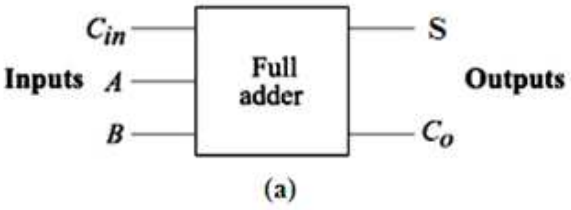


Fig. 4.25 K-Map representation for half adder outputs

Full Adder

A full adder is a logic circuit which adds three bits. Full adder adds two binary bits plus a carry input (C_{in}) to produce the sum (S) and carry (C_o) outputs. Fig. 4.26 (a) shows the block diagram of a full adder. It is formed by using two half adder circuits and an OR gate. Note the carry-in (C_{in}) input which requires the extra half adder. The output of the OR gate forms the carry(C_o) output.

The full adder has three inputs: C_{in}, *A* and *B*. These three inputs must be added to get the S and C_{out} outputs. Fig. 4.26 (b) shows the truth table for a full adder. It shows all the possible combinations of *A, B* and C_{in}.The Fig.4.26(c) shows how the full-adder can be constructed using two half-adders.



Truth Table

Inputs			Outputs	
C_{in}	B	A	S	C_o
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1
Carry + B + A			Sum	Carry out

(b)

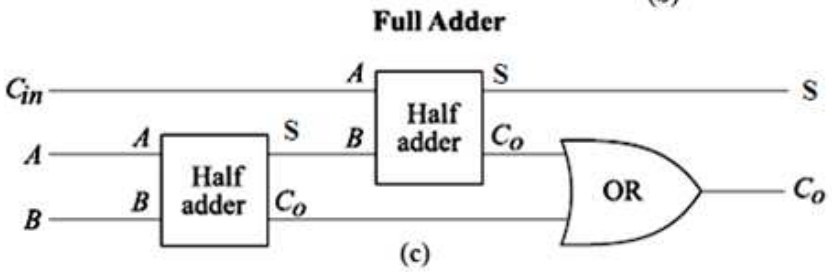
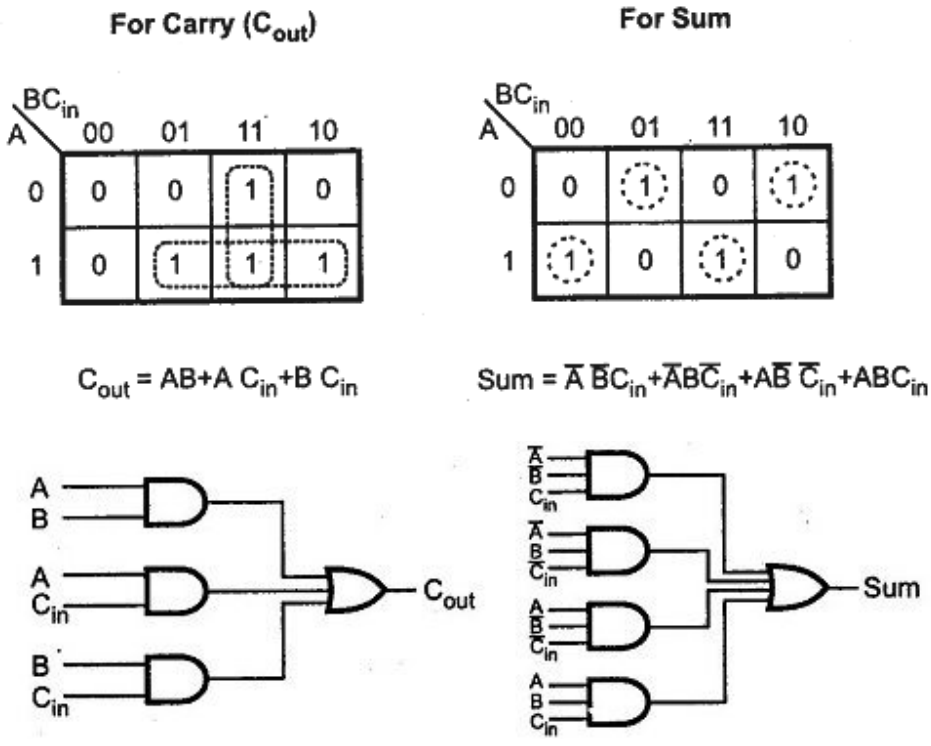


Fig. 4.26 Full adder (a) Block diagram (b) Truth table (c) Combining two half adders

K-map simplification for carry and sum of full adder



The Boolean function for **sum** can be further simplified as follows

$$\begin{aligned}
\text{Sum} &= \overline{A}\ \overline{B}\ C_{in} + \overline{A}\ B\ \overline{C}_{in} + A\ \overline{B}\ \overline{C}_{in} + A\ B\ C_{in} \\
&= C_{in}\ (\overline{A}\ \overline{B} + AB) + \overline{C}_{in}\ (\overline{A}\ B + A\ \overline{B}) \\
&= C_{in}\ (A \odot B) + \overline{C}_{in}\ (A \oplus B) \\
&= C_{in}\ (\overline{A \oplus B}) + \overline{C}_{in}\ (A \oplus B) \\
&= C_{in} \oplus (A \oplus B)
\end{aligned}$$

With this simplified Boolean function circuit for full-adder can be implemented as shown in the Fig. 4.27

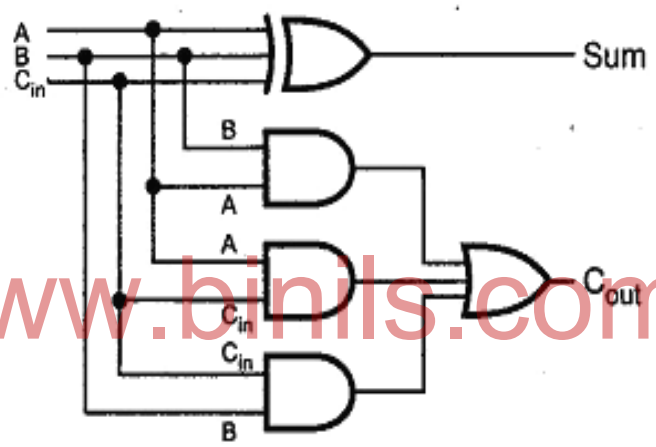


Fig. 4.27 Implementation of Full-adder

For the full-adder the outputs are

Sum $\oplus$ A $\oplus$ B C_{in}
Carry C_{out} = $AB+BC_{in}+AC_{in}$

A full-adder can also be implemented with two half-adders and one OR gate, as shown in the Fig. 4.28.

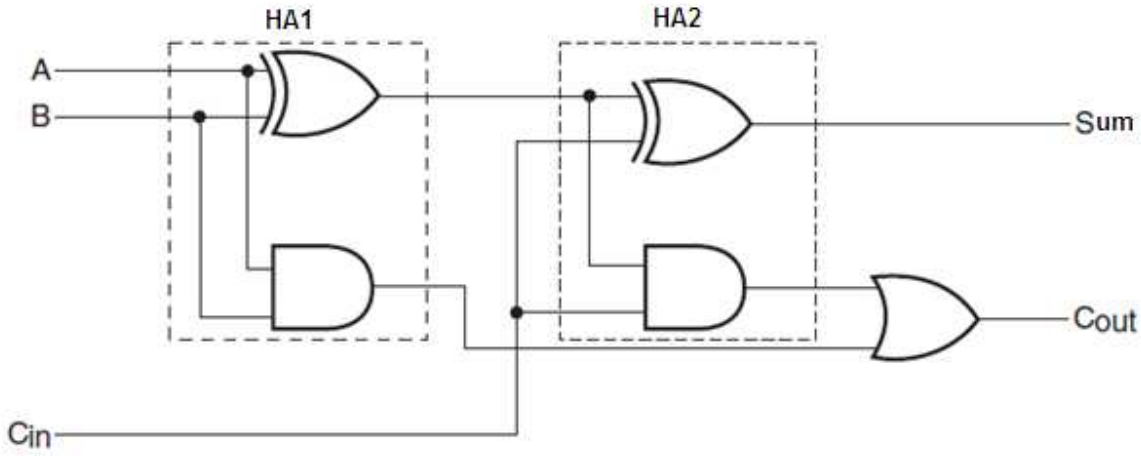


Fig. 4.28 Logic circuit diagram of full adder using two half adders and an OR gate.

The sum output from the second half-adder is the exclusive-OR of C_{in} and the output of the first half-adder, giving

$$
\begin{aligned}
\text{Sum} &= C_{in} \oplus (A \oplus B) \\
&= C_{in} \oplus (A\overline{B} + \overline{A}B) \\
&= \overline{C_{in}}\,(A\overline{B} + \overline{A}B) + C_{in}\,\overline{(A\overline{B} + \overline{A}B)} \\
&= \overline{C_{in}}\,(A\overline{B} + \overline{A}B) + C_{in}\,(\overline{A\overline{B}} \cdot \overline{\overline{A}B}) \\
&= \overline{C_{in}}\,(A\overline{B} + \overline{A}B) + C_{in}\,[(\overline{A} + B) \cdot (A + \overline{B})] \\
&= \overline{C_{in}}\,(A\overline{B} + \overline{A}B) + C_{in}\,(\overline{A}\,\overline{B} + AB) \\
&= \overline{A}\,\overline{B}C_{in} + AB\,C_{in} + A\overline{B}\,\overline{C_{in}} + \overline{A}B\overline{C_{in}} \\
&= \overline{A}\,\overline{B}C_{in} + \overline{A}B\overline{C_{in}} + A\overline{B}\,\overline{C_{in}} + AB\,C_{in}
\end{aligned}
$$

which represents the output of the truth table.

The carry output from the combination of two half adders as shown in Fig.4.28 is

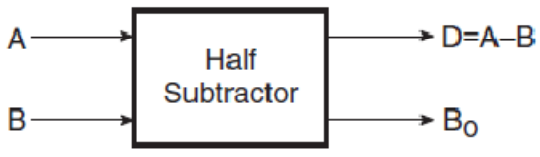
$$
\begin{aligned}
C_{out} &= AB + C_{in}(A\bar{B} + \bar{A}B) \\
&= AB + A\bar{B}C_{in} + \bar{A}BC_{in} \\
&= AB(C_{in} + 1) + A\bar{B}C_{in} + \bar{A}BC_{in} && \because\ C_{in} + 1 = 1 \\
&= ABC_{in} + AB + A\bar{B}C_{in} + \bar{A}BC_{in} \\
&= AB + AC_{in}(B + \bar{B}) + \bar{A}BC_{in} \\
&= AB + AC_{in} + \bar{A}BC_{in} \\
&= AB(C_{in} + 1) + AC_{in} + \bar{A}BC_{in} && \because\ C_{in} + 1 = 1 \\
&= ABC_{in} + AB + AC_{in} + \bar{A}BC_{in} \\
&= AB + AC_{in} + BC_{in}(A + \bar{A}) \\
&= AB + AC_{in} + BC_{in}
\end{aligned}
$$

Half Subtractor

The half subtractor is a combinational circuit which is used to perform subtraction of two bits. It has two inputs, the minuend A and subtrahend B and two outputs the difference D and borrow out B_o.The borrow out signal is set when the subtractor needs to borrow from the next digit in a multi-digit subtraction. That is, B_o =1 when A<B. Since A and B are bits, B_o =1 if and only if A=0 and B=1. An important point worth mentioning is that the half subtractor diagram implements A-B and not B-A. The borrow B_o and difference D are given by

Borrow $B_o = \bar{A}B$

Difference $D = A \oplus B$



A	B	D	B_0
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

Fig. 4.29 Half subtractor (a) Block diagram (b) Truth table.

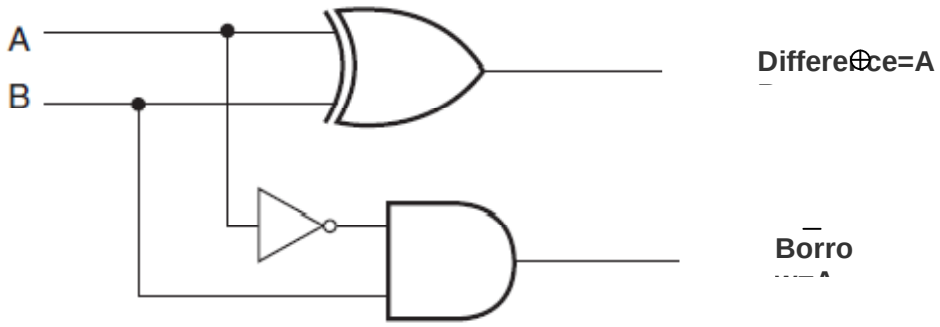


Fig. 4.30 Logic diagram of Half subtractor

Full subtractor

The full-subtractor is a combinational circuit which is used to perform subtraction of three input bits: the minuend A, subtrahend B, and borrow in $\mathbf{B_{in}}$. The full-subtractor generates two output bits: the difference D and borrow out $\mathbf{B_{out}}$.

The third bit $\mathbf{B_{in}}$ is set when the previous digit borrowed from A. Thus, $\mathbf{B_{in}}$ is also subtracted from A as well as the subtrahend B which is $\mathbf{A\text{-}B\text{-}B_{in}}$. Like the half-subtractor, the full-subtractor generates borrow out when it needs to borrow from the next digit. Since we are subtracting B and B_{in} from A, borrow out needs to be generated when $\mathbf{A<B+B_{in}}$. When a borrow out is generated, 2 is added in the current digit. (This is similar to the subtraction algorithm in decimal. Instead of adding 2, we add 10 when we borrow.) Therefore $\mathbf{D=A\text{-}B\text{-}B_{in}+2B_{out}}$. The truth table for the full-subtractor is given below.

Minuend (A)	Subtrahend (B)	Borrow In (B_{in})	Difference (D)	Borrow Out (B_O)
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

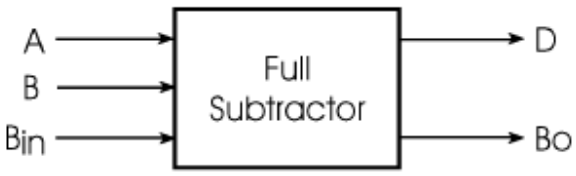


Fig. 4.31(a) Block diagram of full-subtractor

The block diagram of full-subtractor is shown in Fig.4.31(a). The K-Map representation and sum-of-product implementation of the D and B_{out} of truth table are given in Fig.4.31 (b).

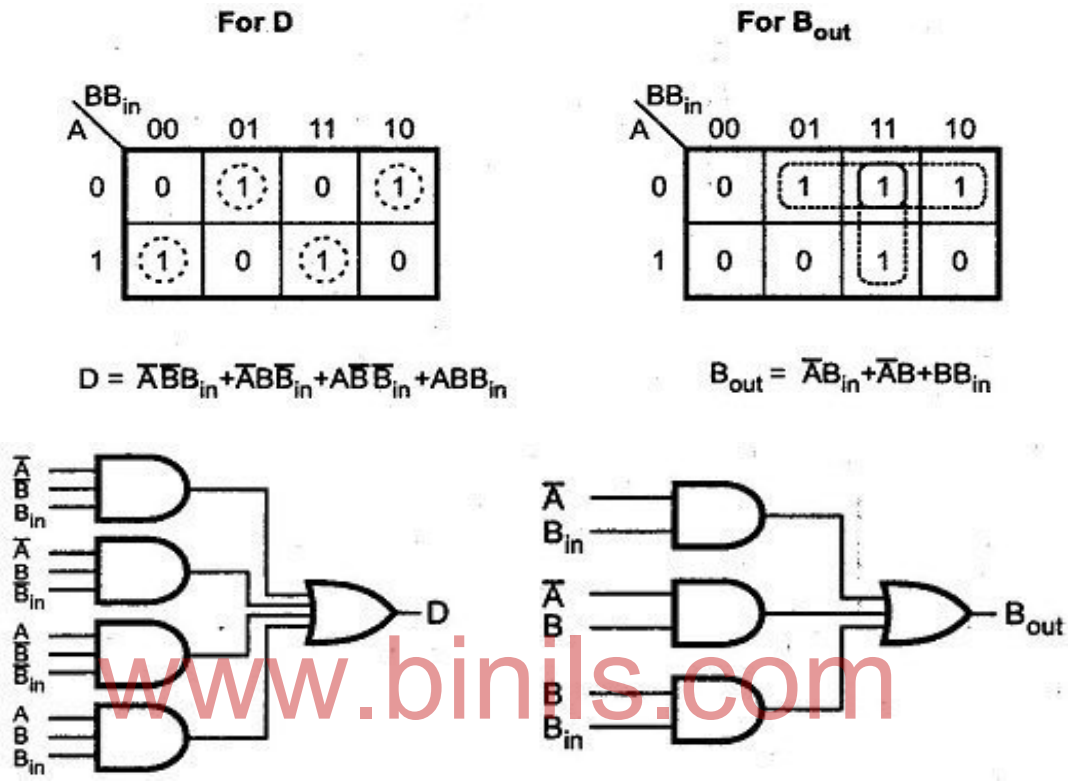


Fig. 4.31(b) Sum of product implementation of full-subtractor

The Boolean function for D (difference) can be further simplified as follows

$$D = \bar{A}\,\bar{B}\,B_{in} + \bar{A}\,B\,\bar{B}_{in} + A\,\bar{B}\,\bar{B}_{in} + A\,B\,B_{in}$$

$$= B_{in}\,(\bar{A}\,\bar{B} + AB) + \bar{B}_{in}\,(\bar{A}\,B + A\,\bar{B})$$

$$= B_{in}\,(A \odot B) + \bar{B}_{in}\,(A \oplus B)$$

$$= B_{in}\,(\overline{A \oplus B}) + \bar{B}_{in}\,(A \oplus B)$$

$$= B_{in} \oplus (A \oplus B)$$

$$B_{out} = \bar{A}B_{in} + \bar{A}B + BB_{in}$$

With this simplified Boolean function circuit for full-subtractor can be implemented as shown in the Fig.4.32.

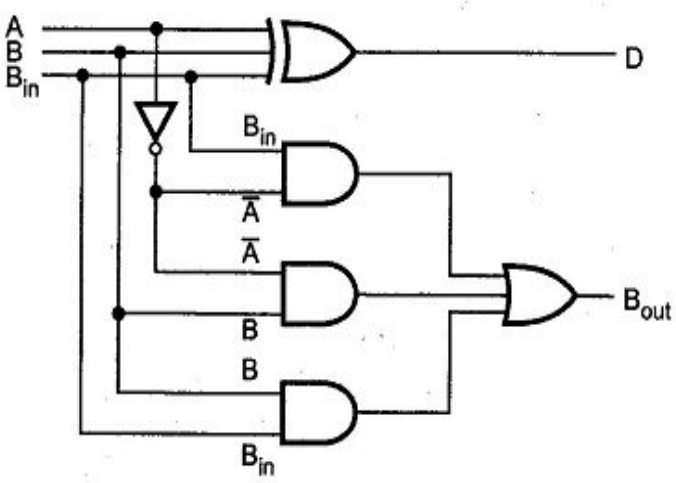
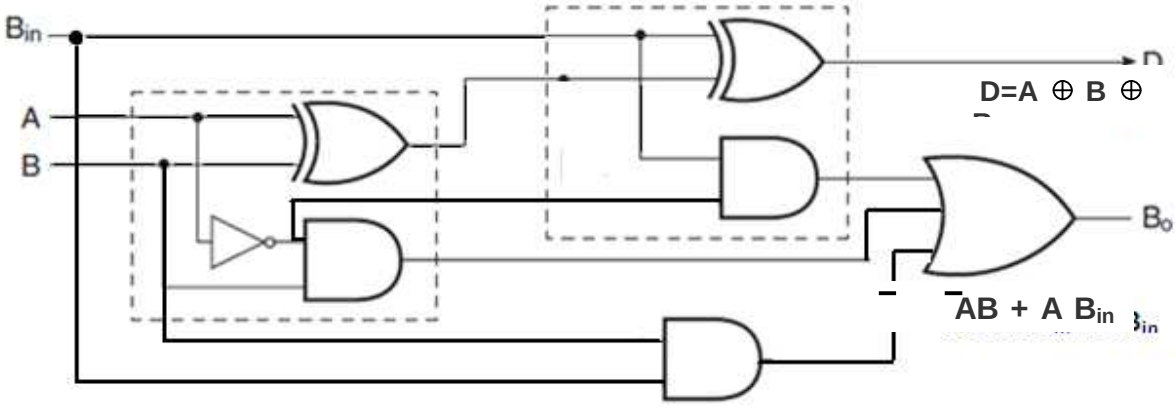


Fig. 4.32 Implementation of full-subtractor

A full subtractor can also be implemented with two half-subtractors and one OR gate, as shown in the Fig.4.33. The difference output from the second half-subtractor is the exclusive-OR of B_{in} and the output of the first half-subtractor, which is same as difference output of full-subtractor.

(a) Block diagram



(b) Logic diagram

Fig. 4.33 (a) Block diagram and (b) logic diagram of Full-Subtractor with two half subtractors.

The borrow output for circuit shown in Fig. 4.33 can be given as

$$
\begin{aligned}
B_{out} &= \bar{A}B+\overline{(A\bar{B}+\bar{A}B)}\,B_{in} = \bar{A}B+(AB+\bar{A}\,\bar{B})\,B_{in} \\
&= \bar{A}B+A\,BB_{in}+\bar{A}\,\bar{B}B_{in} \\
&= \bar{A}B(1+B_{in})+A\,BB_{in}+\bar{A}\,\bar{B}B_{in} \qquad \because (1+B_{in}) = 1 \\
&= \bar{A}B+\bar{A}\,BB_{in}+ABB_{in}+\bar{A}\,\bar{B}B_{in} = \bar{A}B+BB_{in}\,(\bar{A}+A)+\bar{A}\,\bar{B}B_{in} \\
&= \bar{A}B+BB_{in}+\bar{A}\,\bar{B}B_{in} \\
&= \bar{A}B(1+B_{in})+BB_{in}+\bar{A}\,\bar{B}B_{in} \qquad \because (1+B_{in}) = 1 \\
&= \bar{A}B+\bar{A}BB_{in}+BB_{in}+\bar{A}\,\bar{B}B_{in} = \bar{A}B+\bar{A}B_{in}\,(B+\bar{B})+BB_{in} \\
&= \bar{A}B+\bar{A}B_{in}+BB_{in}
\end{aligned}
$$

This boolean function is same as borrow out of the full-subtractor. Therefore, we can implement full subtractor using two half-subtractors and OR gate.

4.5 Combinational logic circuits

Introduction

A logic circuit consisting of two or more logic gates that has no feedback and no memory is called a **combinational logic circuit.**

A combinational logic circuit is constructed using OR, AND and NOT gates. Therefore, the basic building block for combinational circuits is the logic gate. Since a combinational logic circuit has no feedback and no memory, its output depends *only* on the current value of its inputs.

Combinational logic circuit is a type of digital logic circuit which is implemented by Boolean circuits, where the output is a pure function of the present input only. In a c**ombinational logic circuit**, the output depends on the combination of its inputs.

Combinational logic is about combining logic gates together to process two or more signals in order to produce at least one output signal according to the logical function of each logic gate. Common combinational circuits include **Multiplexers**, **De-multiplexers**, **Encoders**, **Decoders**, **adders** and **Comparators**.

Some of the characteristics of combinational circuits are

- The output of combinational circuit at any instant of time depends only on the levels present at input terminals.

- The combinational circuit does not use any memory. The previous state of input does not have any effect on the present state of the circuit.
- A combinational circuit can have an n number of inputs and m number of outputs.

4.5.1 Parity generator and checker

A parity bit is used for the purpose of detecting errors during the transmission of binary information. A parity bit is an extra bit included with a binary message to make the number of 1's either odd or even. The message, including the parity bit, is transmitted and then checked at the receiving end for errors. An error is detected if the checked parity does not match with the transmitted data. The circuit that generates the parity bit in the transmitter is called a ***parity generator***. The circuit that checks the parity in the receiver is called *a* ***parity checker***.

In ***even parity*** the added bit is such that the total number of 1s in the data bit string becomes even, and in an ***odd parity***, the added bit makes the total number of 1s in the data bit string odd. This added bit could be a '0' or a '1'.

As an example, if we have to add an even parity bit to 01000001 (the eight-bit ASCII code for 'A'), it will be a '0' and the number will become 001000001. If we have to add an odd parity bit to the same number, it will be a '1' and the number will become 101000001. **The odd parity bit is a complement of the even parity bit.** The most common convention is to use even parity, that is, the total number of 1s in the bit stream, including the parity bit, is even.

The parity check can be made at different points to look for any possible single-bit error, as it would disturb the parity. This simple parity code suffers from two limitations. Firstly, it cannot detect the error if the number of bits having undergone a change is even. Secondly, the single-bit parity code cannot be used to localize or identify the error bit even if one bit is in error. The simple circuits for parity generators and parity checkers are discussed.

Parity generator

As an example, consider a three-bit message to be transmitted together with an even parity bit. Fig.4.34 shows the logic diagram and truth table for the even parity generator. The three bits- x, y and z constitute the message and are the inputs to the circuit. The parity bit *P* is the output. For even parity the bit *P* must be generated to make the total number of 1's even (including *P)*. From the truth table, we see that *P* constitutes an odd function because it is equal to 1 for those minterms whose numerical values have an odd number of 1's. Therefore, *P* can be expressed as a three-variable exclusive-OR function.

$$P = x \oplus y \oplus z$$

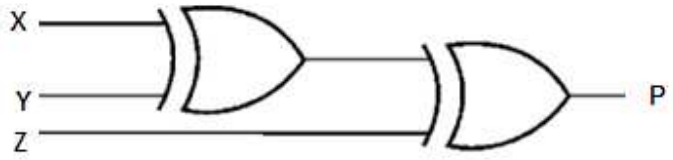


Fig. 4.34 (a) Logic diagram of 3 bit even parity generator

Three-Bit Message			Parity Bit
x	y	z	P
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

Fig. 4.34 (b) truth table for even parity generator

Parity checker

The three bits in the message together with the parity bit are transmitted to their destination where they are applied to a parity-checker circuit to check for possible errors in the transmission. Since the information was transmitted with even parity the four bits received must have an even number of 1s. An error occurs during the transmission if the four bits received have an odd number of 1s, indicating that one bit has changed in value during transmission. The logic diagram of the parity checker is shown in Fig. 4.35 (a). The inputs are the data bits along with parity bit.

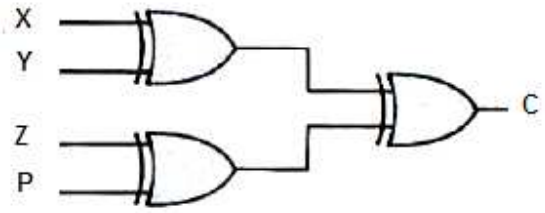


Fig. 4.35 (a) Logic diagram of even parity checker

Four Bits Received				Parity Error Check
x	y	z	p	c
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

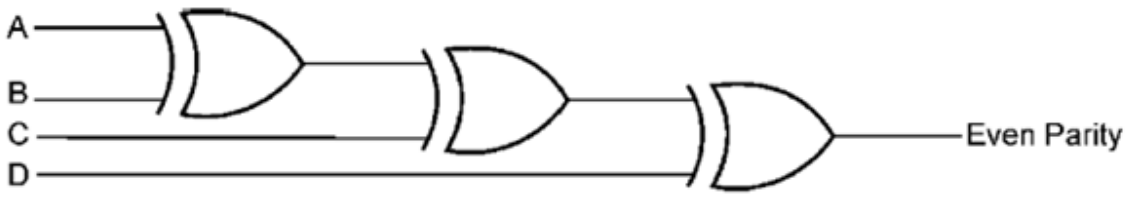
Fig. 4.35 (b) Truth table for even parity checker

The output of the parity checker, denoted by C will be equal to 1 if an error occurs – that is, if the four bits received have an odd number of 1s. Fig. 4.35 (b) is the truth table for the even-parity checker, from it we see that the function C consists of the eight minterms with binary numerical values having an odd number of 1s. The parity checker can be implemented with exclusive-OR gates:

$$C = x \oplus y \oplus z \oplus p$$

The parity generator can be implemented with the above parity checker circuit, if the input P is connected to logic 0 and the output is marked with P. This is because $z \oplus 0 = z$ causing the value of z to pass through the gate unchanged. The advantage of this strategy is that the same circuit can be used for both parity generation and checking.

EX-OR and EX-NOR logic gates are commonly used in parity generation and checking circuits. Figures 4.36 (a) and (b) respectively show even and odd parity generator circuits for a four-bit data. The circuits are self-explanatory.



(a)

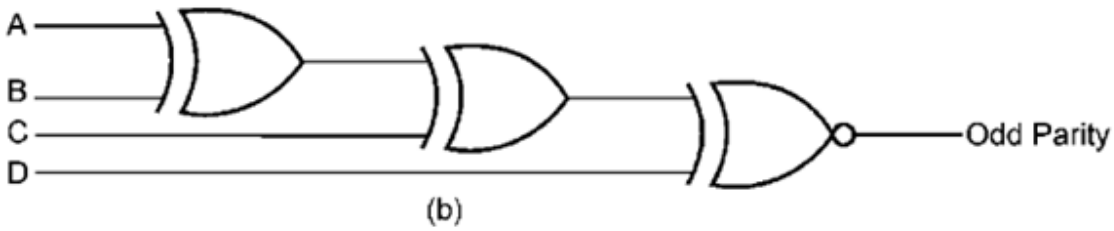


Fig. 4.36 (a) Even and (b) Odd Parity generators using Ex-OR and Ex-NOR gates for 4-bit data.

The parity check operation can also be performed by similar circuits. Figures 4.37(a) and (b) respectively show simple even and odd parity checker circuits for a four-bit data stream. In the circuits a logic '0' at the output signifies correct parity and logic '1' signifies one-bit error. Parity generator/checker circuits are available in IC form.

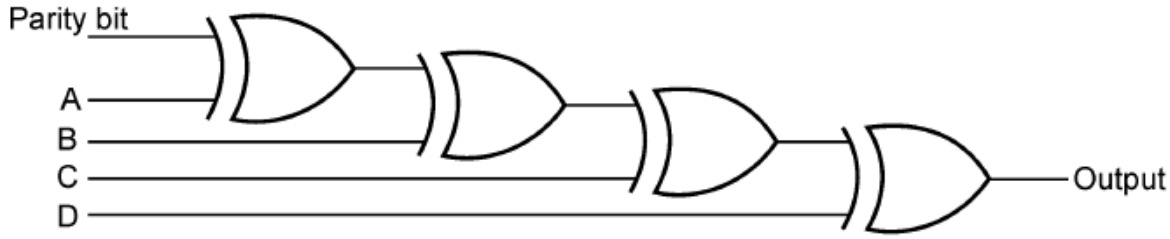


Fig. 4.37 (a) Even parity checker

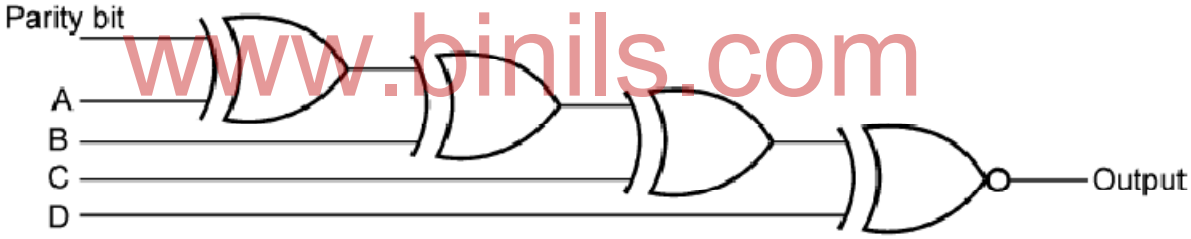


Fig. 4.37 (b) Odd parity checker

4.5.2 Multiplexer

Many tasks in communications, control, and computer systems can be performed by combinational logic circuits. Data generated in one location is to be used in another location. A method is needed to transmit it from one location to another through some communications channel. The data is available, in parallel, on many different lines but must be transmitted over a single communication link. Such a process is called multiplexing.

Another example is the multiplexing of conversations on the telephone system. A number of telephone conversations are alternately switched on the telephone line many times per second.

A multiplexer is a combinational circuit that selects binary information from one of many input lines and directs it to a single output line. The selection of a particular

input line is controlled by a set of selection lines. Normally there are 2^n input lines and n selection lines whose bit combinations determine which input is selected.

A ***multiplexer*** or *MUX*, also called a ***data selector***, is a combinational circuit with more than one input line, one output line and more than one selection (control) lines. A multiplexer selects binary information present on any one of the input lines, depending upon the logic status of the selection inputs, and routes it to the output line. If there are n selection lines, then the number of maximum possible input lines is 2^n and the multiplexer is referred to as a **2^n-to- 1** multiplexer or **2^n ×1** multiplexer.

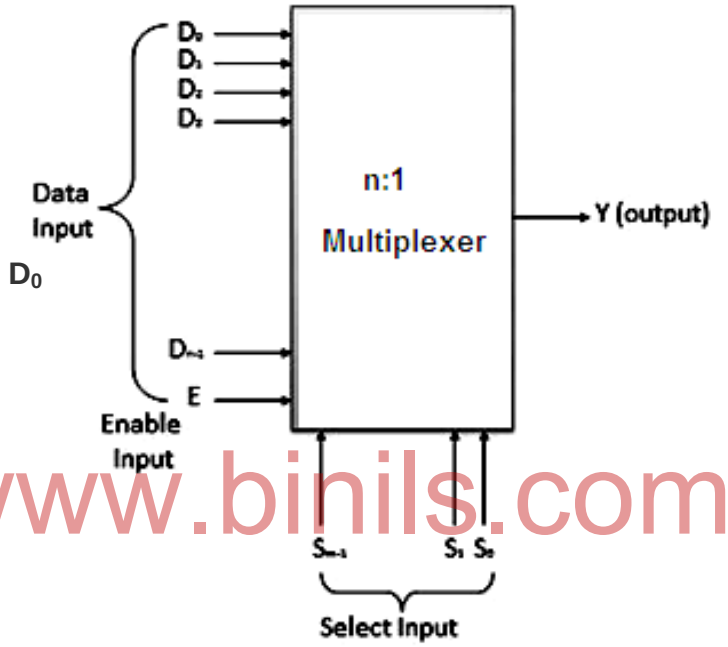


Fig. 4.38 General diagram of a Multiplexer

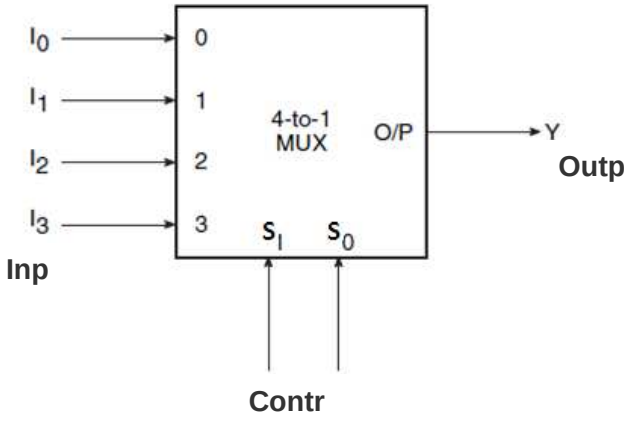
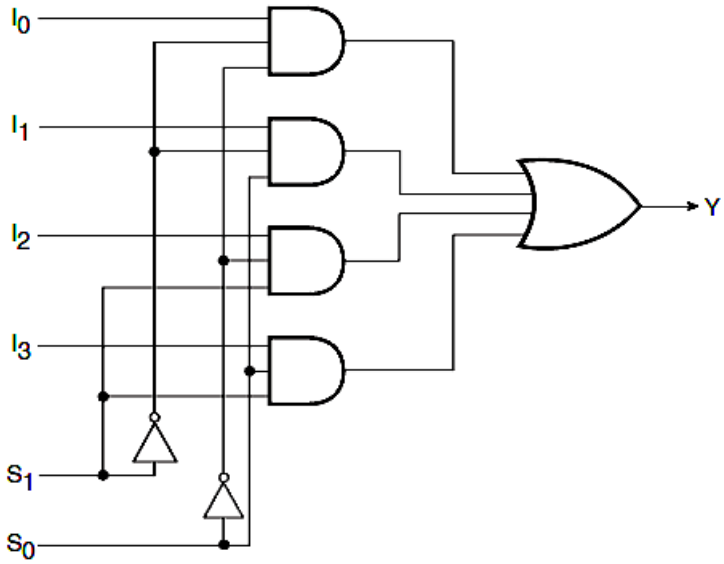


Fig.4.39 (a) Block diagram of 4 – to – 1 multiplexer.



S_1	S_0	Y
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

Fig. 4.39 (b) Logic circuit and the truth table of a basic 4-to-1 multiplexer

Figures 4.39 (a) and (b) respectively show the block diagram and the logic circuit with truth table of a basic 4-to-1 multiplexer. The input combinations 00, 01, 10 and 11 on the select lines (S_1S_0) respectively switch I_0, I_1, I_2 and I_3 to the output. The operation of the circuit is governed by the following Boolean function

$$Y = I_0 . \overline{S_1} . \overline{S_0} + I_1 . \overline{S_1} . S_0 + I_2 . S_1 . \overline{S_0} + I_3 . S_1 . S_0$$

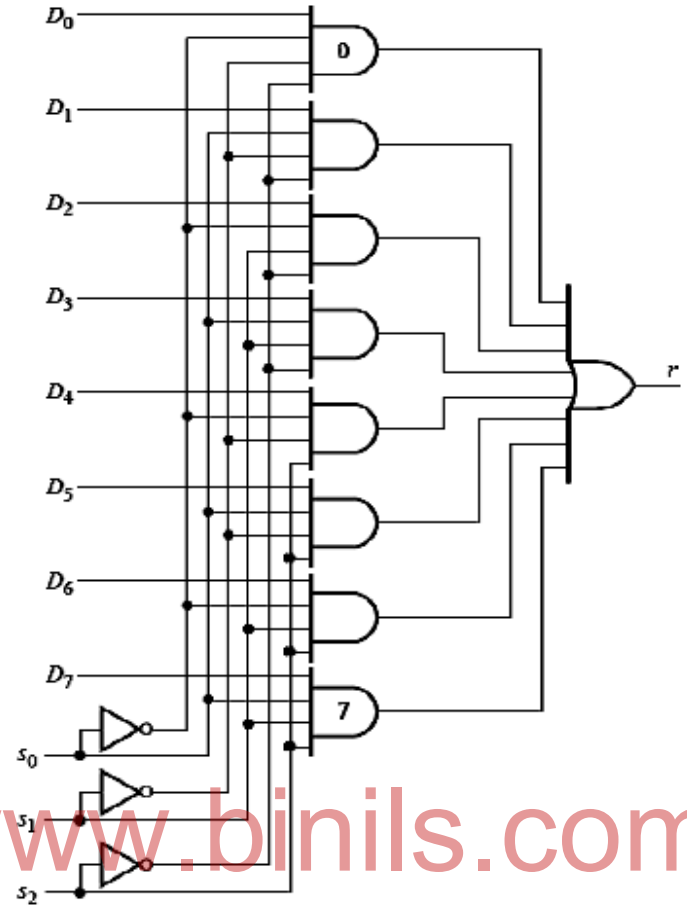


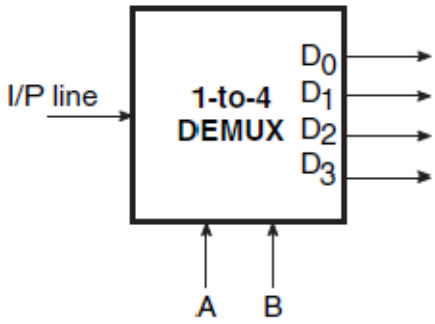
Fig. 4.40 Multiplexer (8 – to – 1) with 8 input lines and 3 control lines.

- Multiplexer is a combinational logic circuit used to select only one input among several inputs based on selection lines.
- This can act as a digital switch.
- This is also called as data selector.
- For a multiplexer, there can be 2^n inputs, n selection lines and only one output.
- It is a Many-to-One selector circuit.

4.5.3 Demultiplexer

A **demultiplexer** is a combinational logic circuit with an input line, n control lines and 2^n output lines. It routes the information present on the input line to any of the output lines. The output line that gets the information present on the input line is decided by the bit status of the selection lines. Demultiplexer is also called data distributor that is the data is distributed to any one of the selected output lines.

Figure 4.41 (a) shows the circuit representation of a 1-to-4 demultiplexer. Figure 4.41 (b) shows the truth table of the demultiplexer when the input line is held HIGH.



(a)

I/P	Select		O/P			
	A	B	D0	D1	D2	D3
1	0	0	1	0	0	0
1	0	1	0	1	0	0
1	1	0	0	0	1	0
1	1	1	0	0	0	1

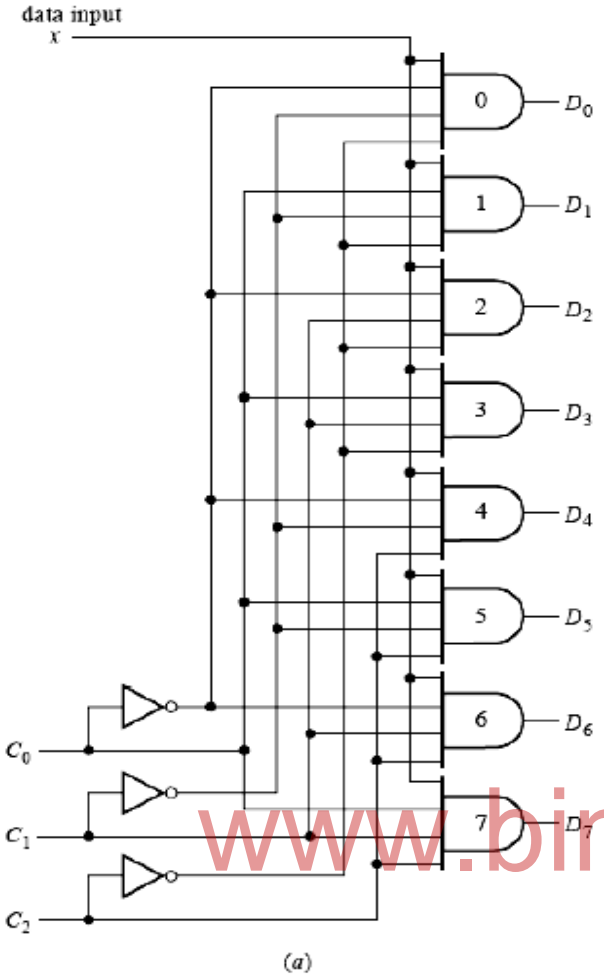
(b)

Fig. 4.41. 1-to-4 Demultiplexer (a) Circuit representation (b) Truth table.

It contains 2 control lines, 4 output lines and only one data input line. The data input line is enabled. When the select lines A and B are 0 0, the input is directed to the output line D_0. When the select lines are at 1 1, the input is directed to line D_3. The output will be available at any one line based on the control or select lines.

Demultiplexer is used to connect a single source to multiple destinations. The main application area of demultiplexer is communication system where multiplexer are used. Most of the communication systems are bidirectional i.e. they function in both ways (transmitting and receiving signals). Hence, for most of the applications, the multiplexer and demultiplexer work in sync. Demultiplexer is also used for reconstruction of parallel data and ALU circuits.

Logic diagram of 1- to - 8 demultiplexer is shown in the figure 4.5. It contains 3 control lines, 8 output lines and only one data input line. The data input line is labeled as x. The control and address bits are labeled as c_0,c_1 and c_2. The output bits are labeled as D_0, D_1, … , D_7. The data input **x** is transmitted to the selected output line. When the control lines $c_0c_1c_2$ = 000, only the AND gate 0 is enabled, other AND gates are disabled. Therefore the data input x is transmitted through D_0. The outputs of all other gates are 0.



Control Inputs			Data Outputs							
C_2	C_1	C_0	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
0	0	0	x	0	0	0	0	0	0	0
0	0	1	0	x	0	0	0	0	0	0
0	1	0	0	0	x	0	0	0	0	0
0	1	1	0	0	0	x	0	0	0	0
1	0	0	0	0	0	0	x	0	0	0
1	0	1	0	0	0	0	0	x	0	0
1	1	0	0	0	0	0	0	0	x	0
1	1	1	0	0	0	0	0	0	0	x

(b)

Fig.4.42 1-to-8 Demultiplexer (a) Logic diagram (b) truth table

A multiplexer is a circuit that accepts many input
function exactly in the reverse of a multiplexer,
input and gives many outputs. Generally multiple
because the communication systems are bidirecti

4.5.4 Encoders and Decoders

A digital circuit can process numbers in binary form. However, most of the information we handle is in decimal form. Therefore, a digital machine must perform the following functions:

(***i***) Convert the information from decimal to digital (binary) form.
(***ii***) Process the digital information.
(***iii***) Convert the digital output back to decimal form.

The circuit that converts decimal form to digital (binary) form is called **encoder** and the circuit that converts digital form to decimal form is called **decoder.** Figure 4.43 shows encoding and decoding in a digital calculator. Here the input is the decimal number 5 punched in at the keyboard. The encoder changes the decimal number 5 to the digital form as the binary digit 0101. The central processing unit (CPU) contains digital logic circuits for necessary calculations. Here all operations are carried out in binary form. The

output of CPU is fed to the decoder which changes the binary signal back to the decimal form. The output display is in the decimal form, showing the original number 5.

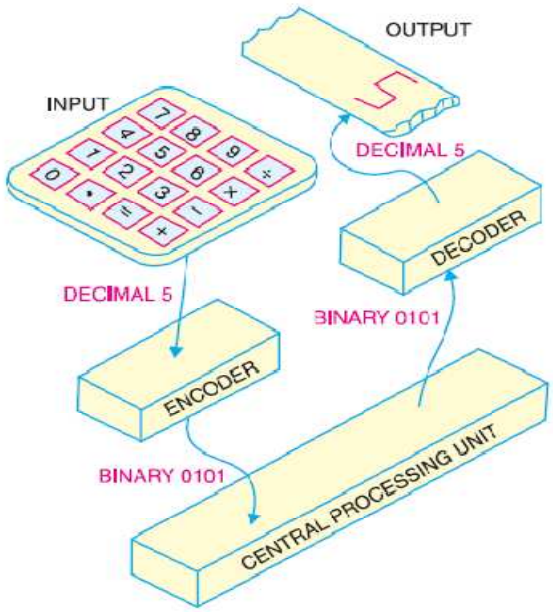


Fig. 4.43 Encoding and decoding in a calculator

Encoder

An *encoder* is a multiplexer without its single output line. It is a combinational logic circuit (function) that has 2^n (or fewer) input lines and n output lines, which correspond to n selection lines in a multiplexer. The n output lines produce the binary code for the possible 2^n input lines. The Fig.4.44 shows the block diagram of an encoder.

Block diagram

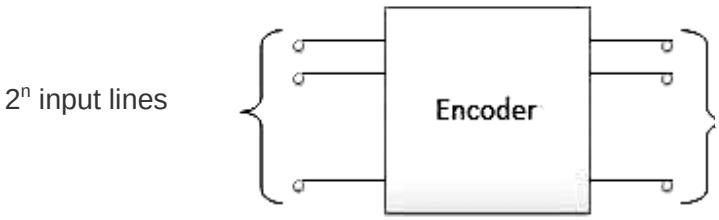


Fig. 4.44 Block diagram of an encoder

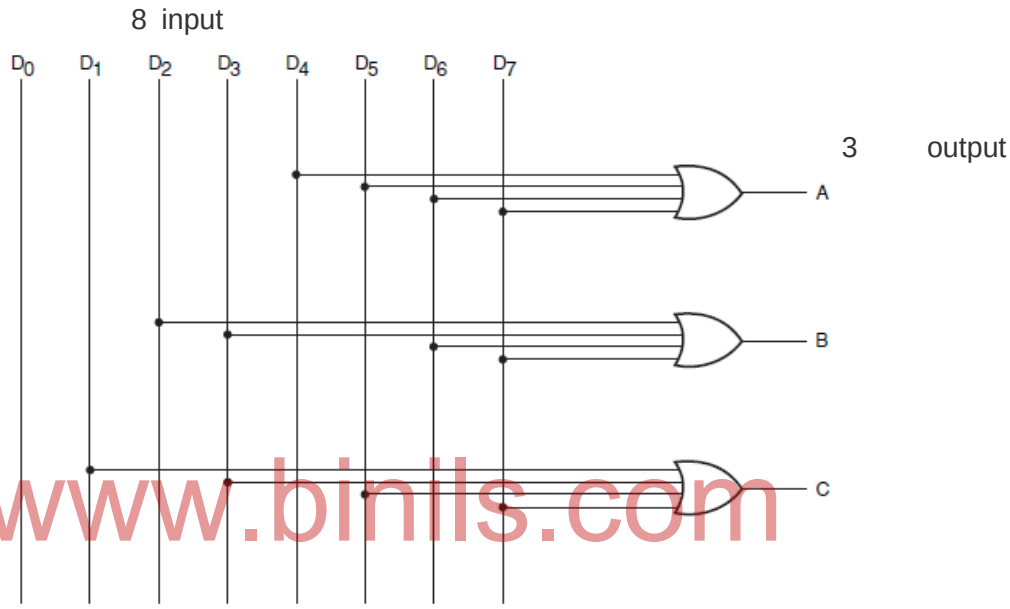


Fig. 4.45 (a) Logic diagram of octal to binary encoder

D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	A	B	C
1	0	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	1	0
0	0	0	1	0	0	0	0	0	1	1
0	0	0	0	1	0	0	0	1	0	0
0	0	0	0	0	1	0	0	1	0	1
0	0	0	0	0	0	1	0	1	1	0
0	0	0	0	0	0	0	1	1	1	1

Fig. 4.45 (b) Truth table of an octal to binary encoder

Let us take the case of an octal-to-binary encoder as shown in figure 4.45 (a). Such an encoder would have eight input lines, each representing an octal digit, and three output lines representing the three-bit binary equivalent. The truth table of such an encoder is

given in Fig.4. In the truth table, D0 to D7 represent octal digits 0 to 7. Any one of the input is given at a time. The corresponding OR gates connected with the input are activated. The 3 outputs A, B and C represent the binary equivalent to the given input octal digit.

Examples of Encoders are following.

- Priority encoders
- Decimal to BCD encoder
- Octal to binary encoder
- Hexadecimal to binary encoder

Decoder

A decoder is a combinational circuit that decodes the information on **n input** lines to a maximum of **2^n unique output** lines. Figure 4.46 shows the circuit representation of 2-to-4, 3-to-8 and 4-to-16 line decoders. If there are some unused or 'don't care' combinations in the n-bit code, then there will be fewer than 2^n output lines. As an illustration, if there are three input lines, it can have a maximum of eight unique output lines. In the three-bit input code, if only the following three-bit combinations 000, 001, 010, 100, 110 and 111 (011 and 101 being either unused or don't care combinations) are used, then this decoder will have only six output lines. In general, if n and m are respectively the numbers of input and output lines, then $m \leq 2^n$. A decoder can generate a maximum of 2^n possible minterms with an n-bit binary code.

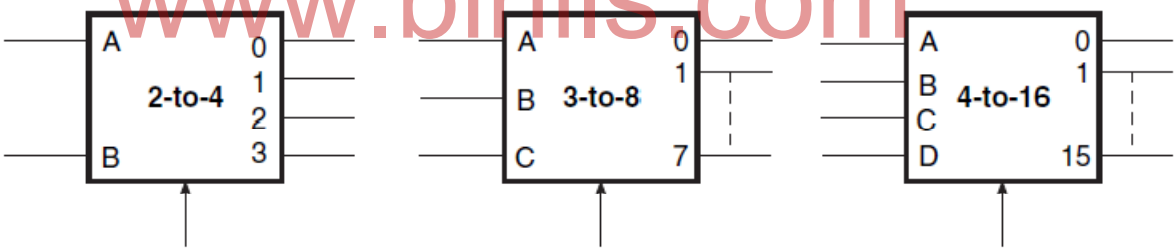
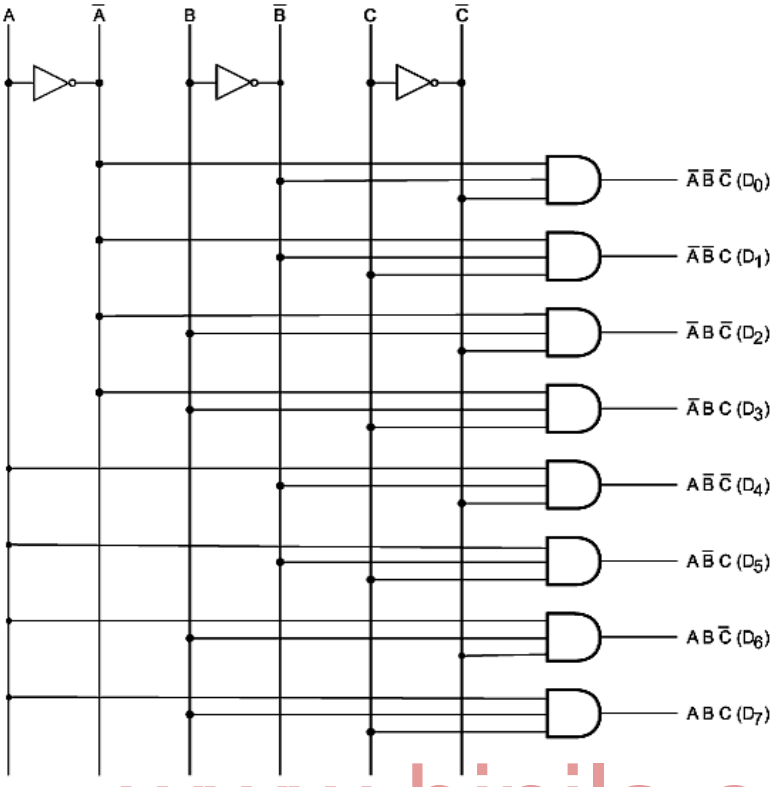


Fig. 4.46 Circuit representation of 2-to-4, 3-to-8 and 4-to-16 line decoders

In order to illustrate further the operation of a decoder, consider the logic circuit diagram in Fig.4.47. This logic circuit implements a 3-to-8 line decoder function. This decoder has three inputs designated as A, B and C and eight outputs designated as D0, D1, D2, D3, D4, D5, D6 and D7. From the truth table given along with the logic diagram it is clear that, for any given input combination, only one of the eight outputs is in logic '1' state. Thus, each output produces a minterm that corresponds to the binary number currently present at the input. In the present case, D0, D1, D2, D3, D4, D5, D6 and D7 respectively represent the following minterms:

$$D_0 \rightarrow \overline{A}.\overline{B}.\overline{C},\quad D_1 \rightarrow \overline{A}.\overline{B}.C,\quad D_2 \rightarrow \overline{A}.B.\overline{C},\quad D_3 \rightarrow \overline{A}.B.C$$

$$D_4 \rightarrow \overline{A}.\overline{B}.\overline{C},\quad D_5 \rightarrow A.\overline{B}.C,\quad D_6 \rightarrow A.B.\overline{C},\quad D_7 \rightarrow A.B.C$$



INPUTS			OUTPUTS							
A	B	C	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	1	0	0	0	0
1	0	0	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	1	0	0
1	1	0	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	1

Fig. 4.47 Logic diagram and truth table of 3-to-8 decoder.

4.5.5 Digital Comparator

A magnitude digital comparator is a combinational circuit that compares two digital or binary numbers (consider A and B) and determines their relative magnitudes in order to find out whether one number is equal, less than or greater than the other digital number.

Three binary variables are used to indicate the outcome of the comparison as A>B, A<B, or A=B. The below figure 4.48 shows the block diagram of a n-bit comparator which compares the two numbers of n-bit length and generates their relation between themselves

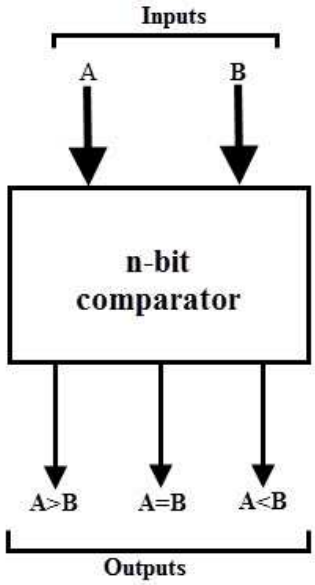


Fig. 4.48 Block diagram of n-bit comparator

These comparators can compare 2-bit, 4-bit and 8-bit numbers depending on the application requirement. These are available in TTL as well as CMOS logic family ICs.

Single Bit Comparator

A comparator used to compare two bits, i.e., two numbers each of single bit is called a **single bit comparator**. It consists of two inputs for allowing two single bit numbers and three outputs to generate less than(<), equal (=) and greater than(>) as comparison outputs.

The figure 4.49 (a) below shows the block diagram of a single bit magnitude comparator. This comparator compares the two bits and produces one of the 3 outputs as L (A<B), E (A=B) and G (A>B).

Fig 4.49 (a) Block diagram of single bit comparator

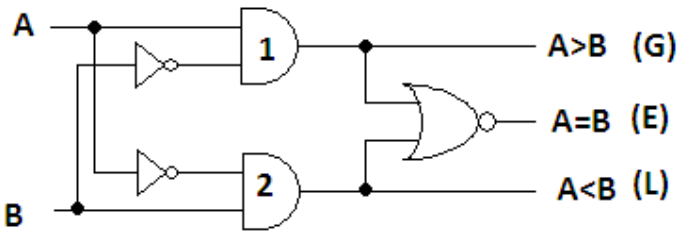


Fig 4.49 (b) Logic diagram of single bit comparator

The logic diagram in Fig 4.49 (b) has two inputs A and B, and three outputs for A>B (G), A=B (E) and A<B (L). The output of AND gate 1 for A>B will be 1 only when A=1 and B=0. The output of AND gate 2 will be 1 when A=0 and B=1 which is A<B. When the inputs A and B are equal (E), the output of both AND gates are 0s. It enables the output of NOR gate as 1. The output is shown in the truth table.

A_0	B_0	L	E	G
0	0	0	1	0
0	1	1	0	0
1	0	0	0	1
1	1	0	1	0

Truth table of single bit comparator

It is to be noted that E can be realized as (L + G)

2-Bit Comparator

A 2-bit comparator compares two binary numbers, each of two bits and produces their relation such as one number is equal or greater than or less than the other. The figure 4.50 shows the block diagram of a two-bit comparator which has four inputs and three outputs.

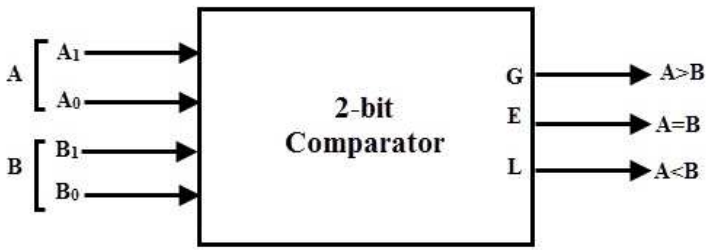


Fig. 4.50 Block diagram of two bit comparator

The first number is designated as A = A1A0 and the second number is designated as B = B1B0. This comparator produces three outputs as G (G = 1 if A>B), E (E = 1, if A = B) and L (L = 1 if A<B). The truth table of this 2 bit comparator is shown below which lists various input and output states.

Inputs				Outputs		
A_1	A_0	B_1	B_0	A>B	A=B	A<B
0	0	0	0	0	1	0
0	0	0	1	0	0	1
0	0	1	0	0	0	1
0	0	1	1	0	0	1
0	1	0	0	1	0	0
0	1	0	1	0	1	0
0	1	1	0	0	0	1
0	1	1	1	0	0	1
1	0	0	0	1	0	0
1	0	0	1	1	0	0
1	0	1	0	0	1	0
1	0	1	1	0	0	1
1	1	0	0	1	0	0
1	1	0	1	1	0	0
1	1	1	0	1	0	0
1	1	1	1	0	1	0

The figure 4.51 shows the logic diagram of a 2-bit comparator using basic logic gates. The logical equations are specified for each condition. It is also possible to construct this comparator by cascading of two 1-bit comparators.

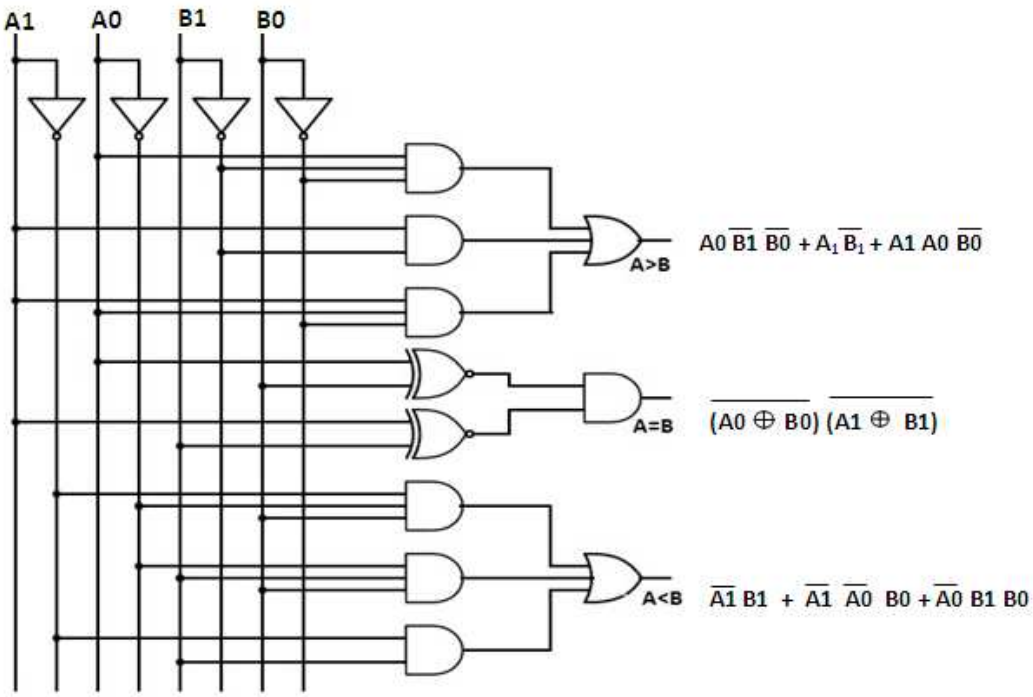


Fig. 4.51 Logic diagram with logical equations for 2 bit comparator

Applications of Comparators

These are used in

- Address decoding circuitry in computers and microprocessor based devices to select a specific input/output device for the storage of data.
- Control applications in which the binary numbers representing physical variables such as temperature, position, etc. are compared with a reference value. Then the outputs from the comparator are used to drive the actuators so as to make the physical variables closest to the set or reference value.
- Process controllers
- Servo-motor control

Review Questions

Part A

1. List the names and the base values for various number systems.
2. Convert the decimal number 75 into binary.
3. Convert the Hexa decimal number 2A into other number systems.
4. Define ASCII and BCD codes.
5. Specify the range of ACII values for the English alphabets.
6. What is meant by parity bit?
7. What is the use of parity bit?

8. What is the disadvantage of parity bit in error detection?
9. Draw the logic diagram for odd parity generator.
10. Draw the symbols of XOR and NAND gates.
11. Write the truth table for 2-input Ex-NOR gate.
12. Define universal gates.
13. What is the importance of NAND gate?
14. What is Boolean algebra?
15. What is the importance of De Morgan's theorems in Boolean algebra?
16. Give two differences between decimal and binary systems.
17. What are the advantages of Boolean theorems?
18. How will you obtain NOT gate from NAND gate?
19. What is indicated by plus (+), dot (.) and bar (—) in a Boolean expression?
20. Most of information we handle is in decimal form. Will a digital circuit process this information as such?
21. Draw a Karnaugh map using 3 variables.
22. Define positive logic system.
23. Define commutative law of Boolean algebra.
24. Define DeMorgan's theorem.
25. List the methods used to minimize the logical expressions.
26. Define duality theorem.
27. What is the relationship between the number of variables and the number of cells for a Karnaugh map?
28. How the cells can be grouped in a Karnaugh map?
29. Define redundant groups.
30. What are advantages of K-Maps?
31. What are the drawbacks of K-Maps?
32. What are the outputs of adder circuits?
33. Define half adder and full adder.
34. Draw the logic circuit of half adder.
35. Draw the truth table for full-subtractor.
36. Define multiplexer.
37. Define demultiplexer.
38. What role is played by encoder and decoder?
39. What is the function of a comparator circuit?

SEQUENTIAL LOGIC SYSTEM

Objectives :

At end the this unit, students can

- Define the flip flop and state the types of flip-flops
- Explain the operation of SR, D, T and JK flip-flops
- State the need of JKMS
- Define Race condition
- Mention the technique to avoid race condition
- Define the counter and state the types of counters
- Describe the working of counter
- Design the counter circuit
- Differentiate between synchronous and asynchronous counters
- State the types of Shift register
- Explain the Serial and Parallel modes of Read and Write operations
- State the applications of Shift register

Introduction

In our daily life, we see the currency counting machines or the machine which counts the persons entering a particular place. All these types of machines are basically a counter circuit. The same counter circuit is also present inside the CPU of the computer. The working of counter depends on flip flop, which is the basic building block of counter.

We hear the term main memory or RAM in computer, mobile phones. This is another application of flip-flops. This memory is made up of registers, which are used for storing temporary data in computer, mobile phones.

We are using USB modems, which needs conversion of data transmission from parallel to serial mode and vice versa. All these conversions are the applications of shift registers.

All these circuits, flip-flops, counters and Shift registers are interlinked and the knowledge of these circuits is much needed for understanding computer architecture.

Flip flops

Basic Principle of Operation

Digital logic circuits are classified into two types. These are,

1. Combinational logic circuits
2. Sequential logic circuits

Combinational circuit is a circuit, whose output depends on inputs only. Examples: Logic gates, adder and subtractor circuits, multiplexer, de-multiplexer, encoder, decoder, etc.

Sequential logic circuit is a circuit, whose output depends on both inputs and previous outputs. It contains memory element, which stores previous output. Examples are counters, shift registers, etc.

Flip Flops

Flip Flop is a logic circuit, used to store a binary bits (0 or 1). It is also called bi-stable storage element or Latch. It is used in constructing memory registers, digital counters and shift registers, etc.

The following are the different types of flip flops :

i. SR flip flop
ii. JK flip flop
iii. D flip flop
v. T flip flop

Four Output Conditions(states) of Flip flop

A Flip flop has one or two inputs (S and R or J and K or T or D) and two outputs Q and Q'. The outputs Q and Q' are always complementary to each other. That is, if Q = 1 then Q' = 0 also if Q = 0 and Q' = 1. The output Q is represented as Q_1, Q_2, Q_3. It means that if Q_2 is present output, then Q_1 is the previous output. If Q_3 is the present output then Q_2 is the previous output. Generally, it is written as Q_{n-1}, Q_n. The output of the flip flop are named as states or conditions . The various states or conditions of the flip flops are,

1. Set state
2. Reset state
3. No change state
4. Toggle state

1. Set state

Whatever may be the inputs and previous output Q_{n-1}, if the present output Q_n= 1 and Q'_n = 0, then it is called set condition or set state.

2. Reset condition

Whatever may be the inputs and previous output Q_{n-1}, if the present output Q_n= 0 and Q'_n = 1, then it is called reset condition or reset state.

3. No Change condition

Whatever may be the inputs and previous output Q_{n-1}, if Q_n ,and Q_n' are same as Q_{n-1},and Q'_{n-1}, then it is called No Change condition or No change state.

4. Toggle condition

Whatever may be the inputs, if Q_n and Q'_n are as complementary of Q_{n-1}, and Q'_{n-1}, then it is called Toggle condition. That is, if Q_{n-1}= 1, then Q_n =0 and if Q_{n-1}= 0, then Q_n =1 .

Triggering

The digital circuits are to work in synchronous with other circuits. Synchronous means that all the circuits are to work in the predefined instant (time). The synchronous is achieved by applying clock signals. The clock signal activates the circuit. This means, even though, the input are applied to the circuit, the output will occur only at the time of arrival of clock signal. It may be also stated as only the clock pulse, makes the circuit to work.

Clock Signals

Clock signal are continuous stream of electrical pulses. Each pulse has one high voltage and low voltage. They are called high level and low level. The clock pulse is in high level for some micro seconds and in the low level for same micro seconds. The clock pulse is applied as one of the inputs to the digital circuits. This is used to enable the circuit i.e. To it make work. The clock pulse is diagrammatically represented as below :

Fig 5.1 Clock Pulse

The application of clock pulse to the circuits is called triggering. After triggering only, the circuit work and produce output. There are two types of triggering :

1. Level Triggering
2. Edge Triggering

Level Triggering

Level triggering means the circuit will be triggered or enabled, when the clock pulse is in high level or low level. These types of circuits are called level triggered circuits. A circuit has been designed such that it will be triggered either by the high level or by the low level, but not by both. Therefore, level triggering is classified into two types :

1. High level Triggering
2. Low level Triggering

Some circuits are high level triggering and some others are low level triggering. This is represented in the circuit, by the following symbols.

Fig 5.2 Level Triggering

Since, the clock pulse is in high level or low level for some number of micro seconds, the circuit is continuously triggered for the same number of micro seconds. For example, if the high level triggering applied to a flip flop, it changes its states or outputs many number of times for the same input. But, for stable output, the output has to occur only once for one set of inputs. This is the main drawback in level triggering. This will be avoided in the edge triggering.

Edge Triggering

In a single clock pulse, there are two transitions. In the beginning, the pulse changed from low voltage to high voltage then high voltage to low voltage. These two transitions are called edges. The changes in the clock pulse from low voltage to high voltage is called positive edge or leading edge and changes from high voltage to low voltage is called negative edge or trailing edge. These edges are used to trigger the circuits. These types of circuits are called edge triggered circuits.

Based on the type of edges, edge triggering is divided into two types :

1. Positive edge triggering
2. Negative edge triggering

Some circuits are positive edge triggering and some others are negative edge triggering. The type of triggering is represented in the circuit as below :

5.3 Edge Triggering

Positive Edge Triggering

The circuit will be triggered or enabled at the moment of clock pulse changing from low to high level. This is called positive edge triggering or leading edge triggering. These types of circuits are called positive edge triggered circuits.

Negative Edge Triggering

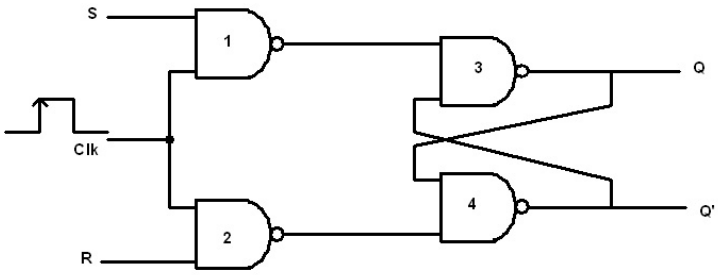
The circuit will be triggered at the moment of the clock pulse changing from high level to low level. This is called negative edge triggering or trailing edge triggering. These types of circuits are called negative edge triggered circuits.

Note :

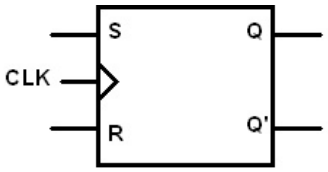
Before understanding the circuit operation of the flip flop, the truth table of NAND is reminded here. When both inputs of the NAND gate are 1, output will be 0. When one or both inputs are 0, then output will be 1.

SR Flip Flop

SR flip flop is a basic flip flop with two inputs S and R. The outputs are named as Q and Q'. The inputs S means Set, R means Reset. The input S is used to Set the flip flop i.e. for storing 1 in the flip flop and R is used to reset the flip flop i.e. for storing 0 in the flip flop. The below figure shows clocked SR flip flop high activated.



5.4.a SR Flip Flop Circuit



5.4 b SR Flip Flop Symbol

A flip flop may be constructed either by NAND or NOR gates. The S R flip flop constructed with NAND gate is shown in the figure. The output of NAND gate 4 as given as one of input to NAND gate 3 and similarly the output of NAND gate 3 is given as one of the inputs to NAND gate 4. This cross connection is known as feedback.

The working of the flip flop is explained with the truth table with the equation

$Q_{n+1} = S + R'Q_n$

CLK	Input		Output		Remarks
	S	R	Q_n	Q_{n-1}	
↑	0	0	Q_{n-1}	Q'_{n-1}	No Change
↑	0	1	0	1	Reset
↑	1	0	1	0	Set
↑	1	1	Forbidden		Not allowed

No Change condition

When S = 0 and R = 0, on the application of clock pulse, the flip flop give no change in the output. It maintains the previous state Q_{n-1} and Q'_{n-1}. Let us assume that $Q_{n-1} = 0$ and $Q'_{n-1} = 1$. If S = 0 and R = 0, output of NAND gate 1 is 1 and NAND gate 2 is 1. The output of NAND gate 3 is 0 as its both inputs are 1 and output of NAND gate 4 is 1 as its one of the input is 0. According to the equation

$Q_n = S + R'Q_{n-1}$ (S = 0, R' = 1, Q_{n-1} = 0)
= 0 + 1.0
= 0 ie. Q_{n-1}

Similarly we can work for Q_{n-1} = 1

Reset condition

When S = 0 and R = 1, on the application of clock pulse, the flip flop give Q_n = 0 and Q'_n = 1. Let us assume that Q_{n-1} = 1 and Q'_{n-1} = 0. If S = 0 and R = 1, output of NAND gate 1 is 1 and NAND gate 2 is 0. The output of NAND gate 3 is 0 as its both inputs are 1 and output of NAND gate 4 is 0 as its one of the input is 0. . According to the equation

$Q_n = S + R'Q_{n-1}$ (S = 0, R' = 0, Q_{n-1} = 1)
= 0 + 0.1
= 0

Similarly we can work out for Q_{n-1} = 0.

Set condition

When S = 1 and R = 0, on the application of clock pulse, the flip flop give Q_n = 1 and Q'_n =0. Let us assume that Q_{n-1} = 0 and Q'_{n-1} = 1. If S = 1 and R = 0, output of NAND gate 1 is 0 and NAND gate 2 is 1. The output of NAND gate 3 is 1 as its one of the inputs is 0 and output of NAND gate 4 is 1 as its both inputs are 1. According to the equation

$Q_n = S + R'Q_{n-1}$ (S = 1, R' = 1, Q_{n-1} = 0)
= 1+ 1.0
= 1

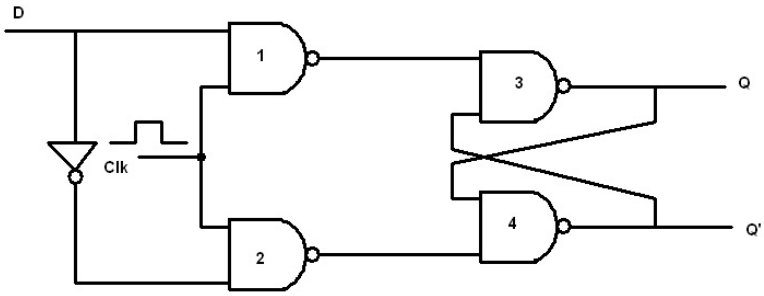
Similarly we can work out for Q_{n-1} = 1.

Forbidden condition

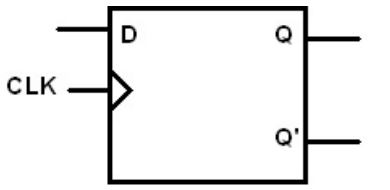
When both S = 1 and R = 1, on the application of clock pulse, the output of the flip flop is undetermined. The output Q_n may be 0 or 1. This is determined by the race condition of the NAND gates. Hence this input is not allowed in S R Flip flop.

D Flip Flop

D flip flop is a modified version of SR flip flop. The two inputs S and R are combined into a single input using a NOT gate as given below.



5.5.a DFlip Flop Circuit



5.5.b D Flip Flop Symbol

The input is named 'D'. The symbol D denote 'Data' or 'Delay'. As it is used to store Data 0 or 1, it is called Data flip flop. Sometimes, it is used to give delay in the circuit so it is also called 'Delay' flip flop. Since it has only one input, the output has only two states. There are

i. Set (storing 1 in the flip flop)
ii. Reset (storing 0 in the flip flop)

Its operation is explained using the truth table give below:

CLK	Input	Output		Remarks
	D	Q_n	Q'_n	
↑	0	0	1	Reset state, equal to S = 0 , R = 1
↑	1	1	0	SET state, equal to S = 1, R = 0

RESET State

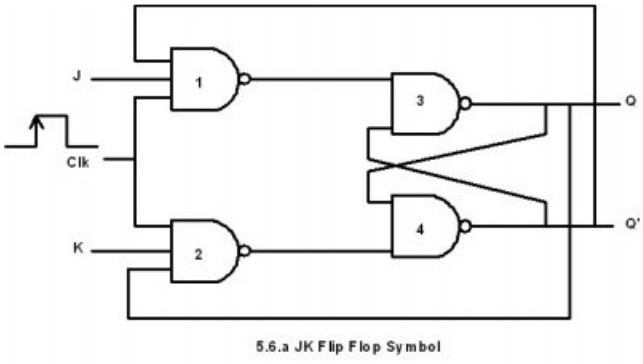
When D = 0, which is equal to S = 0 and R = 1, the output will be $Q_n = 0$ and $Q'_n = 1$.

SET State

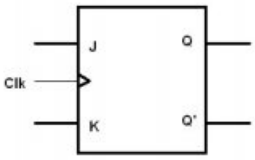
When D = 1, which is equal to S = 1 and R = 0, the output will be $Q_n = 1$ and $Q'_n = 0$.

JK Flip Flop

The JK Flip flop is the refined SR flip flop. The forbidden state in the SR flip flop is avoided in the JK Flip Flop. Here, S input is named J and R input is named K. The forbidden state is changed into Toggle state. When both the inputs are 1, the output will be a Toggled one. Toggle means present output is the complement of the previous output.



5.6.a JK Flip Flop Symbol



5.6.b JK Flip Flop Symbol

In addition to the cross connection between NAND gates 3 and 4, the output of NAND 4 is given as one of the input to NAND gate 1 and output of NAND gate 3 is given as one of the input to the NAND gate2. This feedback avoids forbidden and gives toggle output.

The operation is explained as per truth table given :

CLK	Input		Output		Remarks
	J	K	Q_n	Q'_n	
	0	0	Q_{n-1}	Q'_{n-1}	No Change
	0	1	0	1	Reset
	1	0	1	0	Set
	1	1	Q'_{n-1}	Q_{n-1}	Toggle

The working is same S R flip flop for the first 3 conditions No change, Reset and Set conditions. The output is determined using the equation :

$$Q_n = JQ'_{n-1} + K'Q_{n-1}$$

No Change state :

When J = 0, K = 0, on the application of clock pulse, the remains in the same state. For example, let us assume that $Q_{n-1} = 0$ and $Q'_{n-1} = 1$, according to the equation, the output will be,

$Q_n = 0.1 + 1.0$ ($J = 0, Q'_{n-1} = 1, K' = 1, Q_{n-1} = 0$)

$Q_n = 0$

Similarly, we can work out for the case $Q_{n-1} = 0$.

Set State :

When J = 1, K = 0, on the application of clock pulse, 1 will be stored in the flip flop. For example, let us assume that $Q_{n-1} = 0$ and $Q'_{n-1} = 1$, according to the equation, the output will be,

$Q_n = 1.1 + 1.0 = 0.$ ($J = 1, Q'_{n-1} = 1, K' = 1, Q_{n-1} = 0$)

$Q_n = 1$

Similarly, we can work out for the case $Q_{n-1} = 1$.

Reset State :

When J = 0, K = 1, on the application of clock pulse, 0 will be stored in the flip flop. For example, let us assume that $Q_{n-1} = 1$ and $Q'_{n-1} = 0$, according to the equation, the output will be,

$Q_n = 0.0+0.1$ ($J = 0, Q'_{n-1} = 0, K' = 0, Q_{n-1} = 1$)
$Q_n = 0$

Similarly, we can work out for the case $Q_{n-1} = 0$.

Toggle condition :

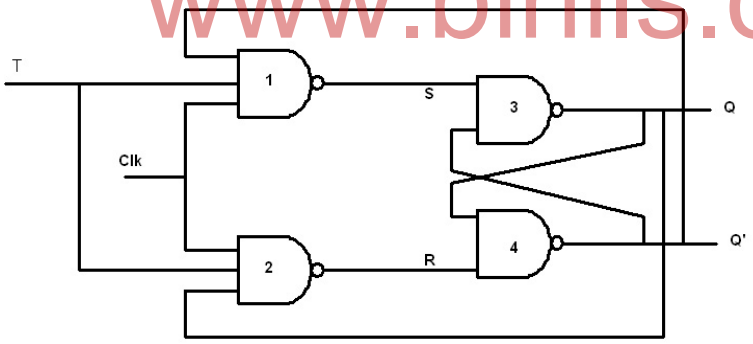
When J = 1, K = 1, on the application of clock pulse, 0 the output will be the complement of the previous state. For example, let us assume that $Q_{n-1} = 1$ and $Q'_{n-1} = 0$, according to the equation, the output will be,

$Q_n = 1.0+0.1$ ($J = 1, Q'_{n-1} = 0, K' = 0, Q_{n-1} = 1$)
$Q_n = 0$

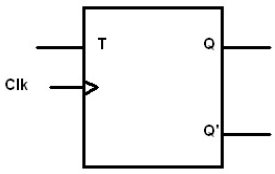
Similarly, we can work out for the case $Q_{n-1} = 0$.

T Flip flop

T flip flop is the modified version of JK flip flop. The inputs J and K are combined into to single input T. The name T indicates 'Toggle'. The circuit diagram is as given below:

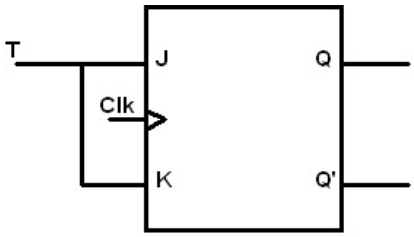


5.7.a T Flip Flop Circuit



5.7.b. T Flip Flop Symbol

The equivalent circuit for T flip flop is as given :



5.8 Equivalent T Flip Flop

Since, it has one input, it has two possible output states. Its operation is explained as given below using truth table.

CLK	Input	Output		Remarks
	T	Q_n	Q'_n	
↑	0	Q_{n-1}	Q'_{n-1}	No Change state, equal to J = 0, K = 0
↑	1	Q'_{n-1}	Q_{n-1}	Toggle State, equal to J =1, K = 1

No Change State :

When T = 0, on the application of clock pulse, the output remains in the previous state.

Toggle State :

When T = 1, on the application of clock pulse, the output will be the complement of the previous state.

Level Triggered Flipflop

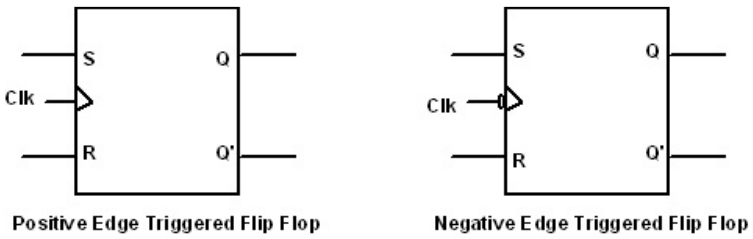
If the flip flop is triggered by High or Low level state of the clock pulse, that flip flop is called level triggered flip flop. It may be High level triggered and Low level triggered flip flop. The symbols are as given below :

High Level Triggered Flip Flop Low Level Triggered Flip Flop

Fig 5.9 Level Triggered Flip Flop

Edge Triggered Flip flop

If the flip flop is triggered by leading or trailing edge of the clock pulse, that flip flop is called edge triggered flip flop. It may be positive edge triggered and negative edge triggered flip flop. The symbols are as given below :



Positive Edge Triggered Flip Flop Negative Edge Triggered Flip Flop

5.10 Edge Triggered Flip Flop

Race Condition and Need for Master Slave Flipflop:

Propagation delay is the time difference between two instants,

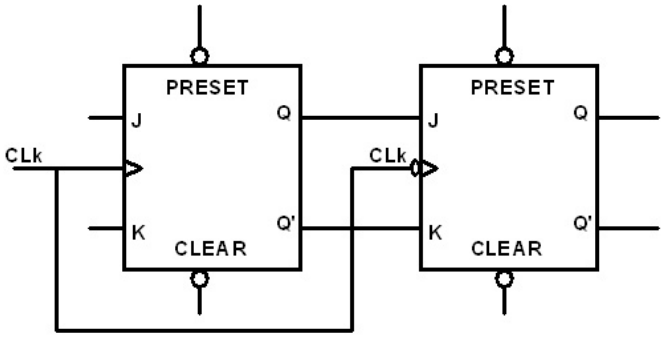
1. Time at which inputs appear in the circuit and

2. Time at which output available in the circuit.

Normally, the propagation delay is about 15ns. In order to get stable output, the width of the clock pulse should be greater than the propagation delay. But, in the simpler circuit like flip flops, the width of clock is smaller than the propagation delay of the flip flop, hence, the output of the flip flop is unpredictable. This means that, the output changes many times, before final output occurs. This is called Race condition. This race condition is the common problem in level triggered and in some case of edge triggered flip flop. Race condition is avoided using Master Salve flipflop.

Master Slave JK Flip flop :

The master slave JK flip flop is combination of two JK flip-flops, one JK flip flop acts as Master and other JK flip flop acts as Slave. The output of the master JK flip flop is given as input to slave JK flip flop. The master JK flip flop is positive edge triggered flip flop and slave JK flip flop is the negative edge triggered flip flop. The arrangement is the solution to avoid the race condition problem in the flip-flops.



5.11 Master Slave Flip Flop

In the above figure, master JK flip flop is the positive edge triggered flip flop, slave JK flip flop is the negative edge triggered flip flop. During triggering, master JK is activated on positive edge of the clock pulse, slave JK is deactivated. On the negative edge of the clock pulse, master JK is deactivated and slave JK is activated. The truth table and working principle are same as JK flip flop.

CLK	Input		Output of master JK		CLK	Output of slave JK		Remarks
	J	K	Q_n	Q'_n		Q_n	Q'_n	
↑	0	0	Q_{n-1}	Q'_{n-1}	↓	Q_{n-1}	Q'_{n-1}	No Change
↑	0	1	0	1	↓	0	1	Reset
↑	1	0	1	0	↓	1	0	Set
↑	1	1	Q'_{n-1}	Q_{n-1}	↓	Q'_{n-1}	Q_{n-1}	Toggle

In addition to J, K and Clock inputs, it has two additional inputs. They are

i. PRESET input
ii. CLEAR input

PRESET input

This is active LOW signal, which means that when low voltage is given to this signal, it is activated. When activated, 1 is stored directly in the flip flop. A high voltage or 1 does not affect this input.

CLEAR input

This is another active LOW signal. When low voltage or 0 given to this input, 0 is stored directly in the flip flop. A high voltage or 1 does not affect this input.

Counters

Counter is a sequential circuit used to count the input signals or time duration. It is made up of cascaded arrangement of flip-flops (T or JK flip-flops). Cascading means the output of first flip flop is given as input to second flip-flop. There are two types of flip-flops.

i. Ripple counter or Asynchronous counter or Serial counter
ii. Synchronous counter or Parallel counter

The number of counts depends on number of flip-flops connected. The number of counts is calculated using the formula 0 to 2^N-1. The variable N indicates number of flip-flops. The number of counts and number of flip-flops are given below :

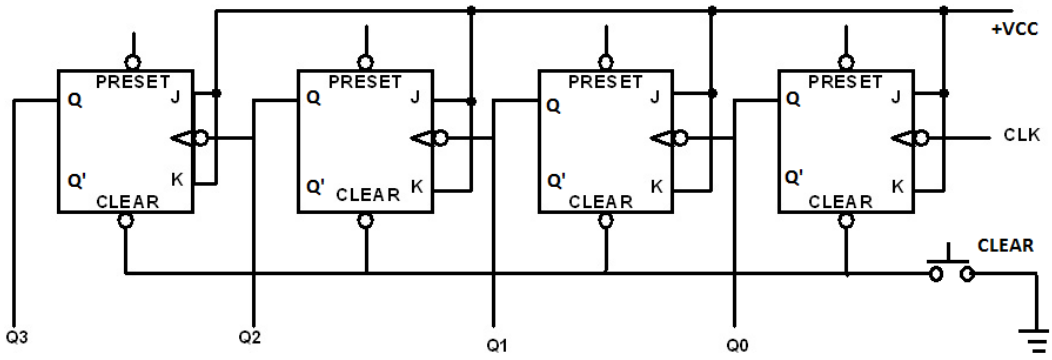
No of flip flops	No of counts	Counts in binary	Counts in decimal
1	2	0, 1	0, 1
2	4	00,01,10,11	0 to 3
3	8	000,001,010,011,100,101,110,111	0 to 7
4	16	0000,0001, to 1111	0 to 15

Need for counters

Counters are used to count things or persons or movements. Digital circuits need to count some events, before taking a certain decision. For example, the print head in the dot matrix printer moves from left side to right side and comeback. The number of steps it has to move is counted by the counter and it informs the control circuit when the head reaches the end of the line. The same principle is also used in Read/Write head movement in Hard disk, DVD. Some other applications are counting persons crossing a line, counting the currency notes.

Four Bit Ripple Counter

It is made up of 4 numbers of T or JK flip-flops. It counts from 0000 to 1111 in binary, 0 to 15 in decimal. The output of first flip flop is given as clock input to second flip flop. The output of second flip flop is given as clock input to the third flip flop and so on. All the flip-flops are given inputs J =1 and K = 1. Therefore, it toggles on every occurrence of clock pulses.



5.13 4 Bit Ripple Counter

Q0,Q1,Q2,Q3 --> COUNTER OUTPUTS

Working of counter

The JK flip flop used in the counters are negative edge triggered and all are given inputs J = 1 and K = 1. So, it changes its state 0 to 1 or 1 to 0 on every negative edge of the clock pulse. Initially all the flip-flops are cleared using CLEAR inputs. It's outputs are

Output				No of clock pulses
Q3	Q2	Q1	Q0	
0	0	0	0	0

When first clock pulse occurs, on its negative edge, the output of Q0 flip flop is changed from 0 to 1, since it's both inputs J = 1 ad K = 1. All other flip-flops are not affected, they have not received clock pulse. Its outputs are,

Output				No of clock pulses
Q3	Q2	Q1	Q0	
0	0	0	0	0
0	0	0	1	1

On the occurrence of second clock pulse, the output of Q0 again changed from 1 to 0 as It toggles on every clock pulse. As Q0 changed from 1 to 0, It gives negative edge clock input to the second flip flop Q1. So, Q1 changes from 0 to 1. The remaining Q2 and Q3 flip-flops are not affected. Now, the output states are as follows :

Output				No of clock pulses
Q3	Q2	Q1	Q0	

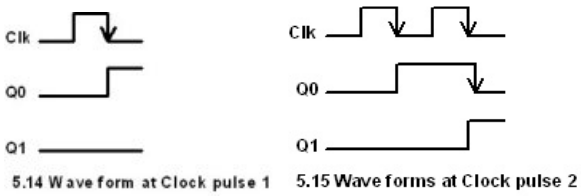
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2

In this way, the output will reach the final count 15 and on 16th clock pulse, it resets to 0000.

Output				No of clock pulses		Output				No of clock pulses
Q3	Q2	Q1	Q0			Q3	Q2	Q1	Q0	
0	0	0	0	0		1	0	0	1	9
0	0	0	1	1		1	0	1	0	10
0	0	1	0	2		1	0	1	1	11
0	0	1	1	3		1	1	0	0	12
0	1	0	0	4		1	1	0	1	13
0	1	0	1	5		1	1	1	0	14
0	1	1	0	6		1	1	1	1	15
0	1	1	1	7		0	0	0	0	16
1	0	0	0	8						

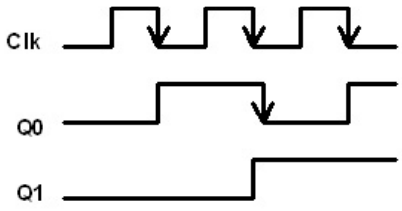
Waveforms

The operation can also be explained using wave forms also. At first, all flip-flops are 0. On the first clock pulse, Q0 changes from 0 to 1, on negative edge of clock pulse. The output will be



5.14 Wave form at Clock pulse 1 5.15 Wave forms at Clock pulse 2

On the second clock pulse, the Q0 changes from 1 to 0. Since it changes from 1 to 0, it becomes negative edge clock pulse to the second flip flop Q1. So, it changes its changes state from 0 to 1.



5.16 Wave forms at clock pulse 3

On the third clock pulse , Q0 changes from 0 to 1. Since, it is a positive edge clock pulse to second flip flop Q1, no change occur in it.

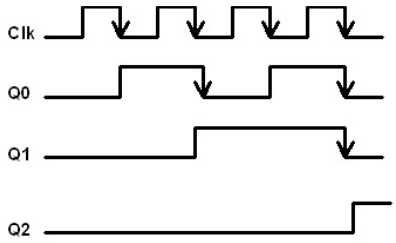


Fig 5.17 Wave forms at clock pulse 4

On the fourth clock pulse, Q0 changes from 1 to 0, Q1 changes from 1 to 0. Q2 changes from 0 to 1.

Similarly for the other cases also. The entire wave forms will be

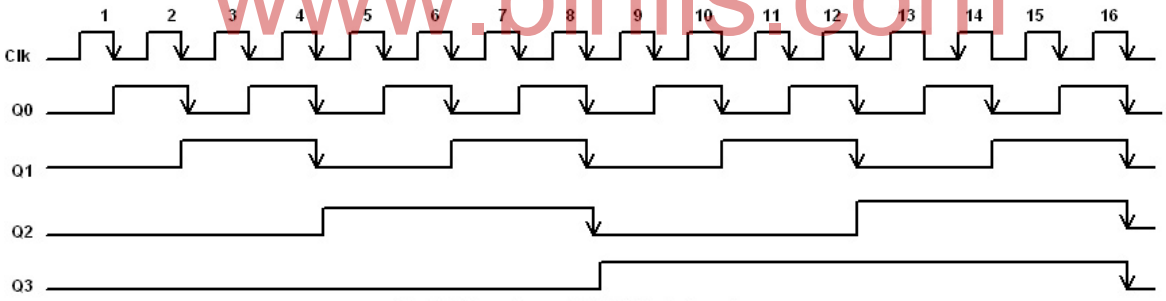


Fig 5.18 Wave forms of 4 bit Ripple Counter

MOD N Counter

If N flip-flops are used in the counter, it counts from 0 to 2^N-1. If it is needed to stop count before it reaches 2^N-1, MOD N counter has to be designed. MOD N counter is a counter, which counts from 0 to N-1 and resets to 0. In other words, this counter resets at Nth count i.e. the MOD 5 counter counts from 0 to 4 and resets at 5^{th} count (It becomes 0 at 5^{th} count). The remaining counts are skipped. Similarly for MOD 12 counter, the counter counts from 0 to 11 and resets at 12th count.

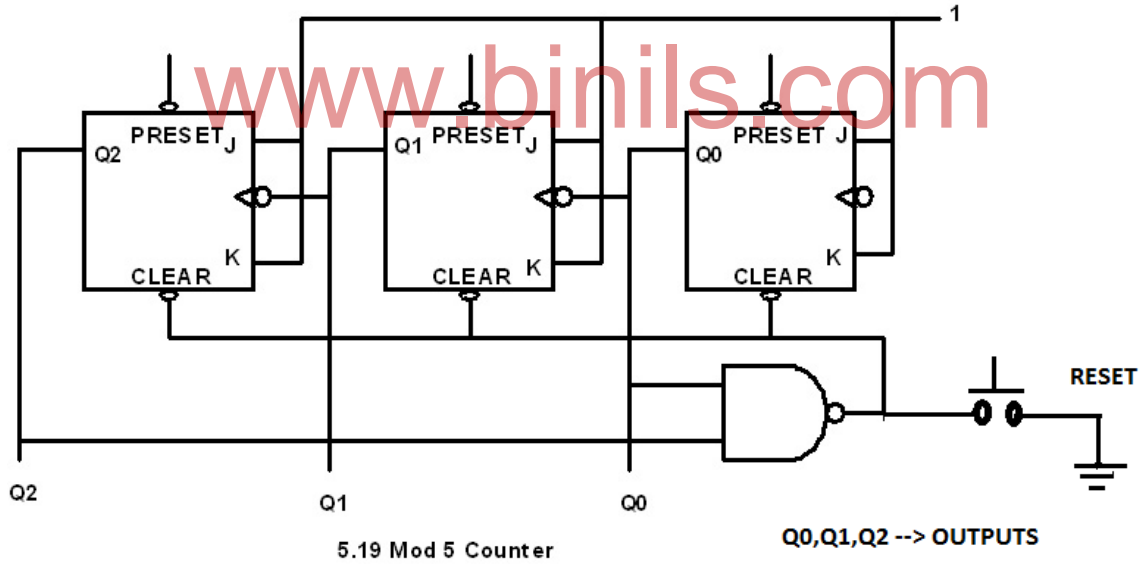
The resetting of counter is done by using a NAND gate, whose active LOW output will be given to CLEAR input of the all the flip-flops. The inputs to the NAND gate is determined by 1s in the count, at which reset has to be done. For example, for MOD 5 counter, to reset at the 5^{th} count 101, the 2 number of 1s in 101 is given as input to NAND gate i.e. the first 1 and

last 1. The table below gives number of flip-flops and where the count stops for some of the MOD counters.

Name of the counter	No of flip-flops needed	Count at which reset to be done	Input to the NAND gate
MOD 5 counter	3 ($0 < 5 < 2^3$-1)	Q2 Q1 Q0 = 1 0 1	Q2, Q0
MOD 6 counter	3 ($0 < 6 < 2^3$-1)	Q2 Q1 Q0 = 1 1 0	Q2, Q1
MOD 9 Counter	4 ($0 < 9 < 2^4$-1)	Q3 Q2 Q1 Q0 = 1 0 0 1	Q3, Q0
MOD 10 counter	4 ($0 < 10 < 2^4$-1)	Q3 Q2 Q1 Q0 = 1 0 1 0	Q3, Q1
MOD 12 counter	4 ($0 < 12 < 2^4$-1)	Q3 Q2 Q1 Q0 = 1 1 0 0	Q3, Q2

MOD 5 Counter

MOD 5 counter is a counter, which counts from 0 to 4 and resets to 0, at 5th count. It is constructed using 3 flip-flops. It counts from 000, 001, 010, 011, 100 and resets i.e., the count will be 000 instead of 101. The reset is done by a NAND gate, whose output is given as input to CLEAR inputs of all flip-flops. The CLEAR input, when activated, stores 0 in the flip flop.



5.19 Mod 5 Counter

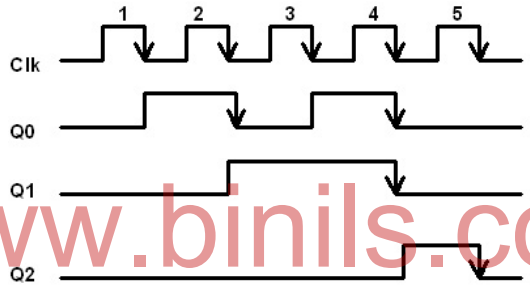
The input to the NAND gate is Q2 and Q0. When the counter reaches 101, Q2 =1, Q1 = 0 and Q0 = 1. Since, Q2 and Q0 has 1, they are given as inputs to NAND gate. The output of NAND gate is HIGH for the count 000 to 100. When 101 occurs, the output of NAND gate is 0 which is given to LOW active input of the CLEAR inputs of all flip-flops. Since, this flip-flop is designed using negative logic, the LOW input activates the CLEAR input of the flip-flops. The CLEAR signal resets the flip flop i.e. stores 0 in the flip flop.

The truth table for MOD 5 counter is as follows :

Output			No of clock pulses
Q2	Q1	Q0	
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
~~1~~	~~0~~	~~1~~	5
0	0	0	

Waveforms of MOD 5 counter

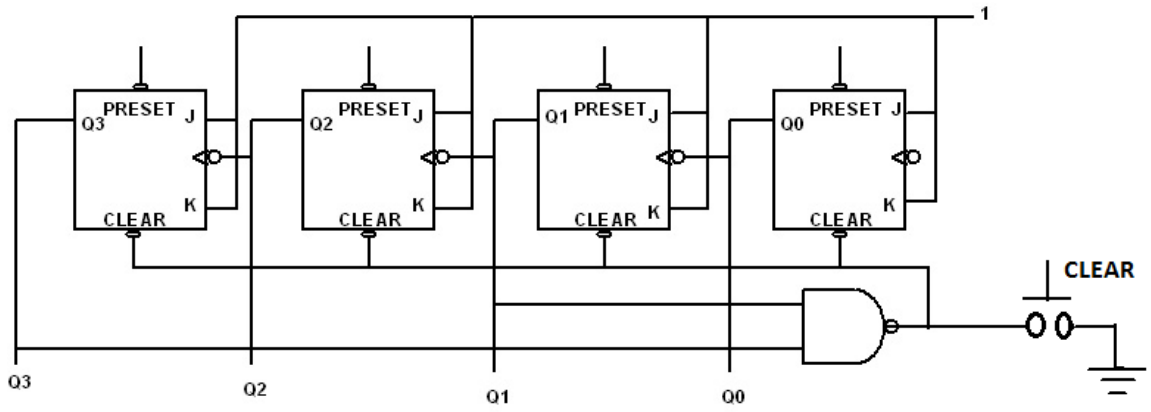
The waveform for MOD 5 counter is as follows. When the count reaches 100, instead of Q2 remaining in 1, it becomes 0.



5.20 Wave forms of Mod 5 Counter

Decade Counter or BCD counter or MOD 10 Counter

Decade counter is a MOD 10 counter, which output will reset at 10^{th} count. It counts from 0000 to 1001 and resets. It is constructed using 4 flip-flops. The reset is done at 10^{th} count ie. when Q3 = 1, Q2 = 0, Q1 = 1 and Q0 = 0. Since, Q3 and Q1 have 1 in it, they are given inputs to NAND gate. The active LOW output of the NAND gate is given as input to CLEAR input of the flip-flops. The CLEAR input resets the flip flop when activated. The circuit is as follows :



5.21 Decade Counter

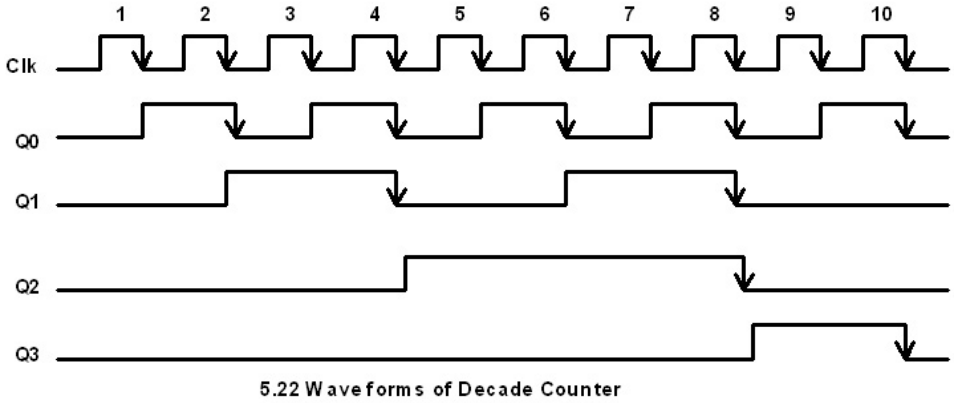
Q0,Q1,Q2,Q3 ---> OUTPUTS

The truth table for decade counter is as follows :

Output				No of clock pulses		Output				No of clock pulses
Q3	Q2	Q1	Q0			Q3	Q2	Q1	Q0	
0	0	0	0	0		0	1	1	0	6
0	0	0	1	1		0	1	1	1	7
0	0	1	0	2		1	0	0	0	8
0	0	1	1	3		1	0	0	1	9
0	1	0	0	4		0	0	0	0	10
0	1	0	1	5						

Waveforms

The waveform will reset at 10th clock pulse as follows :



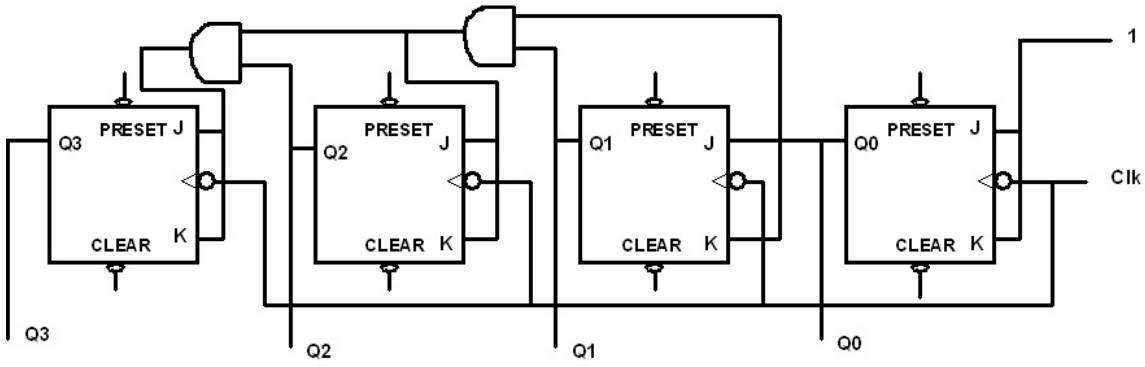
5.22 Waveforms of Decade Counter

4 bit Synchronous Counter or Parallel counter

Synchronous counter is a counter, in which all flip-flops are activated by the same clock pulse is same time i.e. the clock pulse is given to all flip-flops. In ripple counter, the clock pulse is given to first flip flop only. The remaining flip-flops are activated by outputs of previous

flip-flops. Synchronous counter is faster than ripple counter, as it is activated simultaneously. This circuit is complicated than ripple counter. It needs additional logic circuit to toggle flip-flops.

The additional circuit is designed as follows. The second flip flop Q1 is toggled when first flip flop Q0 is 1. The third flip flop Q2 will toggle when first and second flip-flops Q0 and Q1 are 1. The fourth flip flop Q3 will toggle when first, second, third flip-flops Q0, Q1, Q2 are 1. Based on these condition, the logic circuit is designed for 4 bit synchronous counter as follows :



5.23 4 bit Synchronous Counter

Truth Table

The truth table is same as ripple counter.

Output				No of clock pulses		Output				No of clock pulses
Q3	Q2	Q1	Q0			Q3	Q2	Q1	Q0	
0	0	0	0	0		1	0	0	1	9
0	0	0	1	1		1	0	1	0	10
0	0	1	0	2		1	0	1	1	11
0	0	1	1	3		1	1	0	0	12
0	1	0	0	4		1	1	0	1	13
0	1	0	1	5		1	1	1	0	14
0	1	1	0	6		1	1	1	1	15
0	1	1	1	7		0	0	0	0	16
1	0	0	0	8						

Waveforms

The output waveforms is same as ripple counter.

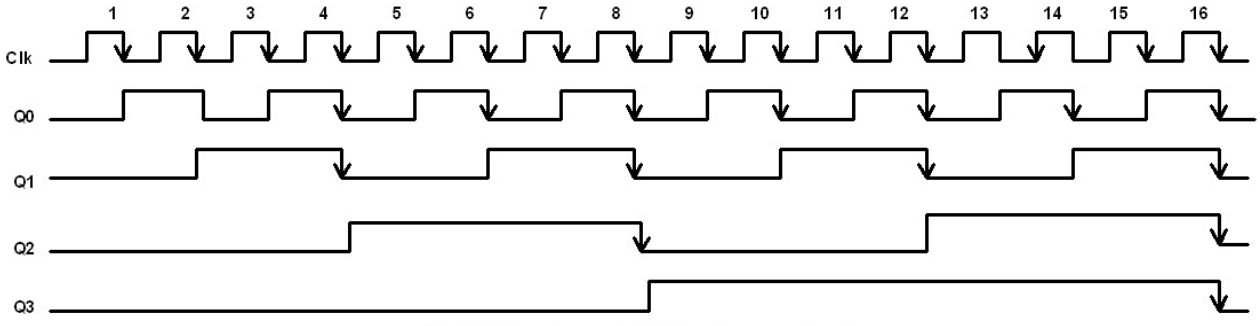


Fig 5.24 Wave forms of 4 bit Synchronous Counter

Difference between Asynchronous and Synchronous counters

Sno	Asynchronous counter	Synchronous counter
1.	It is slower than synchronous counter, as it has large propagation delay.	It is faster, because, the propagation delay is equal propagation delay of single flip flop.
2.	It needs no additional circuit	It needs additional circuit
3.	Clock pulse is applied to first flip flop only	Clock pulse is applied to all flip-flops
4.	Its circuit is simpler	Its circuit is complex than ripple counter
5.	Delay is high	Delay is low
6.	Total propagation delay is sum of propagation delays of all flip-flops	Total propagation delay is equal to propagation delay of single flip flop.
7.	Slow in operation	Fast in operation.

Applications of Counters

It is used in counting machines, which counts things or persons or clocks.

It is used as frequency divisors.

It is used in measuring time durations.

It is used in Print head assembly of dot matrix printer

It is used in Read/Write head assembly of hard disk, DVD etc.

It is used in currency counting machine.

It is used in digital clock machines.

It is used in timers.

Registers

Register is groups of flip-flops used to store binary data temporary. Since, one flip flop can store one bit of binary data, N number of flip-flops are used to store N bit of data. Normally, D flip-flops are used to construct register. These registers are important elements in Arithmetic and Logic circuit and Main memories. The operations in the Register are Read operation and Write operation. The Read operation means data is taken from register or sent from register. The Write operation means data is put into register or sent into register.

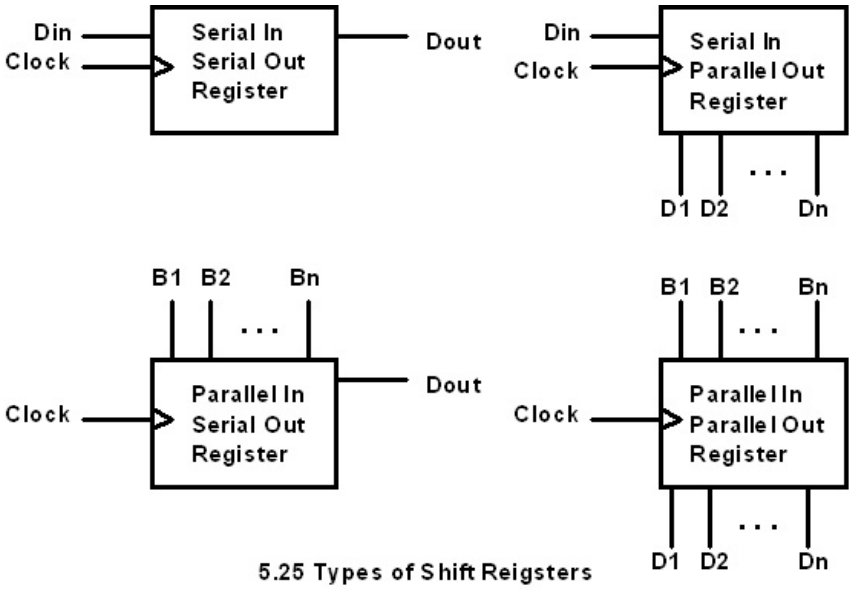
Shift Registers

Shift register is a register which can shift binary bit from one flip flop to another. Shift register are used in building circuits for multiplication, division, addition and subtraction. They are used to transform data from CPU to Input/Output port and vice versa.

Types of Shift Registers

Data can be written/sent and read/received in serial or parallel modes. In serial mode, data is written or read bit by bit i.e. one bit at a time. In parallel mode, data is written or read all bits at a time. The writing of data is called 'in' operation, reading of data is called 'out' operation. Based on in / out operations, serial / parallel modes, the shift registers are divided into four types. They are

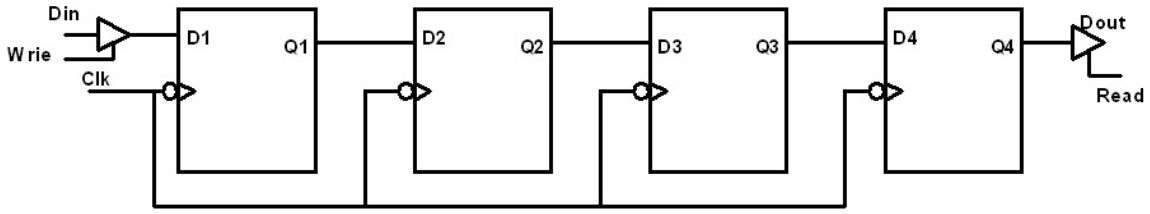
1. Serial-in, Serial-out Shift Register
2. Serial-in, Parallel-out Shift Register
3. Parallel-in, Serial-out Shift Register
4. Parallel-in, Parallel-out Shift Register



5.25 Types of Shift Reigsters

5.3.2 Serial-in, Serial-out Shift Register

This register receives and sends data in serial mode i.e. one bit at a time. The register is made by cascading of D flip-flops. The output of one flip flop is given as input to next flip flop. The circuit arrangement is as follows ;



5.26 Serial-In Serial-Out Shift Register

Serial-in Write Operation :

Initially all the flip-flops are cleared, ie., 0s are stored

1. At the first clock pulse, the LSB (Least Significant Bit) of data is entered into D1 flip flop
2. At the second clock pulse, bit in D1 is shifted to D2, second bit is entered into D1.
3. At the third clock pulse, bit in D2 is shifted to D3, bit in D1 is shifted to D2, third bit is entered into D1.
4. At the fourth clock pulse, bit is D3 is shifted to D4, bit in D2 is shifted to D3, bit D1 is sifted to D2, fourth bit is entered into D1

Example for write Operation :

The write operation is explained using the data 1011. Initially all the flip-flops are cleared, ie.0s are stored

Number of the Clock pulse	D1	D2	D3	D4
	0	0	0	0

1. At the first clock pulse, the LSB (Least Significant Bit) of data '1' is entered into D1 flip flop

Number of the Clock pulse	D1	D2	D3	D4
	0	0	0	0
1	1	0	0	0

2. At the second clock pulse, bit in D1 is shifted to D2, second bit '1' is entered into D1.

Number of the	D1	D2	D3	D4

Clock pulse				
2	1	1	0	0

3. At the third clock pulse, bit in D2 is shifted to D3, bit in D1 is shifted to D2, third bit '0' is entered into D1.

Number of the Clock pulse	D1	D2	D3	D4
3	0	1	1	0

4. At the fourth clock pulse, bit is D3 is shifted to D4, bit in D2 is shifted to D3, bit D1 is sifted to D2, fourth bit '1' is entered into D1

Number of the Clock pulse	D1	D2	D3	D4
4	1	0	1	1

The overall operation is tabulated as follows :

Number of the Clock pulse	D1	D2	D3	D4
0	0	0	0	0
1	1	0	0	0
2	1	1	0	0
3	0	1	1	0
4	1	0	1	1

Serial-out Read Operation :

The data in shift register is read in 4 clock pulses.

1. At the first pulse, bit in D4 is shifted out. The bit in D3 is shifted into D4, bit in D2 is sifted to D3, bit in D1 is shifted to D2. The default bit 0 is entered into D1
2. At the second pulse, bit in D4 is shifted out. The bit D3 is shifted to D4, bit in D2 is shifted into D3, the bit '0' in D1 is shifted to D2, default bit 0 is entered into D1.
3. At the third pulse, bit in D4 is shifted out. The bit in D3 is shifted into D4, 0 in D2 is shifted to D3, D2, default bit 0 is entered into D1.
4. At the fourth pulse, bit in D4 is shifted out. The bit in D3 is shifted into D4, 0 in D2 shifted into D3, 0 in D1 is shifted to D2, default bit 0 is shifted into D1.

Example for Read Operation:

The data in shift register is read in 4 clock pulses. The operation is as follows using the data 1011 in the shift register.

Number of the Clock pulse	D1	D2	D3	D4	Data shifted out
	1	0	1	1	

1. At the first pulse, bit in D4 is shifted out. The bit in D3 is shifted into D4, bit in D2 is sifted to D3, bit in D1 is shifted to D2. The new bit 0 is entered into D1.

Number of the Clock pulse	D1	D2	D3	D4	Data shifted out
1	0	1	0	1	1

2. At the second pulse, bit in D4 is shifted out. The bit D3 is shifted to D4, bit in D2 is shifted into D3, the bit '0' in D1 is shifted to D2, new '0' bit is entered into D1.

Number of the Clock pulse	D1	D2	D3	D4	Data shifted out
2	0	0	1	0	1

3. At the third pulse, bit in D4 is shifted out. The bit in D3 is shifted into D4, 0 in D2 is shifted to D3, D2, new '0' is entered into D1.

Number of the Clock pulse	D1	D2	D3	D4	Data shifted out
3	0	0	0	1	0

4. At the fourth pulse, bit in D4 is shifted out. The bit 0 in D3 is shifted into D4, 0 in D2 shifted into D3, 0 in D1 is shifted to D2, new 0 is shifted into D1.

Number of the Clock pulse	D1	D2	D3	D4	Data shifted out
4	0	0	0	0	1

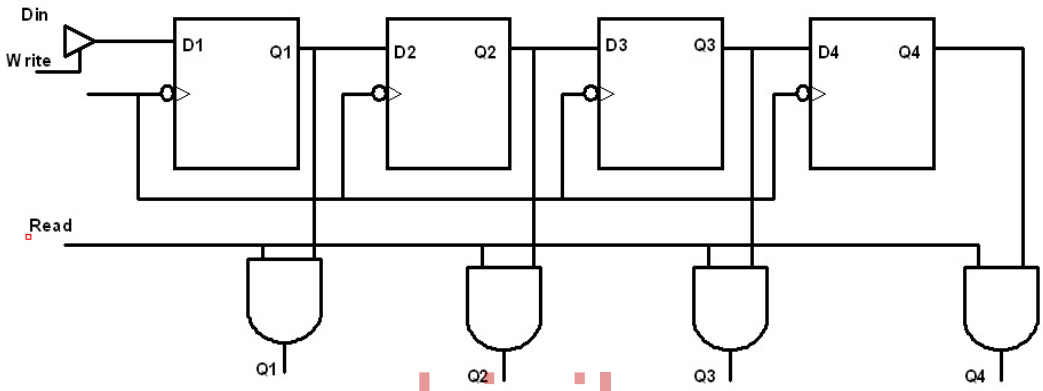
The overall operation is tabulated as follows:

Number of the Clock pulse	D1	D2	D3	D4	Data shifted out
	1	0	1	1	
1	0	1	0	1	1

2	0	0	1	0	1
3	0	0	0	1	0
4	0	0	0	0	1

Serial-in Parallel-out Shift Register

The data is written in serial mode, read in parallel mode. The write operation is same as serial-in, serial-out register. The data is read using the signal Read. This read signal is fed as enable input to four AND gates. The second input is output of all 4 flip-flops as shown in the figure.



5.27 Serial-In Parallel-Out Shift Register

Serial-in Write Operation :

1. At the first clock pulse, the LSB (Least Significant Bit) of data is entered into D1flip flop
2. At the second clock pulse, bit in D1 is shifted to D2, second bit is entered into D1 flip flop
3. At the third clock pulse, bit in D2 is shifted to D3, bit in D1 is shifted to D2, third bit is entered into D1.
4. At the fourth clock pulse, bit in D3 is shifted to D4, bit in D2 is shifted to D3, bit D1 is sifted to D2, fourth bit is entered into D1.

Parallel-out Read operation :

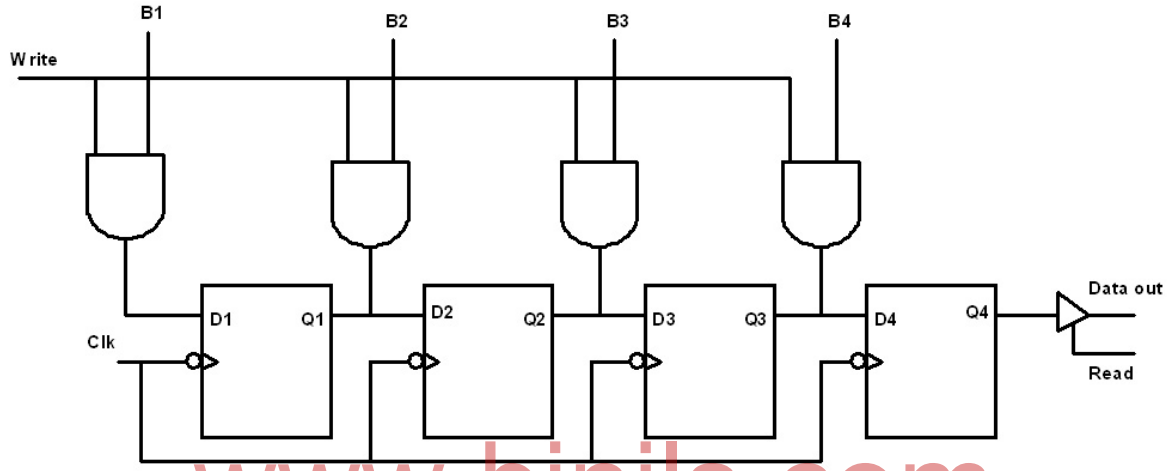
The parallel read operation is done in single clock pulse.

The Read signal is enabled, on the arrival of clock pulse, the bits Q1,Q2,Q3,Q4 are available at the output of the 4 AND gates. For example, if data 1011 is in shift register, the they are read in a single pulse.

Read Signal	Number of Clock pulse	Data			
		Q1	Q2	Q3	Q4
1	1	1	0	1	1

Parallel-in Serial-out Shift Register:

The data is written in parallel mode, read in serial mode in this register. The circuit is as follows :



5.29 Parallel-In Serial-Out Shift Register

Parallel-in Write Operation

The data is written in single clock pulse as follows :

The 4 bits are available at B1, B2, B3, B4 pins. When Write signal is enabled, on the application of clock pulse, the 4 bits are entered into register. The following table stores the data 1011 in the reg*ister*.

Write signal	Number of clock pulse	Data			
		D1	D2	D3	D4
1	1	1	0	1	1

Serial-out Read operation

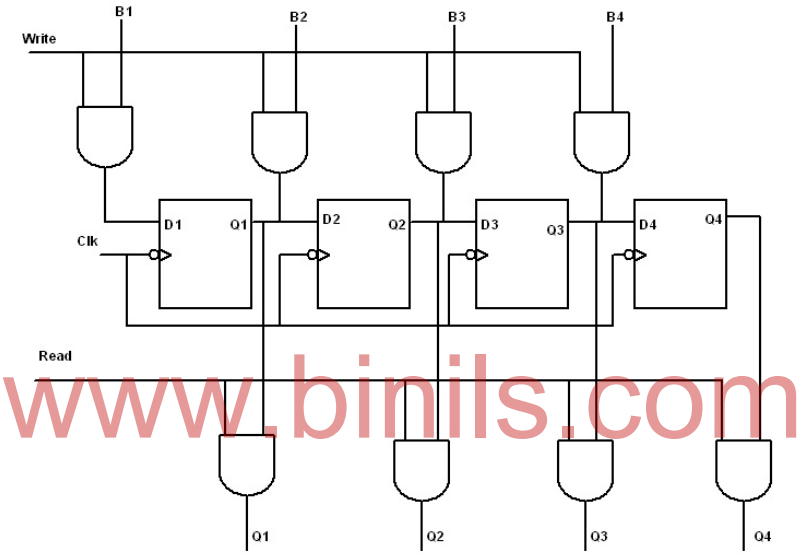
The data is read in 4 clock pulses. The operation is as follows:

1. At the first pulse, bit in D4 is shifted out. The bit in D3 is shifted into D4, bit in D2 is shifted to D3, bit in D1 is shifted to D2. The default bit 0 is entered into D1

2. At the second pulse, bit in D4 is shifted out. The bit D3 is shifted to D4, bit in D2 is shifted into D3, the bit '0' in D1 is shifted to D2, default bit 0 bit is entered into D1.
3. At the third pulse, bit in D4 is shifted out. The bit in D3 is shifted into D4, 0 in D2 is shifted to D3, D2, default bit 0 is entered into D1.
4. At the fourth pulse, bit in D4 is shifted out. The bit 0 in D3 is shifted into D4, 0 in D2 shifted into D3, 0 in D1 is shifted to D2, default bit 0 is shifted into D1.

Parallel-In Parallel-out Shift Register

The write and read operations are done in single clock pulse. Here, both Read and Write signals are used as shown in the figure.



5.30 Parallel-In Parallel-Out Shift Register

Parallel-in Write Operation

The data is written in single clock pulse as follows :

The 4 bits are available at B1, B2, B3, B4 pins. When Write signal is enabled, on the application of clock pulse, the 4 bits are entered into register. The following table stores the data 1011 in the register.

Write signal	Number of clock pulse	Data			
		D1	D2	D3	D4
1	1	1	0	1	1

Parallel-out Read operation :

The parallel read operation is done in single clock pulse.

The Read signal is enabled, on the arrival of clock pulse, the bits Q1,Q2,Q3, Q4 are available at the output of the 4 AND gates. For example, if data 1011 is in shift register, the bits are read in a single pulse.

Read Signal	Number of Clock pulse	Data			
		Q1	Q2	Q3	Q4
1	1	1	0	1	1

Applications of Shift Registers :

1. Shift registers are used for storing binary data
2. Shift registers are used in Arithmetic circuits for doing addition, subtraction, multiplication, division operations.
3. Shift registers are used in Parallel to Serial data transmission and vice versa.
4. Shift registers are used in industrial automation
5. Shift registers are used in modems
6. It is used in producing delay in the circuit.

Summary

- ✓ Digital circuits are of two types : combinational and sequential circuits
- ✓ Flip flop is a single bit storage element and is one type of sequential circuit.
- ✓ Four types of flip-flops are SR, D, T and JK flip flop.
- ✓ Four states of flip-flops are Set, Reset, No change and Toggle.
- ✓ The forbidden state in SR flip flop is S = 1 and R = 1. Forbidden means not used.
- ✓ Triggering means activating the circuit with clock signal.
- ✓ Two types of Triggering are Level and Edge triggering.
- ✓ Level triggering are of two types : High and Low level triggering.
- ✓ Edge triggering are of two types : Positive and Negative edge triggering.
- ✓ D flipflop is modified SR flip flop. The S and R inputs are combined using a NOT gate into single input D.
- ✓ D flip flop is the data flip flop with two states : Set and Reset.
- ✓ JK flip flop has one Toggle state when J = 1 and K = 1.
- ✓ T flip flop is modified version of JK Flip flop. The J and K inputs are combined into single input T.
- ✓ T flip flop has two states : Set and Toggle.
- ✓ Propagation delay is the reason for the race condition.
- ✓ JK or T flip flop is the building block of counter.
- ✓ Counter is the counting circuit which counts from 0 to 2^N-1

- ✓ Two types of counters are parallel and serial.
- ✓ Asynchronous counter or serial counter is triggered in cascaded manner.
- ✓ MOD N counter counts from 0 to N-1 and resets at Nth count.
- ✓ Synchronous counter or parallel counter needs additional circuit for counting.
- ✓ Synchronous counter is triggered simultaneously.
- ✓ Counters are used in counting machines, printers and plotters.
- ✓ Register is a memory element
- ✓ Shift register are one type of registers.
- ✓ D or SR flip-flops are building blocks of Shift register.
- ✓ Four types of shift registers are 1. Serial-in, Serial-out 2. Serial-in, Parallel-out 3. Parallel-in, Serial-out 4. Parallel-in, Parallel – out
- ✓ Two methods of write operations are serial and parallel
- ✓ Two methods of read operations are serial and parallel
- ✓ In serial transmission, data is sent one bit at a time.
- ✓ In parallel transmission, data is sent all bits at a time.
- ✓ Shift registers are used in arithmetic circuits
- ✓ Shift register are Serial and Parallel modes of data transmission

REVIEW QUESTIONS :

Part A

12. Name the different types of digital circuits.
13. Define : Combinational circuit.
14. Define : Sequential circuit.
15. Differentiate between combinational and digital circuits.
16. What is a flip flop ?
17. Write the types of Flip-flops
18. State the four conditions of flip flop.
19. What do you mean by triggering ?
20. Define : clock signals
21. What are the types of triggering ?
22. Write the definition of Level triggering.
23. Write the definition of Edge triggering.

24. What is the forbidden state in SR flip flop ?

25. What is D flip flop ?

26. What is toggling ?

27. What are the applications of flip flop ?

28. What is a race condition ?

29. What is the JKMS ?

30. What are PRESET and CLEAR inputs ?

31. Define : Counter.

32. What are the applications of counter ?

33. What are the types of counter ?

34. What is a MOD N counter ?

35. What is the BCD counter ?

36. What is the difference between Parallel and Serial counters ?

37. What is a Register ?

38. What is the use of Shift Register ?

39. What are the types of Shift Register ?

40. What is a Read operation ?

41. What is a Write operation ?

42. What is the serial read operation ?

43. What is the serial write operation ?

44. What is the parallel read operation ?

45. What is the parallel write operation ?

Part B

1. Write on four states of flip-flops.
2. Write notes on Level Triggering.
3. What is edge triggering ? Write on it.
4. Write on Race condition and need for Master Slave flip flop.
5. Write on Counter.
6. How MOD N counter is working ?

7. Draw the circuit for MOD 5 counter
8. What are the differences between parallel and serial counters ?
9. What are the applications of counters ?
10. Write on types of shift registers.
11. What are the applications of Shift registers ?

Part C

12. How SR flip flop works ? Explain.
13. Explain the working of D flip flop
14. Describe the working of T flip flop.
15. How JK flip flop works ?
16. Write on JKMS flip flop.
17. How a 4 bit asynchronous counter is working ?
18. Write on MOD 5 counter.
19. What is decade counter ? Write on it.
20. Explain the working of synchronous counter.
21. How serial-in, serial-out and serial-in, Parallel-out shift registers are working ?
22. Explain the working of Parallel-in, Serial-out and Parallel-in, Parallel-out shift registers.