Reg. No. :

Question Paper Code : X86436

M.E./M.Tech. DEGREE EXAMINATIONS, APRIL/MAY 2021
Second Semester
Applied Electronics
AP5291 – HARDWARE-SOFTWARE CO-DESIGN
(Regulations – 2017)

Time : Three Hours | Maximum : 100 Marks

Answer ALL questions

PART – A **(10×2=20 Marks)**

1. Sketch the design flow of hardware/software co-design approach.
2. Compare the co-design approaches in terms of specification and implementation power.
3. Formulate hardware/software partitioning problem.
4. Identify the optimal parameters involved in hardware/software cost estimation.
5. List the steps involved in the co-synthesis flow for reactive real-time systems.
6. For the sample C program given below, generate the control flow graph.
   if (c > d)
   x=e ;
   else y =f ;
7. Differentiate simulation and emulation methods.
8. Sketch the microcontroller based FSM implementation.
9. Mention the models for interfacing the concurrent components of a design.
10. Sketch the generic flow for co-design of system level heterogeneous specification.

PART – B **(5×13=65 Marks)**

11. a) Explain the single processor and multi-processor architectures supported in co-design tools.

(OR)

b) Discuss in detail about the various models of computation in hardware/software co-design.

12. a) With suitable pseudo codes explain how hardware/software partitioning can be done using heuristic scheduling algorithms.

(OR)

b) Describe the Hardware Software Partitioning problem as a Constraint Satisfaction Problem (CSP), and present a Genetic algorithm based approach to solve the CSP in order to obtain the partitioning solution.

13. a) Develop an Integer Linear Programming (ILP) formulation for the single-rate co-synthesis problem and use general ILP solvers to solve the resulting system of equations.

(OR)

b) Deduce an architectural co-synthesis algorithm for distributed, embedded computing system.

14. a) Explain in detail about source-level emulation with necessary diagrams.

(OR)

b) Explore the target architectures for various signal processing applications and explain them.

15. a) Illustrate the significance of concurrency based computation in an embedded system. Also specify the alternative ways in which concurrent computations can be coordinated.

(OR)

b) Compare and contrast the various specification languages used in computing systems.

PART – C **(1×15=15 Marks)**

16. a) Deduce the input-based and state-based FSM model of an elevator controller in a building with three floors. In this model, the set of inputs I = {r1, r2, r3} represents the floor requested. For example, r2 means that floor 2 is requested. The set of outputs 0 = {d2, d1, n, u1, u2} represents the direction and number of floors the elevator should go. For example, d2 means that the elevator should go down 2 floors, u2 means that the elevator should go up 2 floors, and n means that the elevator should stay idle. The set of states represents the floors.

(OR)

b) Illustrate the various approaches to increase computation performance without compromising short latency times and control concurrency. Also identify suitable architectures to implement high performance controller and explain them.