Reg. No. :

Question Paper Code : X86435

M.E./M.Tech. DEGREE EXAMINATIONS, APRIL/MAY 2021

Second Semester

Applied Electronics

AP5252 – ASIC AND FPGA DESIGN

(Common to Electronics and Communication Engineering/Electronics and Communication Engineering (Industry Integrated))

(Regulations 2017)

Time : Three Hours | Maximum : 100 Marks

Answer ALL questions.

PART – A **(10×2=20 Marks)**

1. What is the advantage of λ based design rule ?
2. What is the difference between EEPROM and UVPROM technology ?
3. What is meant by Timing Driven Placement and Timing Driven Routing ?
4. List the different design checks used in ASIC.
5. Define MRST and EDIF.
6. What is meant by Built-in-Self-Test (BIST) ?
7. Compare Xilinx LCA, Actel Act and Altera MAX architecture.
8. What is the difference between Act2 and Act3 logic modules ?
9. List the Signal Integrity Effects in SOC Design.
10. Write SOC architecture typical design steps.

PART – B **(5×13=65 Marks)**

11. a) Explain the performance and characteristics for the following design styles.
    i) Standard cells. **(7)**
    ii) Cell based ASIC. **(6)**

(OR)

b) i) Explain in details how an EPROM can be used to realize a sequential circuit. **(7)**
    ii) Why SRAM based FPGAs are popular when compared to other types ? Explain. **(6)**

12. a) i) What are the goals and objectives of system partitioning ? Explain any one algorithm for partitioning. **(7)**

ii) Distinguish between global routing and detailed routing. **(6)**

(OR)

b) i) Explain SDF (Standard Delay Format) back annotation/SPEF (Standard Parasitic Exchange Format) timing correlation flow. **(7)**

ii) How is scan DEF(Design Exchange Format) generated ? **(6)**

13. a) i) Explain about Boundary Scan Architecture design and its Routing. **(7)**

ii) Explain in detail about design flow of the Half Gate ASIC. **(6)**

(OR)

b) Write about :

i) Verilog and logic synthesis. **(5)**

ii) VHDL and logic synthesis. **(4)**

iii) Scan design testing. **(4)**

14. a) i) How FPGA placement and routing is different from ASIC placement and routing process. **(7)**

ii) Why SRAM based FPGAs are popular when compared to other types ? Explain. **(6)**

(OR)

b) i) Design 3-bit shift register and implement using Xilinx FPGA. **(7)**

ii) Explain the basic logic programming elements of the FPGA with a suitable example. **(6)**

15. a) i) Explain in detail about the types Configurable SOC Platform. **(7)**

ii) Write a complete system for capturing, improving and storing digital images. **(6)**

(OR)

b) i) Explain briefly how the hardware/software co-simulation and co-synthesis issued are addressed. **(7)**

ii) Write a note on SOC design and verification techniques. **(6)**

PART – C **(1×15=15 Marks)**

16. a) Construct the conceptual architecture of Embedded Core-Based SOC, and analyze the challenges of SOC Testing and Verification.

(OR)

b) Explain the ASIC design flow with a neat diagram and write the difference between custom IC and standard IC ?

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