Reg. No. :

Question Paper Code : X86425

M.E./M.Tech. DEGREE EXAMINATIONS, APRIL/MAY 2021

Second Semester

Applied Electronics

AP5003 – VLSI DESIGN TECHNIQUES

(Regulations 2017)

Time : Three Hours | Maximum : 100 Marks

Answer ALL questions.

PART – A **(10×2=20 Marks)**

1. Draw the electric model for CMOS inverter.
2. What do you meant by dynamic power dissipation and write the express for it.
3. Draw the stick diagram for 2input NAND Gate.
4. Write down the advantage of dynamic CMOS logic gates.
5. Make a difference between static and dynamic latches.
6. List out the merits of pipelining techniques which is used in VLSI Circuits.
7. Draw the general structure of ripple carry adder circuits.
8. Write down the classification of memories based on their architecture.
9. Give the relationship between resistance and propagation delay of the CMOS Logic Circuits.
10. Write short notes on self-timed circuit.

PART – B **(5×13=65 Marks)**

11. a) Write notes on :

    i) Process Variations. **(7)**

    ii) MOSFETs as switches. **(6)**

    (OR)

    b) Illustrate the concept of Complementary MOS inverter DC characteristics with neat diagram.

12. a) Draw the stick diagram and a mask layout for an8 : 1nMOS inverter circuit. Both the Input and Output points should be on the polysilicon layer.

(OR)

b) Detail description about the low power design techniques in CMOS design with neat diagram.

13. a) Detail description about Dynamic edge triggered registers with required diagram.

(OR)

b) Explain about the architecture of 4×4 MOS NAND operation.

14. a) Illustrate the circuit design consideration for complementary static CMOS implementation of full adder.

(OR)

b) Give the details about the 4×4 bit array multiplier for unsigned numbers.

15. a) Derive the expression for resistance and capacitance for CMOS interconnect model.

(OR)

b) Detail description about timing classification of digital systems with neat diagram.

PART – C **(1×15=15 Marks)**

16. a) Construct a Clocked CMOS circuit and dynamic logic for the function F=Not{a.b.c + a.(d+e)}.

(OR)

b) Illustrate about the various Clocking styles used in CMOS circuits.

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