Reg. No. | | | | | | | | | | | | | | |

Question Paper Code : X85081

M.E./M.Tech. DEGREE EXAMINATIONS – NOV / DEC 2020

First Semester

VLSI Design and Embedded Systems

AP5151 Advanced Digital System Design

(Common to: Applied Electronics/ M.E. VLSI Design)

(Regulations 2017)

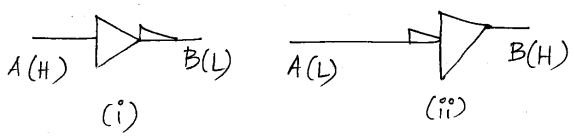
Time: 3 Hours | Answer ALL Questions | Max. Marks 100

PART- A (10 x 2 = 20 Marks)

1. Draw the state diagram for the following state table :

	x=0	x=1	0	1
S_0	S_1	S_0	0	0
S_1	S_0	S_2	1	0
S_2	S_2	S_2	1	1
S_3	S_0	S_1	0	1

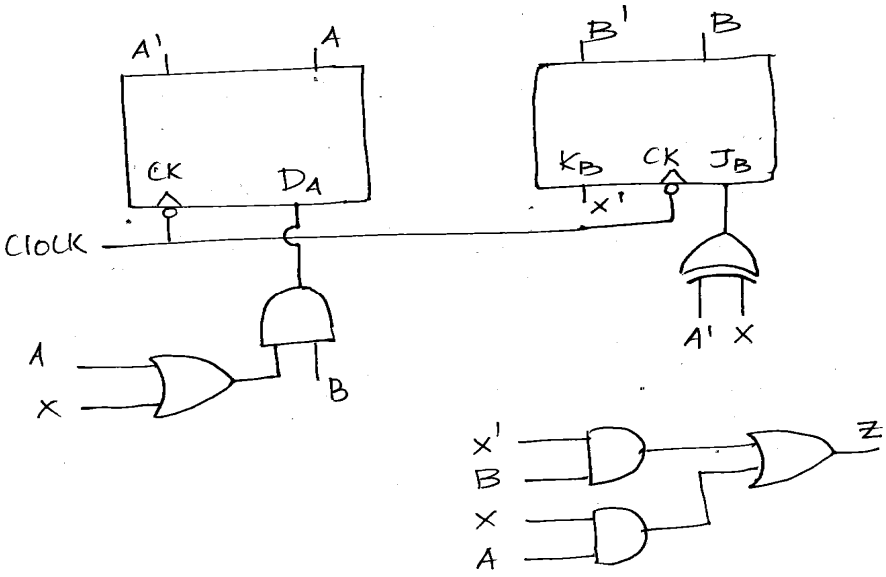
2. What is an iterative network?
3. Name the two types of Asynchronous sequential circuit.
4. Give the truth tables for Inverter with positive logic for the input and negative logic for the output



5. Define S-a-0 and S-a-1 faults.
6. Define Fault Equivalence and Fault Dominance.
7. Draw the structure of an EEPROM transistor used in FPGA programming technologies.
8. What is a dedicated carry logic in Xilinx 4000 series FPGA? Give its significance.
9. What are functions and tasks in Verilog?
10. Write the Verilog code for an half adder using data flow modeling?

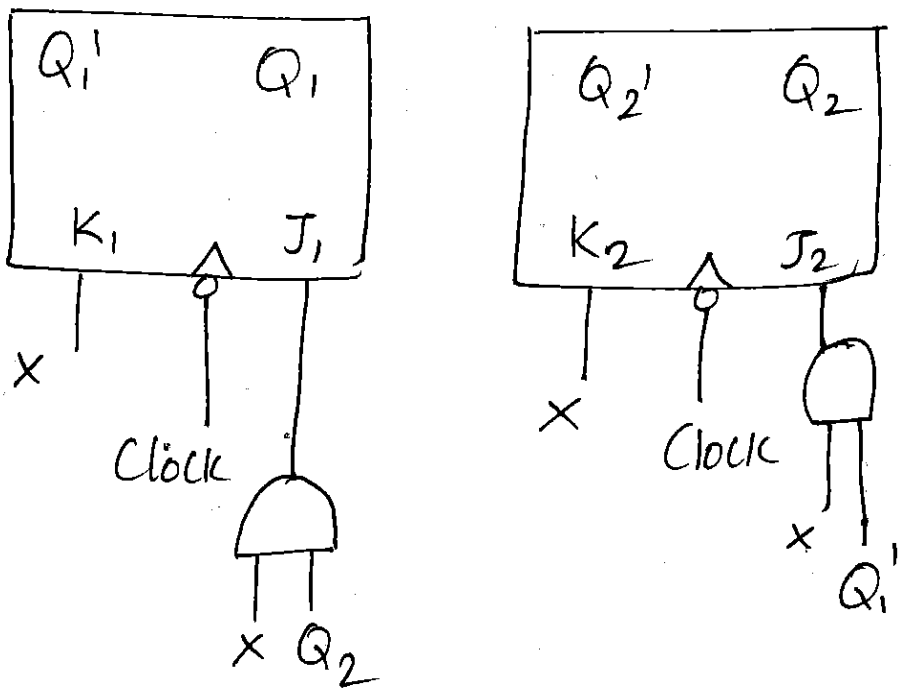
PART- B (5 x 13 = 65 Marks)

11. a) Analyze the following sequential network using a state table and timing chart. **(13)**



OR

b) (i) Construct a timing chart for the network for an input sequence X=10011. Indicate at what timer Z has the correct value and specify the correct output sequence.(Assume that X changes midway between clock pulses) Initially, $Q_1=Q_2=0$ **(7)**



(ii) With an example, explain the ASM chart. **(6)**

12. a) (i) Explain cycles and races in asynchronous sequential circuits with suitable examples. **(7)**

(ii) Reduce the following primitive flow table

	$X_1 X_2$				
	00	01	11	10	Z_1 Z_2
1	(1)	7	-	4	1 1
2	(2)	5	-	4	0 1
3	-	7	(3)	11	1 0
4	2	-	3	(4)	0 0
5	6	(5)	9	-	1 1
6	(6)	7	-	11	0 1
7	1	(7)	14	-	1 0
8	(8)	12	-	4	0 1
9	-	7	(9)	13	0 1
10	-	7	(10)	4	1 0
11	8	-	10	(11)	0 0
12	6	(12)	9	-	1 1
13	8	-	14	(13)	1 1
14	-	12	(14)	11	0 0

(6)

OR

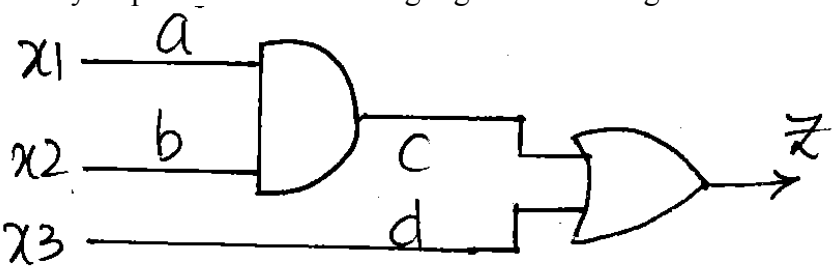
b) (i) Design a synchronizer circuit to synchronize the input changes with clock in a sequential network. **(5)**

(ii) Explain static and dynamic hazards with suitable example. **(8)**

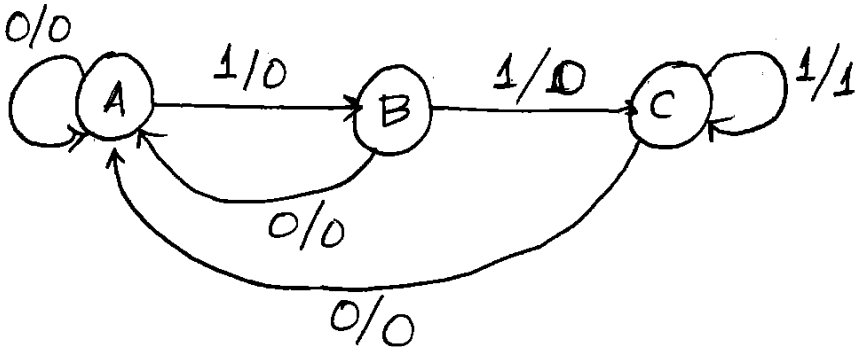
13. a) Discuss the COMPACT algorithm with a suitable example to derive the foldable compatibility matrix to fold a given PLA. **(13)**

OR

b) (i) Explain design for testability (DFT) scheme. **(5)**
(ii) Deduce the set of all possible single stuck –at-faults and the fault –free and faulty response of the following logic circuit using Fault table method: **(8)**



14. a) (i) With suitable examples, explain the basic difference between PLA and PAL. **(5)**
(ii) Design the following circuit and realize it with a sequential PLA. **(8)**



OR

b) Discuss the configurable logic block architecture and Input-Output block of Xilinx 4000 series FPGA. **(13)**

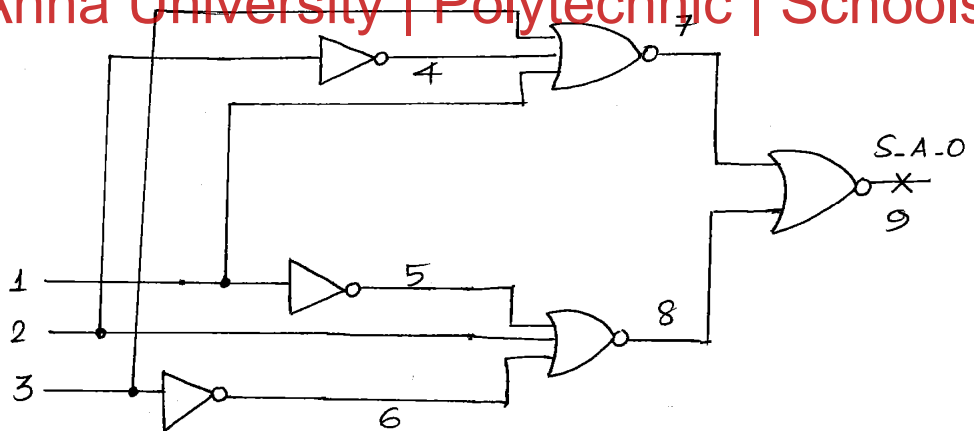
15. a) Design a full adder and write the Verilog code using
(i) Structural modeling **(5)**
(ii) Behavioral modeling **(4)**
Also write the test bench. **(4)**

OR

b) (i) Write the Verilog code for a D flip flop using behavioral modeling. **(5)**
(ii) Design Moore based serial adder and Mealy based Serial adder. Write the Verilog code to realize it using structural modeling. **(8)**

PART- C (1 x 15 = 15 Marks)

16. a) Derive the test vector to detect the Stuck- at-o fault in line 9 of the following logic circuit using D-Algorithm: **(13)**

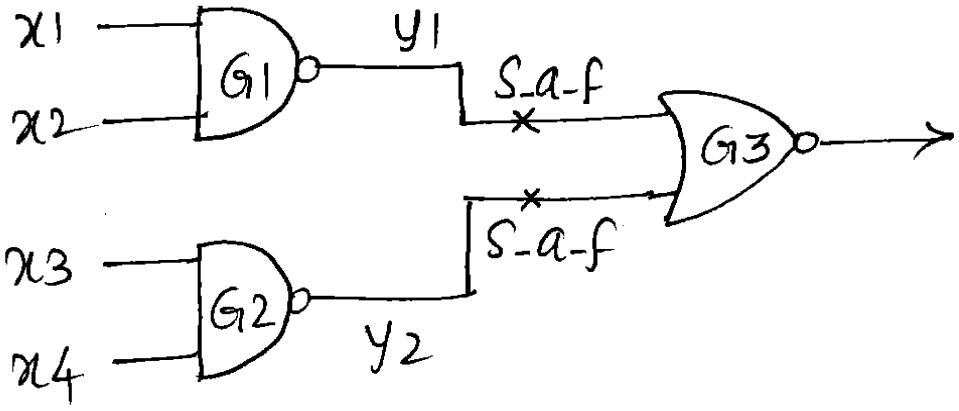


OR

b) Derive the test vector to detect the single Stuck- at-fault using

(i) Path Sensitization method **(7)**

(ii) Boolean difference method **(8)**



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