## Question Paper Code : X10368

B.E./B.Tech. DEGREE EXAMINATIONS, NOVEMBER/DECEMBER 2020

Fifth Semester
Electronics and Communication Engineering
EC 8553 - DISCRETE-TIME SIGNAL PROCESSING
(Common to Biomedical Engineering/Electronic Telecommunication Engineering/Medical Electronics)
(Regulations 2017)
Time : Three Hours
Maximum : 100 Marks

Answer ALL questions
PART - A
(10×2=20 Marks)

1. State and prove the circular time shift property of DFT.
2. Justify the statement, "with zero padding, Discrete Fourier Transform can be used to perform linear filtering".
3. Using Bilinear transform obtain $\mathrm{H}(\mathrm{z})$ if $\mathrm{H}(\mathrm{s})=\frac{1}{(\mathrm{~s}+1)^{2}}$ and the sampling period
$\mathrm{T}=0.1 \mathrm{~s}$.
4. Draw the frequency response of a digital Butterworth low pass filter with a cut-off frequency of $2 \mathrm{rad} / \mathrm{sec}$.
5. What is the Gibb's phenomenon ? Show how it can be reduced by using smooth windowing function in the design of FIR filters?
6. Write the Hamming Window function and outline its characteristic features.
7. Express -0.125 in floating point binary representation.
8. Outline the characteristics of error in product quantization.
9. List the merits of instruction pipelining.
10. Compare fixed point and floating point DSP processors.
PART - B
11. a) i) Obtain the response of a digital filter having the impulse response $h(n)=\{1,2,4\}$ to the input sequence $\mathrm{x}(\mathrm{n})=\{1,2\}$.
ii) Compute the DFT of $\mathrm{x}(\mathrm{n})=\cos (\mathrm{n} \pi / 4) ; 0 \leq \mathrm{n} \leq 7$ using DIT-FFT algorithm.
(OR)

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b) i) Obtain the output $y(n)$ of a filter whose impulse response is $h(n)=\{1,1,1\}$ and input signal $x(n)=\{3,-1,0,1,3,2,0,1,2,1\}$ using overlap-save method.
ii) Given $\mathrm{X}(\mathrm{k})=\{36,-4+\mathrm{j} 9.656,-4+\mathrm{j} 4,-4+\mathrm{j} 1.656,-4,-4-\mathrm{j} 1.656,-4-\mathrm{j} 4$, $-4-\mathrm{j} 9.656\}$, find $\mathrm{x}(\mathrm{n})$, using DIF-FFT algorithm.
12. a) i) Determine the transfer function of the second order normalized analog Chebyshev low pass filter.
ii) Determine the direct form I and II realization for a third-order IIR transfer function.

$$
\begin{equation*}
\mathrm{H}(\mathrm{z})=\frac{\left(0.28 \mathrm{z}^{2}+0.3 \mathrm{z}+0.04\right)}{\left(0.5 \mathrm{z}^{3}+0.3 \mathrm{z}^{2}+0.7 \mathrm{z}-0.2\right)} \tag{6}
\end{equation*}
$$

(OR)
b) Determine $\mathrm{H}(\mathrm{z})$ for a Butterworth filter satisfying the following constraints.

$$
\begin{array}{rl}
\sqrt{0.5} \leq\left|\mathrm{H}\left(\mathrm{e}^{\mathrm{j} \omega}\right)\right| \leq 1 & 0 \leq \omega \leq \pi / 2  \tag{13}\\
& \left|\mathrm{H}\left(\mathrm{e}^{\mathrm{j} \omega}\right)\right| \leq 0.2
\end{array} \quad 0.75 \pi \leq \omega \leq \pi ~ \$ ~ l
$$

With $\mathrm{T}=1 \mathrm{~s}$. Apply impulse invariant transformation.
13. a) The desired frequency response of a low pass filter is
$\mathrm{H}_{\mathrm{d}}\left(\mathrm{e}^{\mathrm{j} \omega}\right)=\left\{\begin{array}{l}1,-\pi / 2 \leq \omega \leq \pi / 2 \\ 0, \pi / 2 \leq \omega \leq \pi\end{array}\right.$
Determine $h_{d}(n)$. Also determine $h(n)$ using the symmetric rectangular window, with window length $=7$.
(OR)
b) i) Use the Fourier series method to design a low pass digital filter to approximate the ideal specifications given by
$H\left(e^{j \omega}\right)=\left\{\begin{array}{ll}1, & \text { for }|f| \leq f_{p} \\ 0, & f_{p} \leq|f| \leq F / 2\end{array}\right.$, where $f_{p}$ is the passband frequency and $F$ is the sampling frequency.
ii) Obtain FIR linear phase and cascade realizations of the system function.

$$
\mathrm{H}(\mathrm{z})=\left(1+\frac{1}{2} \mathrm{z}^{-1}+\mathrm{z}^{-2}\right)\left(1+\frac{1}{4} \mathrm{z}^{-1}+\mathrm{z}^{-2}\right)
$$

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14. a) Discuss the effects of finite word length in the implementation of the FFT algorithms using fixed point arithmetic.
(OR)
b) Explain the effects of coefficient quantization in Direct Form Realization of IIR filter.
15. a) i) Illustrate the addressing modes of DSP processors.
ii) Sketch the structure of the MAC unit and DSP processor and explain its functions.
(OR)
b) i) Explain the architecture of fixed point and floating point DSP processors.
ii) With suitable diagrams show how to implement FIR filter in DSP processor.
PART - C
16. a) The first order filter shown in Fig. 1 below is implemented in four-bit (including sign bit) fixed point two's complement fractional arithmetic. Products are rounded to four-bit representation using the input $x(n)=0.10 \delta(n)$. Determine
i) the first five outputs if $\alpha=0.5$. Does the filter go into a limit cycle?
ii) the first five outputs if $\alpha=0.75$. Does the filter go into a limit cycle ?


## Fig. 1

(OR)
b) i) Express the magnitude response of an FIR filter of length 11 exhibiting the linear phase property.
ii) A band reject FIR filter of length seven is required. It is to have lower and upper cut-off frequencies as 3 KHz and 6 KHz respectively. The sampling frequency is 18 KHz . Determine the filter co-efficients using Hanning window. Draw the structure of the filter.

