Reg. No.

Question Paper Code : X10348

B.E./B.Tech. DEGREE EXAMINATIONS NOVEMBER/ DECEMBER 2020 AND APRIL / MAY 2021

Sixth /Seventh Semester

Electronics and Communication Engineering

EC8095- VLSI DESIGN

(Common to: Electronics and Telecommunication Engineering/ Electrical and Electronics Engineering/ Electronics and Instrumentation Engineering)

(Regulations 2017)

Time: 3 Hours   Answer ALL Questions   Max. Marks 100

PART- A (10 x 2 = 20 Marks)

1. Sketch a complementary CMOS gate computing $Y = (AB + BC)'$.

2. What is body effect?

3. What is the logical effort for two input NOR gate? (Assume the required values)

4. What is the use of transmission gates?

5. List the timing classification of Digital system.

6. Differentiate latches and flip-flops.

7. Draw the dot diagram for Wallace tree multiplier.

8. List the categories of memory arrays.

9. What is the significance of field programmable gate arrays?

10. Identify the ways to optimize the manufacturability, to increase yield.

PART- B (5 x 13 = 65 Marks)

11. a) i) Differentiate static and dynamic latches and registers.   **6**
    ii) Obtain the first-order model relating the current and voltage for an nMOS   **7**
    transistor in three regions of MOS operation.

    OR

    b) i) Explain the DC transfer characteristics of CMOS inverter.   **6**
    ii) Estimate the delay of CMOS logic gates as the RC product of the effective   **7**
    driver resistance and the load capacitance.

12. a) Sketch a combinational function $Y = (A(B+C+D)+ E.F.G)'$ using
    i.   Pseudo-nMOS logic   **4**
    ii.   Domino logic   **4**
    iii. Cascode voltage switch logic.   **5**

    OR

    b) Explain the pass transistor logic and show how complementary pass   **13**
    transistor logic and double pass transistor logic are applied for 2: 1
    multiplexer.

13. a) i. Illustrate the circuit designs for basic latches, then build the flip-flops and pulsed latches. **7**

ii. Design the pulse registers suitable for sequential CMOS circuits. **6**

OR

b) i) Describe the concept of pipelining in sequential circuits with a suitable example. **7**

ii) Sketch and explain the Monostable sequential circuits based on CMOS logic. **6**

14. a) i) Explain the carry-propagate adder and show how the generation and propagation signals are framed. **6**

ii) List the several commonly used shifters. Design the shifter that can perform all the commonly used shifters. **7**

OR

b) Illustrate the building blocks of Memory architectures and memory peripheral circuitry adapted to operate for non-volatile memory. **13**

15. a) i) Show how routing is performed in FPGA interconnect. **6**

ii) Illustrate the basic building block architectures of FPGA. **7**

OR

b) Explain the three main approaches commonly used for design for testability (DFT). **13**

PART- C (1 x 15 = 15 Marks)

16. a) i) Differentiate static and dynamic power in CMOS circuits. **7**

ii) Sketch the 4:1 multiplexer using transmission gates. **8**

OR

b) Generate the partial products using radix-4 booth encoded multiplier to compute 01110_2 x 01101_2. For the same multiplier apply radix-8 booth encoding and justify the advantages between radix-4 and radix-8 booth multiplier. **15**