Bus Impedance matrix building algorithm

Bus impedance matrix Zbus of a power network can be obtained byinverting the bus admittance matrix Ybus , which is easy to construct. However, when the order of matrix is large, direct inversion requires more core storage and enormous computer time. Therefore inversion of Ybus is prohibited for large size network. Bus impedance matrix can be constructed by adding the network elements one after the other. Using impedance parameters, performance equations in bus frame of reference can be written as

$$E_{bus} = Z_{bus} I_{bus}$$

In the expanded form the above becomes

$$\begin{bmatrix} E_1 \\ E_2 \\ \vdots \\ E_N \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{12} & \cdots & Z_{1N} \\ Z_{21} & Z_{22} & \cdots & Z_{2N} \\ \vdots & \vdots & \vdots & \vdots \\ Z_{N1} & Z_{N2} & \cdots & Z_{NN} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \\ \vdots \\ I_N \end{bmatrix}$$

From this we can write

$$Ep = Z_{p1} I_1 + Z_{p2} I_2 + ... + ZpqIq + ... + ZpN$$

From the above, it can be noted that with Iq = 1 p.u. other bus currents set to

zero, Ep = Zpq . Thus Zpq can be obtained by measuring Ep when 1 p.u. current is injected at bus q and leaving the other bus currents as zero. In fact p and q can be varied from 1 to N.While making measurements all the buses except one, are opencircuited. Hence, the bus impedance parameters are called open circuitimpedances. The diagonal elements in Zbus are known as driving pointimpedances, while the off-diagonal elements are called transferimpedances.

Symmetrical fault analysis through bus impedance matrix. Once the bus impedance matrix is constructed, symmetrical fault analysiscan be carried out with a very few calculations. Bus voltages andcurrents in various elements can be computed quickly. When faults areto be simulated at different buses, this method

is proved to be good.Symmetrical short circuit analysis essentially consists of determining thesteady state solution of linear network with balanced sources.Since the short circuit currents are much larger compared to prefault currentsthe following assumptions are made while conducting short circuit study.

1. all the shunt parameters like loads, line charging admittances

   etc. are neglected.

2. all the transformer taps are at nominal position.

3. prior to the fault, all the generators are assumed to operate at

   rated voltage of 1.0 p.u. with their emf's in phase. With these assumptions, in the prefault condition, there will not be anycurrent flow in the network and all the bus voltages will be equal to1.0 p.u.

The linear network that has to be solved comprises of

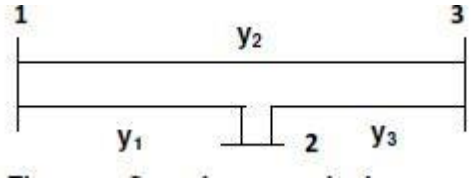
i) Transmission network

ii) ii) Generation system and iii) Fault

By properly combining the representations of the above three components,

we can solve the short circuit problem.

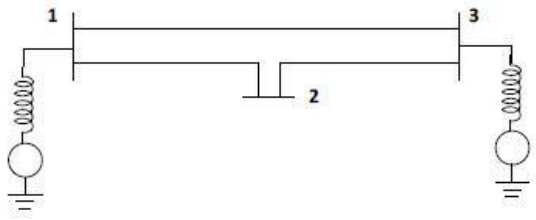
Consider the transmission network shown in Fig



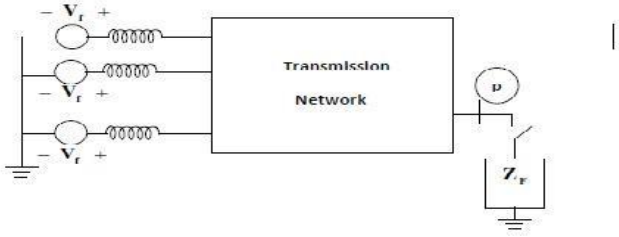
Taking the ground as the reference bus, the bus admittance matrix is obtained as

$$Y_{bus} = \begin{array}{c} \\ 1 \\ 2 \\ 3 \end{array} \begin{array}{c} \begin{array}{ccc} 1 & 2 & 3 \end{array} \\ \begin{bmatrix} y_1+y_2 & -y_1 & -y_2 \\ -y_1 & y_1+y_3 & -y_3 \\ -y_2 & -y_3 & y_2+y_3 \end{bmatrix} \end{array}$$

If we add all the columns (or rows) we get a column (or row) of allzero elements. Hence this Ybus matrix is singular and hence correspondingZbus matrix of this transmission network does not exist. Thus, when all the shunt parameters are neglected, Zbus matrix will not exist for thetransmission network. However, connection to ground is established at the generator buses, representing the generator as a constant voltage source behind appropriatereactance as shown in Fig.



If the generator reactance are included with the transmission network, Zbus matrix of the combined network can be obtained. As stated earlier, there is no current flow in the network in the pre-fault condition and all the bus voltages will be 1.0 p.u. Consider the network shown in Fig. Symmetrical fault occurring at bus 2can be simulated by closing the switch shown in Fig.HereZf is the fault impedance



In the faulted system there are two types of sources:

1. Current injection at the faulted bus

2. Generated voltage sources.

The bus voltages in the faulted system can be obtained using Superposition

Theorem.

Bus voltages due to current injection:

Make all the generator voltages to zero. Then we have Generator-Transmission system without voltage sources. Such network has transmission parameters and generator reactances between generator buses and the ground. LetZbus be the bus impedance matrix of such Generator-Transmission network. Then the bus voltages due to the current injection will be given by

$$Vbus = Z_{bus} I_{bus} (F)$$

where I_{bus} (F) is the bus current vector having only one non-zero element.

Thus when the fault is at the p^{th} bus

$$I_{bus\,(F)} = \begin{bmatrix} 0 \\ \vdots \\ 0 \\ I_{p\,(F)} \\ 0 \\ \vdots \\ 0 \end{bmatrix}$$

Here Ip (F) is the faulted bus current

$$V_{bus} = \begin{bmatrix} Z_{11} & Z_{12} & \cdots & Z_{1p} & \cdots & Z_{1N} \\ Z_{21} & Z_{22} & \cdots & Z_{2p} & \cdots & Z_{2N} \\ \vdots & \vdots & & \vdots & & \vdots \\ Z_{p1} & Z_{p2} & \cdots & Z_{pp} & \cdots & Z_{pN} \\ \vdots & \vdots & & \vdots & & \vdots \\ Z_{N1} & Z_{N2} & \cdots & Z_{Np} & \cdots & Z_{NN} \end{bmatrix} \begin{bmatrix} 0 \\ 0 \\ \vdots \\ I_{p\,(F)} \\ \vdots \\ 0 \end{bmatrix} = \begin{bmatrix} Z_{1p} \\ Z_{2p} \\ \vdots \\ Z_{pp} \\ \vdots \\ Z_{Np} \end{bmatrix} I_{p\,(F)}$$

Bus voltages due to generator voltages

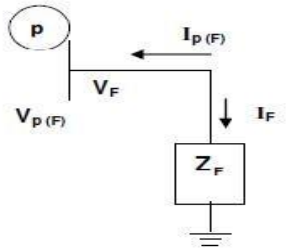
Make the fault current to be zero. Since there is no shunt element, there will be no current flow and all the bus voltages are equal to V0 , the pre-fault voltage which will be normally equal to 1.0 p.u. Thus, bus voltages due to generator voltages will be

$$V_{bus} = \begin{bmatrix} 1 \\ 1 \\ \vdots \\ 1 \\ \vdots \\ 1 \end{bmatrix} V_0$$

Thus for the faulted system, wherein both the current injection and generator sources are simultaneously present, the bus voltages can be obtained by adding the voltages. Therefore, for the faulted system the bus voltages are

$$V_{bus\,(F)} = \begin{bmatrix} V_{1(F)} \\ V_{2(F)} \\ \vdots \\ V_{p(F)} \\ \vdots \\ V_{N(F)} \end{bmatrix} = \begin{bmatrix} Z_{1p} \\ Z_{2p} \\ \vdots \\ Z_{pp} \\ \vdots \\ Z_{Np} \end{bmatrix} I_{p\,(F)} + \begin{bmatrix} 1 \\ 1 \\ \vdots \\ 1 \\ \vdots \\ 1 \end{bmatrix} V_0$$

To calculate V_{bus} (F) we need the faulted bus current Ip (F) which can be determined as discussed below. The fault can be described as shown in Fig.



It is clear that $V_F = Z_F I_F$, $Vp\,(F) = V_F$ and $Ip\,(F) = -I_F$

Therefore $Vp\,(F) = -Z_F\, Ip\,(F)$.

The pth equation extracted from eqngives $Vp\,(F) = Z_{pp} I_p\,(F) + V0$

$Vp\,(F) = -Z_F\, I_p\,(F)$

The pth equation extracted from above equation gives

$V_p\,(F) = Z_{pp} I_p\,(F) + V0$

Substituting eqn. in the above, we get

$- Z_F\ Ip\ (F) = Z_{pp} I_p\ (F) + V0$

Thus the faulted bus current I_p (F) is given by

$$I_{p\,(F)} = - \frac{V_0}{Z_{pp} + Z_F}$$

Substituting the above in eqn. (3.41), the faulted bus voltage Vp (F) is

$$V_{p\,(F)} = \frac{Z_F}{Z_{pp} + Z_F} V_0$$

Finally voltages at other buses at faulted condition are to be obtained. The ithequation extracted from equation gives

$$V_i\ (F) = Z_{ip}\ I_p\ (F) + V0$$

Substituting in the above, we get

$$V_{i\,(F)} = V_0 - \frac{Z_{ip}}{Z_{pp} + Z_F} V_0 \qquad \begin{matrix} i = 1,2,\ldots\ldots\ldots,N \\ i \neq p \end{matrix}$$

Knowing all the bus voltages, current flowing through the various networkelements can be computed asi k_m (F) = (V_k (F) – V_m (F)) yk_m where yk_m is the admittance of element k-m.

When the fault is direct, ZF = 0 and hence

$$I_{p\,(F)} = - \frac{V_0}{Z_{pp}}$$

$$V_{p\,(F)} = 0 \text{ and}$$

$$V_{i\,(F)} = V_0 - \frac{Z_{ip}}{Z_{pp}} V_0 \qquad \begin{matrix} i = 1,2,\ldots\ldots\ldots,N \\ i \neq p \end{matrix}$$

It is to be noted that when the fault occurs at the p_{th} bus, only the p^{th} column of Zbus matrix (and not the entire Zbus matrix) is required for further calculations.

The following are the various steps for conducting symmetrical short circuit analysis.

Step 1 Read i) Transmission line data
ii) Generator reactances data
iii) Faulted bus number p and
iv) Fault impedance Z_f.

Step 2 Construct the bus impedance matrix of the transmission network including the generator reactances.

Step 3 Compute $I_{p(F)} = -\dfrac{V_0}{Z_{pp} + Z_f}$

Step 4 Compute $V_{p(F)} = \dfrac{Z_f}{Z_{pp} + Z_f} V_0$

Step 5 Compute $V_{i(F)} = V_0 - \dfrac{Z_{ip}}{Z_{pp} + Z_f} V_0$ $\quad i = 1,2,\ldots\ldots,N$, $i \neq p$

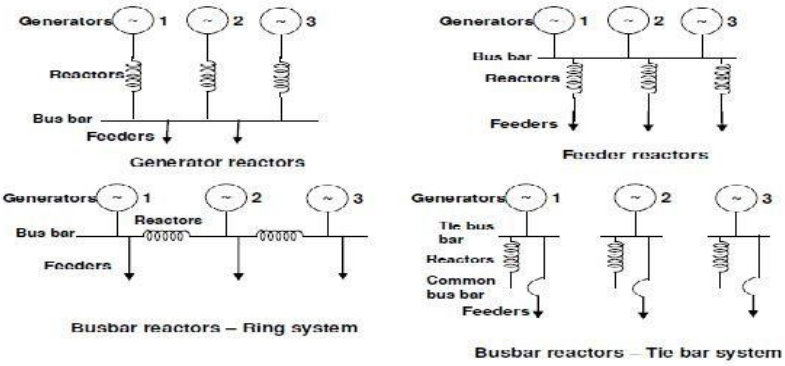
Step 6 Calculate the element currents from $i_{km(F)} = (V_{k(F)} - V_{m(F)})\, y_{km}$

Current Limiting Reactor

A current limiting reactors is also called as series reactors. It is an inductive coil having large inductive reactance compared to the resistance and is used to limit the short circuit current during fault conditions. These reactors are connected in feeders and ties, in generator leads and between the bus sections to reduce the magnitude of the short circuit current. The reactor allow free interchange of power under normal condition. however during fault condition the disturbance is confined to only faulty location. As the resistance of the reactors are small compared to reactance the efficiency of the system is not affected much

Short circuit current is reduced by an increase in the reactance of the system. Short circuit current depends on the generating capacity, voltage at the fault point and the total reactance between the generating point and the fault location. Breaking capacity of the circuit breaker depends on the magnitude of the fault current. If the fault current is beyond the designed limit of the breaking capacity of the breaker, the fault cannot be extinguish. Therefore in large interconnected power system large number of generators and motors feed the fault on occurrence of the fault. Therefore at times the magnitude of the short circuit current exceeds the breaking capacity of the breaker. Therefore it is necessary to limit the fault current by some means. By including a reactor or few reactors at some strategic locations, short circuit currents at different points can be reduced.

The current limiting reactor is an inductive coil having large inductive reactances in comparison to their resistance and is used for limiting short circuit currents during fault conditions. Current-voltage reactors also reduced the voltage disturbances on the rest of the system. It is installed in feeders and ties, in generators leads, and between bus sections, for reducing the magnitude of short circuit currents and the effect of the respective voltage disturbance.Current reactor allows free interchange of power under normal condition, but when the fault occurs the disturbance is restricted by the current reactor to the faulty section. As the resistance of the system is very small as compared to their reactance. Hence, the efficiency of the system is not much affected.



Main Function of Current Limiting Reactor

The main purpose of the current limiting reactor is that its reactance should not decrease when a large short current flows through its windings. When the fault current exceeds about three times rated full-load current then large cross section iron cored reactor is used for limiting the fault current. Because of the large cross-section area, the iron cored reactor becomes very costly and heavy. Therefore, the air cored reactor is usually used to limit the short circuit or fault current.

The iron-cored reactor produces hysteresis and eddy current loss due to which more power is consumed as compared to air cored reactor. Normally, in an air cored reactor, the total losses are of the order of 5% of KVA rating of the reactor.

Functions of Current Limiting Reactor

- Current limiting reactor reduces the flow of short circuit current so as to protect the appliances from mechanical stress and overheating.
- Current reactor reduced the magnitude of voltage disturbances which is caused by short circuits.
- It limits the fault current to flow into the healthy feeders or parts of the system, thereby avoiding the fault from spreading. This increases the chances of continuity of supply.

Drawbacks of current limiting reactor

The main drawbacks of the current limiting reactors are as follows

- When the reactor is installed on the network, the total percentage reactance of the circuit increases.
- It decreases the power factor and thus the regulation becomes poorer.

Advantages:

- Protective reactors are used to reduce the flow of short circuit current at the fault point so as to protect the apparatus from excessive mechanical stresses and from over heating and thus protect the system as a whole
- Protective systems are used to reduce the voltage disturbances caused by the short circuits
- They also localize the fault by limiting the current that flow in to the fault from other healthy feeders or parts of the system thereby avoiding the fault by spreading
- It helps to reduce the duty imposed on the switching equipment during fault conditions

Disadvantages:

- Total percentage reactance of the system increases thereby causing increase in reactive voltage drop and decrease in power factor due to increased angle of lag. Thus regulation of the system becomes poor.

IMPORTANCE SHORT CIRCUIT (OR) FOR FAULT ANALYSIS

A fault in a circuit is any failure which interferes with the normal flow of current. The faults are associated with abnormal change in current, voltage and frequency of the power system.

Faults occur in a power system

The faults occur in a power system due to

(i). Insulation failure of equipment

(ii). Flashover of lines initiated by a lighting stroke

(iii). Due to permanent damage to conductors and towers or due to accidental faulty operations.

Various types of faults

(i) Series fault or open circuit fault

One open conductor fault

Two open conductor fault

(ii) Shunt fault or short circuit fault.

Symmetrical fault or balanced fault

§ Three phase fault

Unsymmetrical fault or unbalanced fault

§ Line to ground (L-G) fault

§ Line to Line (L-L) fault

§ Double line to ground (L-L-G) fault

Relative frequency of occurrence of various types of fault

Types of fault	Relative frequency of occurrence of faults
Three phase fault	5%
Double line to ground fault	10%
Line to Line fault	15%
Line to ground fault	70%

Symmetrical fault or balanced three phase fault

This type of fault is defined as the simultaneous short circuit across all the three phases. It occurs infrequently, but it is the most severe type of fault encountered. Because the network is balanced, it is solved by per phase basis using Thevenins theorem or bus impedance matrix or KVL, KCL laws.

ASSUMPTIONS IN SHORT CIRCUIT ANALYSIS

Basic assumptions in fault analysis of power systems.

(i). Representing each machine by a constant voltage source behind proper reactance which may be X", X', or X

(ii). Pre-fault load current are neglected

(iii). Transformer taps are assumed to be nominal

(iv). Shunt elements in the transformers model that account for magnetizing current and core loss are neglected

(v). A symmetric three phase power system is conducted

(vi). Shunt capacitance and series resistance in transmission are neglected

(vii). The negative sequence impedances of alternators are assumed to be the same as their positive sequence impedance Z+ = Z-

Need for short circuit studies or fault analysis

Short circuit studies are essential in order to design or develop the protective schemes for various parts of the system. To estimate the magnitude of fault current for the proper choice of circuit breaker and protective relays.

Bolted fault or solid fault

A Fault represents a structural network change equivalent with that caused by the addition of impedance at the place of a fault. If the fault impedance is zero, the fault is referred as bolted fault or solid fault.

Reason for transients during short circuits

The faults or short circuits are associated with sudden change in currents. Most of the components of the power system have inductive property which opposes any sudden change in currents, so the faults are associated with transients.

Doubling effect

If a symmetrical fault occurs when the voltage wave is going through zero then the maximum momentary short circuit current will be double the value of maximum symmetrical short circuit current. This effect is called doubling effect.

DC off set current

The unidirectional transient component of short circuit current is called DC off set current.

Symmetrical fault analysis through bus impedance matrix

(i). Adding branch of impedance from new bus to reference bus Zbus = [Zb]

(ii). Adding brance of impedance from new bus to existing bus Zbus = [Zorg ….

…… Zb+Zqq]

(iii). Adding branch of impedance from existing bus to ref bus

(iv). Adding branch of impedance between 2 existing bus

Bus impedance matrix

Bus impedance matrix is the inverse of the bus admittance matrix. The matrix consisting of driving point impedance and transfer impedances of the network is called as bus impedance matrix. Bus impedance matrix is symmetrical.

Methods available for forming bus impedance matrix

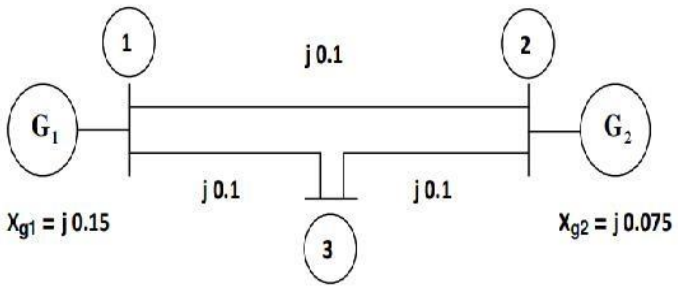
(i). Form bus admittance matrix and take the inverse to get bus impedance matrix.

(ii). Using bus building algorithm.

(iii). Using L-U factorization of Y-bus matrix.

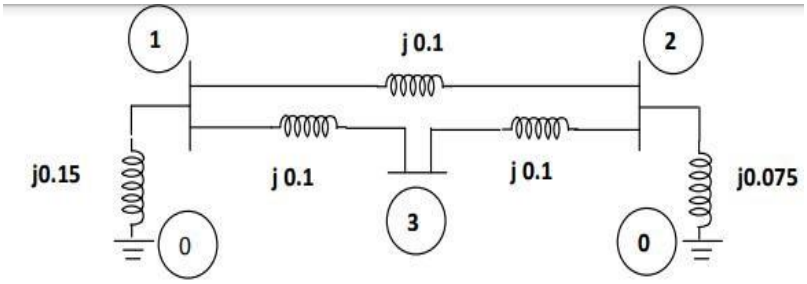
Problem:1

Consider the power system shown in Fig. The values marked are p.u. impedances. The p.u. reactances of the generator 1 and 2 are 0.15 and 0.075 respectively. Compute the bus impedance matrix of the generator – transmission network.



Solution :

The ground bus is numbered as 0 and it is taken as reference bus. The p.u. impedance diagram is shown in Fig.



When element 0 – 1 is included

$$Z_{bus} = j \begin{matrix} \\ 1 \end{matrix} \begin{matrix} 1 \\ [0.15] \end{matrix}$$; When element 0 – 2 is included $$Z_{bus} = j \begin{matrix} & 1 & 2 \\ 1 \\ 2 \end{matrix} \begin{bmatrix} 0.15 & 0 \\ 0 & 0.075 \end{bmatrix}$$

Element 1 – 2 is added; it is a link between buses 1 and 2. With bus ℓ

$$Z_{bus} = j \begin{matrix} & 1 & 2 & \ell \\ 1 \\ 2 \\ \ell \end{matrix} \left[\begin{array}{cc|c} 0.15 & 0 & 0.15 \\ 0 & 0.075 & -0.075 \\ \hline 0.15 & -0.075 & 0.325 \end{array}\right]$$;

Eliminating the ℓ^{th} bus

$$Z_{bus} = j \begin{matrix} & 1 & 2 \\ 1 \\ 2 \end{matrix} \begin{bmatrix} 0.08077 & 0.034615 \\ 0.034615 & 0.05769 \end{bmatrix}$$

Add element 1 – 3. It is a branch from bus 1 and it creates bus 3.

$$Z_{bus} = j \begin{array}{c} \\ 1 \\ 2 \\ 3 \end{array} \begin{array}{c} \begin{array}{ccc} 1 & 2 & 3 \end{array} \\ \begin{bmatrix} 0.08077 & 0.034615 & 0.08077 \\ 0.034615 & 0.05769 & 0.034615 \\ 0.08077 & 0.034615 & 0.18077 \end{bmatrix} \end{array}$$

Finally add element 2 – 3. It is a link between buses 2 and 3. With bus ℓ

$$Z_{bus} = j \begin{array}{c} \\ 1 \\ 2 \\ 3 \\ \ell \end{array} \begin{array}{c} \begin{array}{cccc} 1 & 2 & 3 & \ell \end{array} \\ \left[\begin{array}{ccc|c} 0.08077 & 0.034615 & 0.08077 & -0.046155 \\ 0.034615 & 0.05769 & 0.034615 & 0.023075 \\ 0.08077 & 0.034615 & 0.18077 & -0.146155 \\ \hline -0.046155 & 0.023075 & -0.146155 & 0.26923 \end{array}\right] \end{array}$$

$$Z_{bus} = j \begin{array}{c} \\ 1 \\ 2 \\ 3 \end{array} \begin{array}{c} \begin{array}{ccc} 1 & 2 & 3 \end{array} \\ \begin{bmatrix} 0.07286 & 0.03857 & 0.05571 \\ 0.03857 & 0.05571 & 0.04714 \\ 0.05571 & 0.04714 & 0.10143 \end{bmatrix} \end{array}$$

Symmetrical short circuit analysis using Thevenin's theorem

An alternate method of computing Short Circuit Current Computation is through the application of the Thevenin theorem. This Short Circuit Current Computation method is faster and easily adopted to systematic computation for large networks. While the method is perfectly general, it is illustrated here through a simple example.

Consider a synchronous generator feeding a synchronous motor over a line. Figure 9.13a shows the circuit model of the system under conditions of steady load. Fault computations are to be made for a fault at F, at the motor terminals. As a first step the circuit model is replaced by the one shown in Fig. 9.13b, wherein the synchronous machines are represented by their transient reactances (or subtransient reactances if subtransient currents are of interest) in series with voltages behind transient reactances. This change does not disturb the prefault current I° and prefault voltage V° (at F).

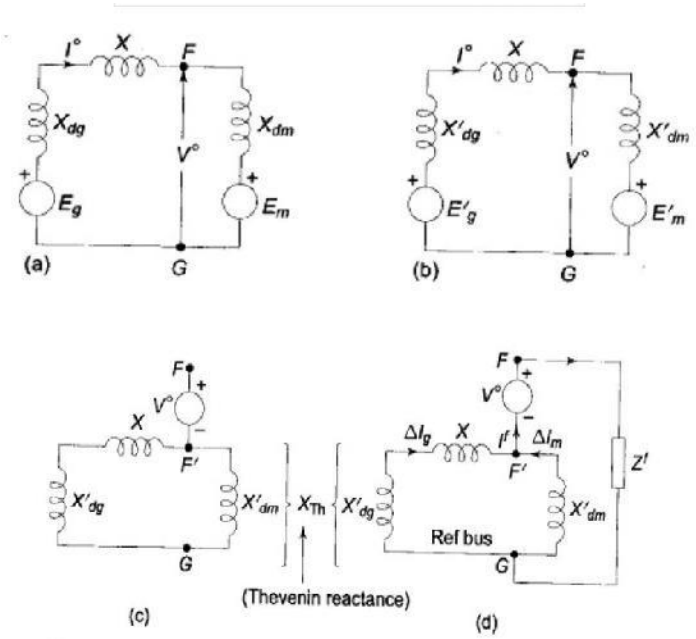
As seen from FG the Thevenin equivalent circuit of Fig. 9.13b is drawn in Fig. 9.13c. It comprises prefault voltage V° in series with the passive Thevenin impedance network. It is noticed that the prefault current I° does not appear in the passive Thevenin impedance network. It is therefore to be remembered that this current must be accounted for by superposition after the SC solution is obtained through use of the Thevenin equivalent.

Consider now a fault at F through an impedance Zf Figure 9.13d shows the Thevenin equivalent of the system feeding the fault impedance. We can immediately write

$$I^f = \frac{V^\circ}{jX_{\text{Th}} + Z^f}$$

Current caused by fault in generator circuit

$$\Delta I_g = \frac{X'_{dm}}{(X'_{dg} + X + X'_{dm}} I^f$$



Current caused by fault in motor circuit

$$\Delta I_m = \frac{X'_{dg} + X}{(X'_{dm} + X + X'_{dg})} I^f$$

Post fault currents and voltages are obtained as follows by superposition:

$$I_g^f = I^o + \Delta I_g$$
$$I_m^f = -I^o + \Delta I_m \text{ (in the direction of } \Delta I_m)$$

Post fault voltage

$$V^f = V^o + (-jX_{Th} I^f) = V^o + \Delta V$$

where $\Delta V = -jX_{Th} I_f$ is the voltage of the fault point F′ on the Thevenin passive network (with respect to the reference bus G) caused by the flow of fault current I_f.

The above approach to SC computation is summarized in the following four steps:

An observation can be made here. Since the prefault current flowing out of fault point F is always zero, the postfault current out of F is independent of load for a given prefault voltage at F.

step 1: Obtain steady state solution of loaded system (load flow study).

Step 2: Replace reactances of synchronous machines by their subtransient/ transient values. Short circuit all emf sources. The result is the passive Thevenin network.

Step 3: Excite the passive network of Step 2 at the fault point by negative of prefault voltage (see Fig. 9.13d) in series with the fault impedance. Compute voltages and currents at all points of interest.

Step 4: Postfault currents and voltages are obtained by adding results of Steps 1 and 3.

The following assumptions can be safely made in SC computations leading to considerable computational simplification:

Assumption 1: All prefault Voltage magnitudes are 1 pu.

Assumption 2: All prefault currents are zero.

The first assumption is quite close to actual conditions as under normal operation all voltages (pu) are nearly unity.

The changes in current caused by Short Circuit Current Computation are quite large, of the order of 10-20 pu and are purely reactive; whereas the prefault load currents are almost purely real. Hence the total postfault current which is the result of the two currents can be taken in magnitude equal to the larger component (caused by the fault). This justifies assump-tion 2.

SYMMETRICAL FAULT

In symmetrical faults all the three phases are short circuited to each other and to earth also. Such faults are balanced and symmetrical in the sense that the voltage and current of the system remains balanced even after the fault and it is enough if we consider any one phase

Short circuit capacity of power system or fault level.

Short circuit capacity (SCC) or Short circuit MVA or fault level at a bus is defined as the product of the magnitude of the pre fault bus voltage and the post fault current

$$\text{SCC or Short circuit MVA} = |V_{prefault}| \times |I_f|$$

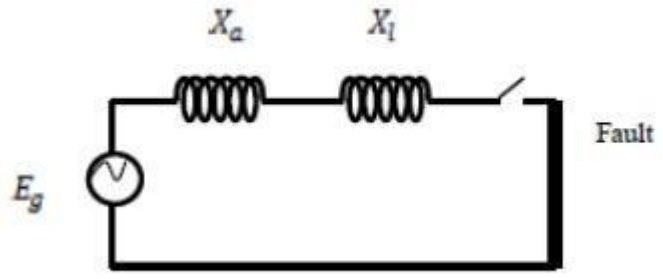
(OR)

$$\text{SCC} = \frac{1}{x_{th}} \; p.u \; MVA$$

Synchronous reactance or steady state condition reactance

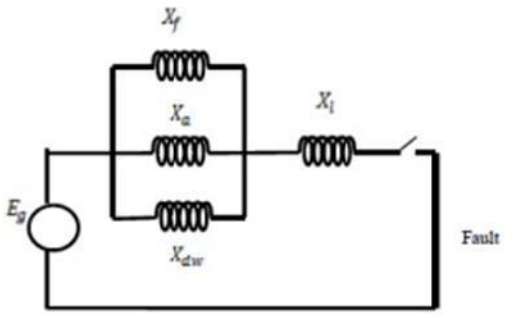
The synchronous reactance is the ratio of induced emf and the steady state rms current. It is the sum of leakage reactance (Xl) and the armature reactance (Xa).

$$X_d = X_a + X_l$$



Sub transient reactance

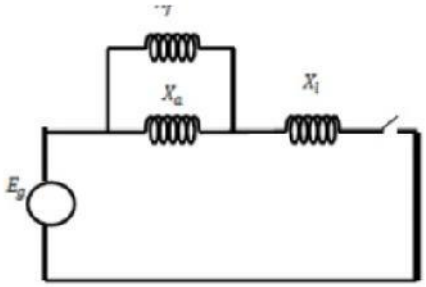
The synchronous reactance is the ratio of induced emf on no load and the sub transient symmetrical rms current



$$X''_d = X_l + \frac{X_a + X_f}{X_a X_f}$$

Transient reactance

The synchronous reactance is the ratio of induced emf on no load and the transient symmetrical rms current.



$$X'_d = X_l + \frac{1}{\frac{1}{X_a} + \frac{1}{X_f}}$$

Thevenin's theorem:

(i). Fault current = Eth / (Zth+Zf)

(ii). Determine current contributed by the two generators IG1 = If * (Z2/(Z1+Z2))

I_{G2} = If * (Z_1 / (Z_1+Z_2))

(iii). Determine Post fault voltage V_{if} = Vi°+ΔV = V°+(-Z_{i2}*I_{Gi})

(iv). Determine post fault voltage line flows Iij = (V_i – V_j) / Z_{ij} series

(v). Short circuit capacity If = | Eth | 2 / Xth