UNIT IV – ANALOG MULTIPLIER AND PLL

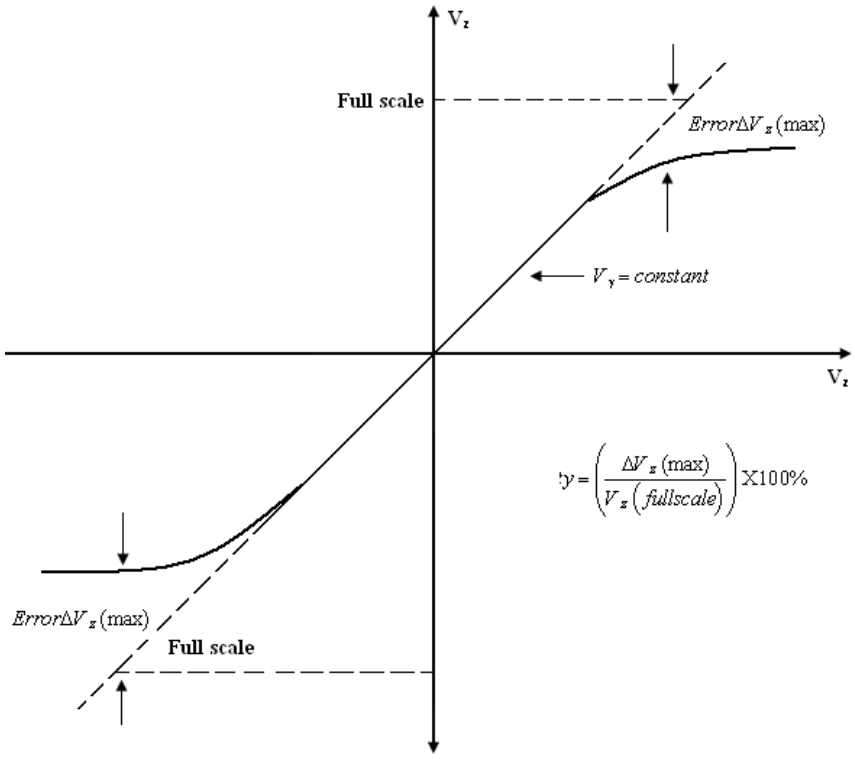
Analog Multipliers:

A multiple produces an output V_0, which is proportional to the product of two inputs V_x and V_y.

That is, $V_0 = KV_xV_y$ where K is the scaling factor that is usually maintained as (1/10) V^{-1}. There are various methods available for performing analog multiplication. Four of such techniques, namely,

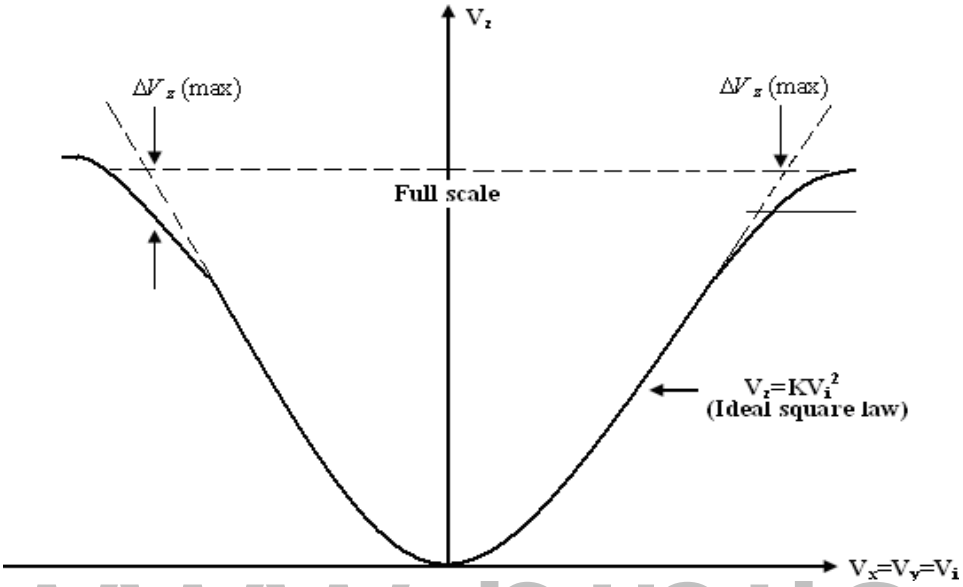
1. Logarithmic summing technique
2. Pulse height/width modulation Technique
3. Variable trans conductance Technique
4. Multiplication using Gilbert cell and
5. Multiplication using variable trans conductance technique.

An actual multiplier has its output voltage V_0 defined by



Squaring Mode Accuracy:

The Square – law curve is obtained with both the X and Y inputs connected together and applied with the same input signal. The maximum derivation of the output voltage from an ideal square – law curve expresses the squaring mode accuracy.



Bandwidth:

The Bandwidth indicates the operating capability of an analog multiplier at higher frequency values. Small signal 3 dB bandwidth defines the frequency f_0 at which the output reduces by 3dB from its low frequency value for a constant input voltage. This is identified ind ividually for the X and Y input channels normally.

The transconductance bandwidth represents the frequency at which the transconductance of the multiplier drops by 3dB of its low frequency value. This characteristics defines the application frequency ranges when used for phase detection or AM detection.

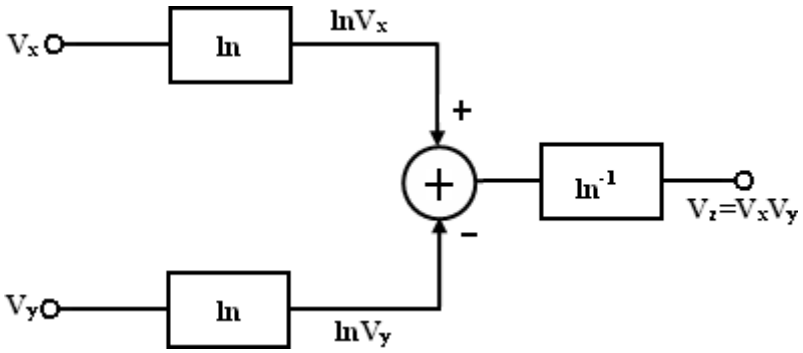
Quadrant:

The quadrant defines the applicability of the circuit for bipolar signals at its inputs. First – quadrant device accepts only positive input signals, the two quadrant device accepts one bipolar signal and one unipolar signal and the four quadrant device accepts two bipolar signals.

Logarithmic summing Technique:

This technique uses the relationship

$\ln V_x + \ln V_y = \ln(V_x V_y)$



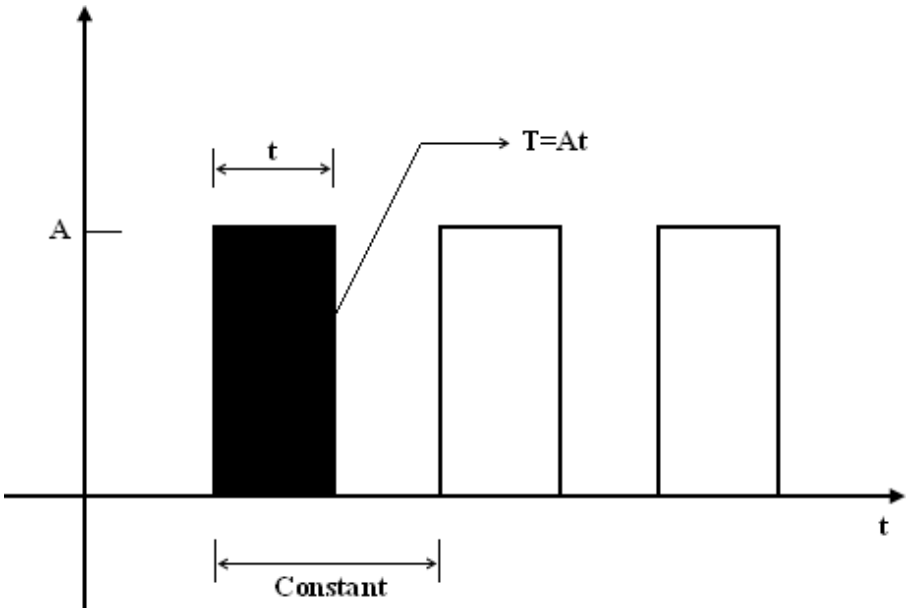
As shown in figure the input voltages V_x and V_y are converted to their logarithmic equivalent, which are then added together by a summer. An antilogarithmic converter produces the output voltage of the summer. The output is given by,

$V_z = \ln^{-1} (\ln(V_x V_y)) = V_x V_y$ The exponential relationship between the collector current and base

to emitter voltage of bipolar transistor during its active mode of operation could be explained for the logarithmic and anti- logarithmic conversions. The relationship between I_0 and V_{BE} of the transistor is given by

$I_C = I_0 e^{(VBE /VT)}$ It is found that the transistor follows the relationship very accurately in the range of 10nA to 100mA. Logarithmic multiplier has low accuracy and high temperature instability. This method is applicable only to positive values of V_x and V_y. Therefore, this type of multiplier is restricted to one quadrant operation only.

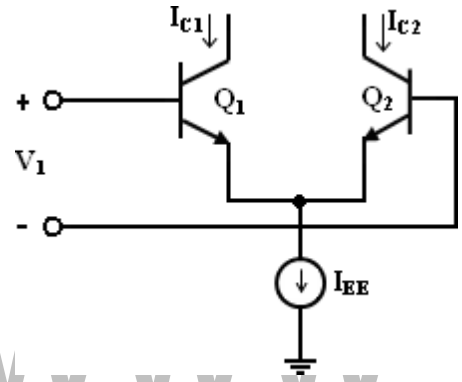
Pulse Height/ Width Modulation Technique:



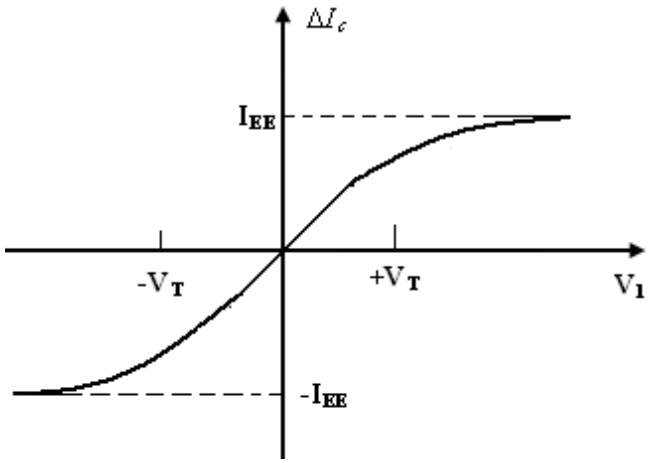
In this method, the pulse width of a pulse train is made proportional to one input voltage and the pulse amplitude is made proportional to the second input voltage. Therefore, $V_x = K_x A$, $V_y = K_y t$, and $V_z = K_z T$ where K_x, K_y, K_z are scaling factors. In figure A is the amplitude of the pulse, t is the pulse width and T is the area of the pulse. Therefore,

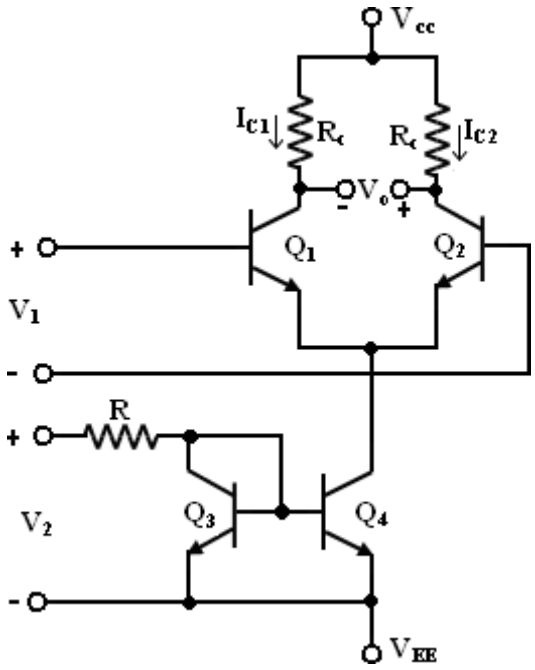
The modulated pulse train is passed through an integrated circuit. Therefore, the input of the integrator is proportional to the area of pulse, which in turn is proportional to the product of two input voltages.

A simple multiplier using an Emitter coupled Transistor pair:



A circuit using an emitter coupled pair is shown in figure. The output currents I_{C1} and I_{C2} arrelatedto the differential input voltage The dc transfer characteristics of the emitter – coupled pair is shown in figure. It shows that the emitter coupled pair can be used as a simple multiplier using this configuration. When the differential input voltage $V_1 << V_T$, we can appropriate as given by





This arrangement is shown in figure. It is a simple modulator circuit constructed using a differential amplifier. It can be used as a multiplier, provided V_1 is small and much less than 50mV, and V_2 is greater than $V_{BE(on)}$. But, the multiplier circuit shown in figure has several limitations. The first limitation is that V_2 is offset by $V_{BE(on)}$. The second is that V_2 must always be positive which results in only a two-quadrant multiplier operation. The third limitation is that, the tanh (X) is approximately as X, where $X = V_1 / 2V_T$. The first two limitations are overcome in the Gilbert cell.

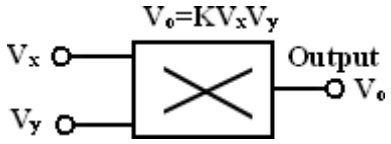
Gilbert Multiplier cell:

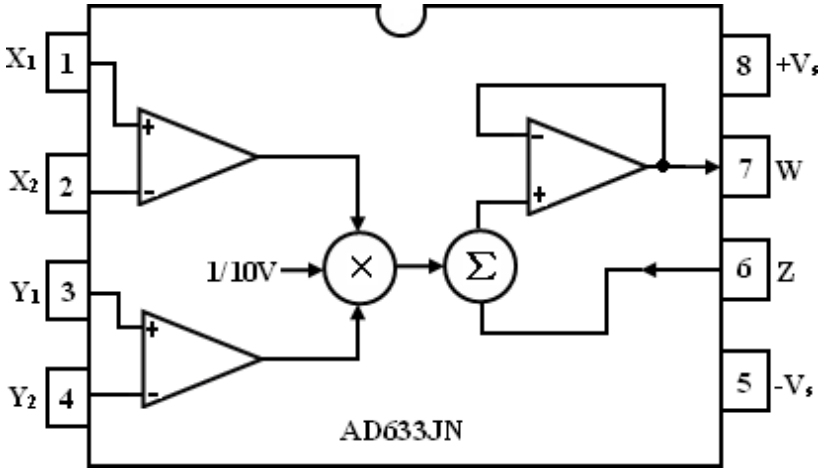
The Gilbert multiplier cell is a modification of the emitter coupled cell and this allows four – quadrant multiplication. Therefore, it forms the basis of most of the integrated circuit balanced

multipliers. Two cross- coupled emitter- coupled pairs in series connection with an emitter coupled pair form the structure of the Gilbert multiplier cell.

Analog Multiplier ICs

Analog multiplier is a circuit whose output voltage at any instant is proportional to the product of instantaneous value of two individual input voltages. The important applications of these multipliers are multiplication, division, squaring and square – rooting of signals, modulation and demodulation. These analog multipliers are available as integrated circuits consisting of op-amps and other circuit elements. The Schematic of a typical analog multiplier, namely, AD633 is shown in figure.





The AD633 multiplier is a four – quadrant analog multiplier. It possesses high input impedance, and this characteristic makes the loading effect on the signal source negligible. It can operate with supply voltages ranging from ±18V. The IC does not require external components. The calibration by user is not necessary. The typical range of the two input signals is ±10V.

Schematic representation of a multiplier:

The schematic representation of an analog multiplier is shown in figure. The output V_0 is the product of the two inputs V_x and V_y is divided by a reference voltage Vref. Normally, the reference voltage Vref is internally set to 10V. Therefore, V_0 =VxVy/10. In other words, the basic input – output relationship can be defined by $KV_x V_y$ when K = 1/10, a constant. Thus for peak input voltages of 10V, the peak magnitude of output voltage is 1/10 *10 *10 =10V. Thus, it can be noted that, as long as $V_x < 10V$ and $V_y < 10V$, the multiplier output will not saturate.

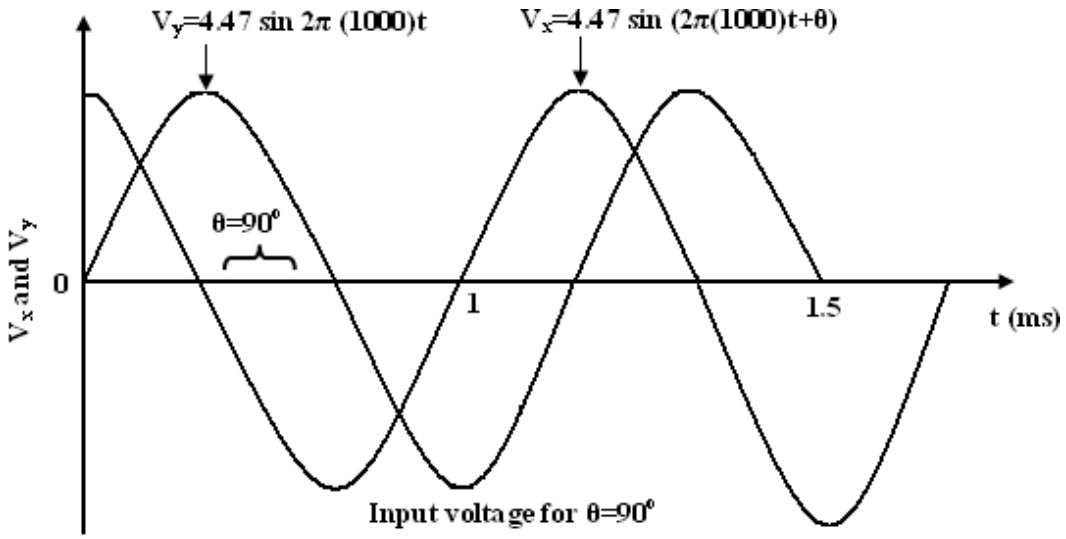
Multiplier quadrants:

The transfer characteristics of a typical four-quadrant multiplier is shown in figure. Both the inputs can be positive or negative to obtain the corresponding output as shown in the transfer characteristics.

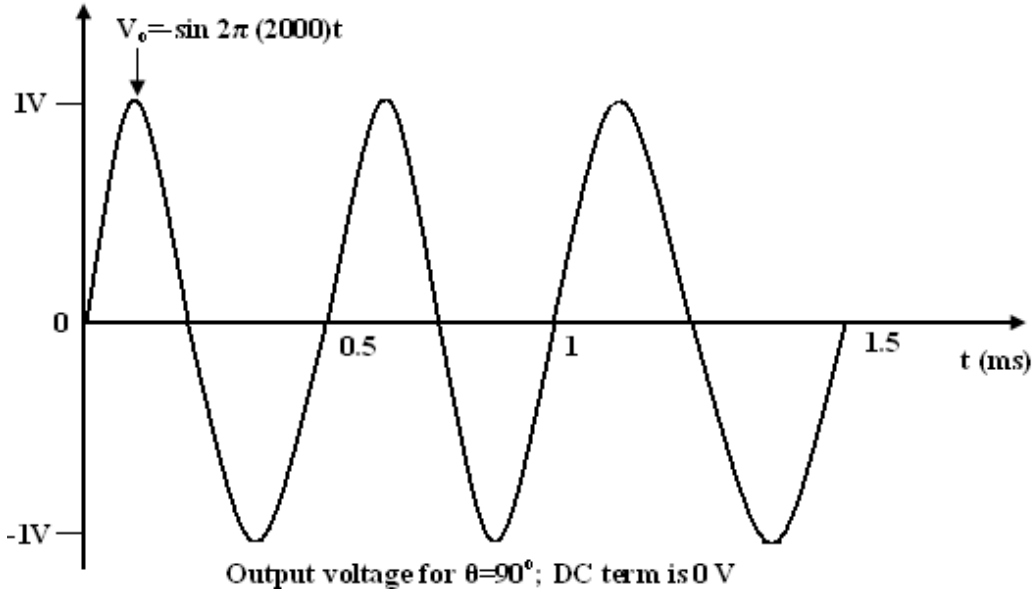
Applications of Multiplier ICs:

The multiplier ICs are used for the following purposes:

1. Voltage Squarer
2. Frequencydoubler



Input voltage for θ=90°



Output voltage for θ=90°; DC term is 0 V

CONTROL SYSTEM ANALYSIS/ CLOSED LOOP ANALYSIS OF PLL

Phase locked loops can also be analyzed as control systems by applying the Laplace transform. The loop response can be written as:

Where

δo is the output phase in radians

δi is the input phase in radians

Kp is the phase detector gain in volts per radian

Kv is the VCO gain in radians per volt-second

F(s) is the loop filter transfer function (dimensionless)

The loop characteristics can be controlled by inserting different types of loop filters. The simplest filter is a one-pole RC circuit. The loop transfer function in this case is:

$$F(s) = \frac{1}{1 + sRC}$$

The loop response becomes:

$$\frac{\theta_o}{\theta_i} = \frac{\frac{K_p K_v}{RC}}{s^2 + \frac{s}{RC} + \frac{K_p K_v}{RC}}$$

This is the form of a classic harmonic oscillator. The denominator can be related to that of a second order system:

$$s^2 + 2s\zeta\omega_n + \omega_n^2$$

Where

δ is the damping factor

ωn is the natural frequency of the loop For the one-pole RC filter,

$$\omega_n = \sqrt{\frac{K_p K_v}{RC}}$$

$$\zeta = \frac{1}{2\sqrt{K_p K_v RC}}$$

The loop natural frequency is a measure of the response time of the loop, and the damping factor is a measure of the overshoot and ringing. Ideally, the natural frequency should be high and the damping factor should be near 0.707 (critical damping). With a single pole filter, it is not possible to control the loop frequency and damping factor independently. For the case of criticaldamping,

$$RC = \frac{1}{2K_p K_v}$$

$$\omega_c = K_p K_v \sqrt{2}$$

A slightly more effective filter, the lag-lead filter includes one pole and one zero. This can be realized with two resistors and one capacitor. The transfer function for this filter is

$$F(s) = \frac{1 + sCR_2}{1 + sC(R_1 + R_2)}$$

This filter has two time constants

τ1 = C(R1 + R2) τ2 = CR2

Substituting above yields the following natural frequency and damping factor

$$\omega_n = \sqrt{\frac{K_p K_v}{\tau_1}} \qquad \zeta = \frac{1}{2\omega_n \tau_1} + \frac{\omega_n \tau_2}{2}$$

The loop filter components can be calculated independently for a given natural frequency and damping factor

$$\tau_1 = \frac{K_p K_v}{\omega_n^2}$$

$$\tau_2 = \frac{2\zeta}{\omega_n} - \frac{1}{K_p K_v}$$

Real world loop filter design can be much more complex eg using higher order filters to reduce various types or source of phase noise.

Applications of PLL:

The PLL principle has been used in applications such as FM ste reo decoders, motor speed control, tracking filters, FM modulation and demodulation, FSK modulation, Frequency multiplier, Frequency synthesis etc.,

Example PLL ICs:

560 series (560, 561, 562, 564, 565 & 567)

Feedback path and optional divider:

Most PLLs also include a divider between the oscillator and the feedback input to the phase detector to produce a frequency synthesizer. A programmable divider is particularly useful in radio transmitter applications, since a large number of transmit frequencies can be produced from a single stable, accurate, but expensive, quartz crystal–controlled reference oscillator.

Some PLLs also include a divider between the reference clock and the reference input to the phase detector. If this divider divides by M, it allows the VCO to multiply the reference frequency by N / M. It might seem simpler to just feed the PLL a lower frequency, but in some cases the reference frequency may be constrained by other issues, and then the reference divider is useful. Frequency multiplication in a sense can also be attained by locking the PLL to the 'N'th harmonic of the signal.

Equations:

The equations governing a phase-locked loop with an analog multiplier as the phase detector may be derived as follows. Let the input to the phase detector be xc(t) and the output of the voltage-controlled oscillator (VCO) is xr(t) with frequency ωr(t), then the output of the phase detector xm(t) is given by

$$x_m(t) = x_c(t) \cdot x_r(t)$$

the VCO frequency may be written as a function of the VCO input y(t) as

$$\omega_r(t) = \omega_f + g_v y(t)$$

where gv is the sensitivity of the VCO and is expressed in Hz / V.

Hence the VCO output takes the form

$$x_r(t) = A_r \cos\left(\int_0^t \omega_r(\tau)\, d\tau\right) = A_r \cos(\omega_f t + \varphi(t))$$

where

The loop filter receives this signal as input and produces an output

xf(t) = Ffilter(xm(t))

where FFilter is the operator representing the loop filter transformation.

When the loop is closed, the output from the loop filter becomes the input to the VCO thus

y(t) = xf(t) = Ffilter(xm(t))

We can deduce how the PLL reacts to a sinusoidal input signal:

xc(t) = Acsin(ωct).

The output of the phase detector then is:

This can be rewritten into sum and difference components using trigonometric identities:

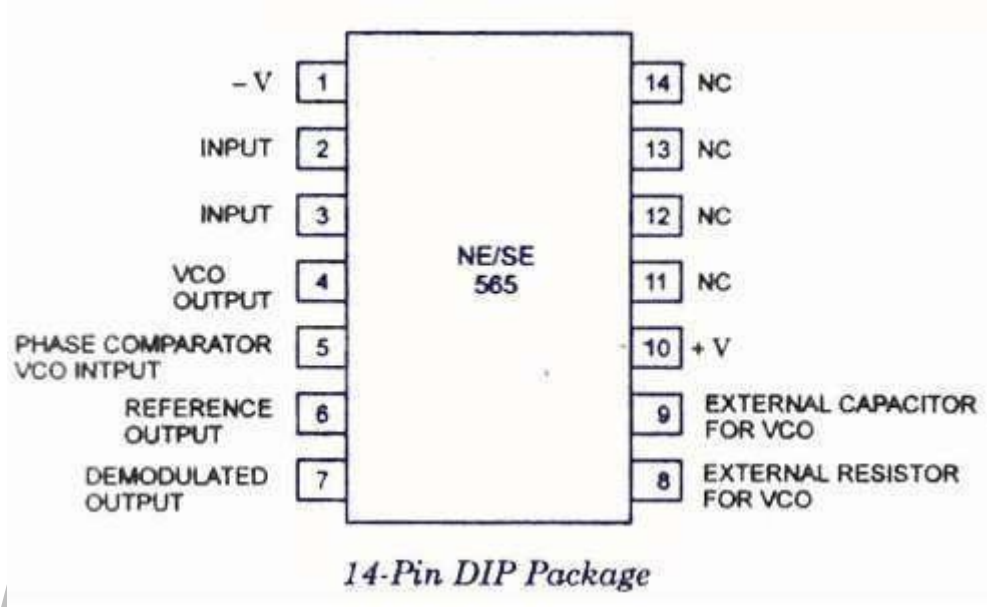
$$x_m(t) = \frac{A_c A_f}{2} \sin(\omega_c t - \omega_f t - \varphi(t)) + \frac{A_c A_f}{2} \sin(\omega_c t + \omega_f t + \varphi(t))$$

As an approximation to the behaviour of the loop filter we may consider only the difference frequency being passed with no phase change, which enables us to derive a small-signal model of the phase- locked loop. If we can make $\omega_f \approx \omega_c$, then the $\sin(\cdot)$ can be approximated by its argument resulting in: $y(t) = x_f(t) \simeq -A_c A_f \varphi(t)/2$.

The phase- locked loop is said to be locked if this is the case.

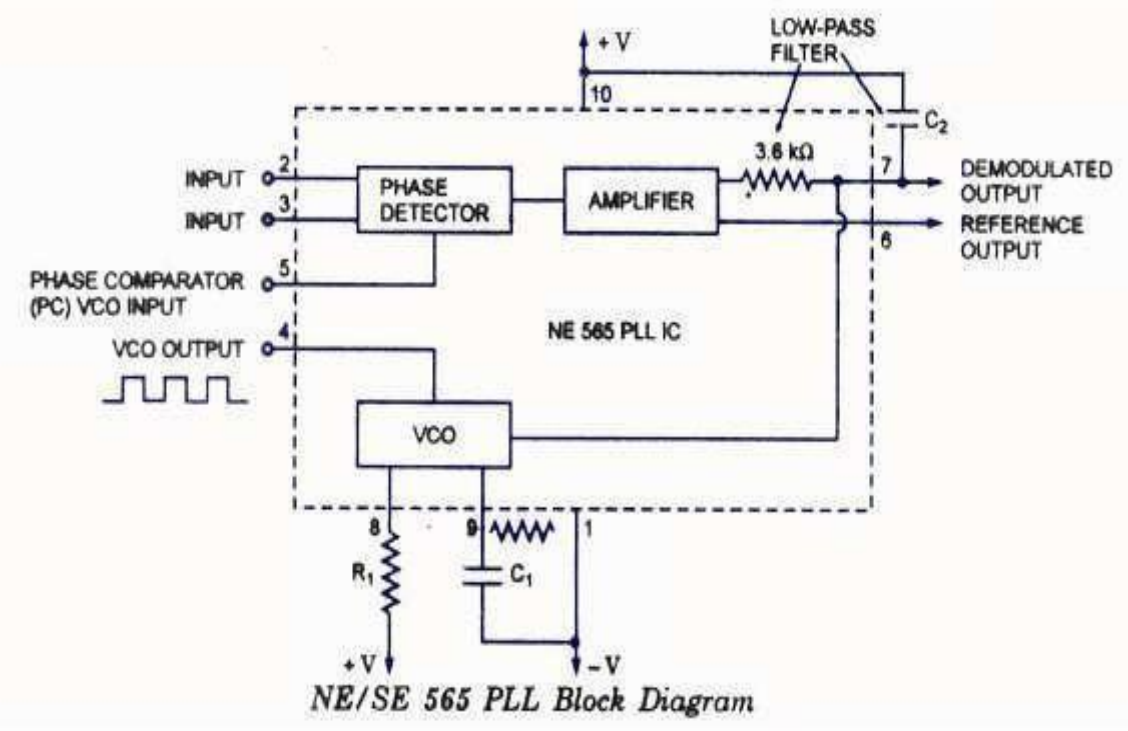
MONOLITHIC PHASE LOCKED LOOPS (PLL IC 565):

Pin Configuration of PLL IC 565:



14-Pin DIP Package

Basic Block Diagram Representation of IC 565



NE/SE 565 PLL Block Diagram

The signetics NE/SE 560 series is monolithic phase locked loops. The SE/NE 560, 561,

562, 564, 565 & 567 differ mainly in operating frequency range, poser supply requirements & frequency & bandwidth adjustment ranges. The important electrical characteristics of the 565 PLL are,

- Operating frequency range: 0.001Hz to 500 Khz.
- Operating voltage range: ±6 to ±12v
- Input level required for tracking: 10mv rms min to 3 Vpp max
- Input impedance: 10 K ohms typically.
- Output sink current: 1mA
- Output source current: 10 mA

The center frequency of the PLL is determined by the free running frequency of the VCO, which is given by

$$f_{OUT} = \frac{1.2}{4R1C1} \text{ Hz} \quad \text{---------- (1)}$$

where R1&C1 are an external resistor & a capacitor connected to pins 8 & 9.

- The VCO free-running frequency f_{OUT} is adjusted externally with R1 & C1 to be at the center of the input frequency range.
- C1 can be any value, R1 must have a value between 2 k ohms and 20 K ohms.
- Capacitor C2 connected between 7 & +V.
- The filter capacitor C2 should be large enough to eliminate variations in the demod ulated output voltage in order to stabilize the VCO frequency.
- The lock range f_L & capture range fc of PLL is givenby,

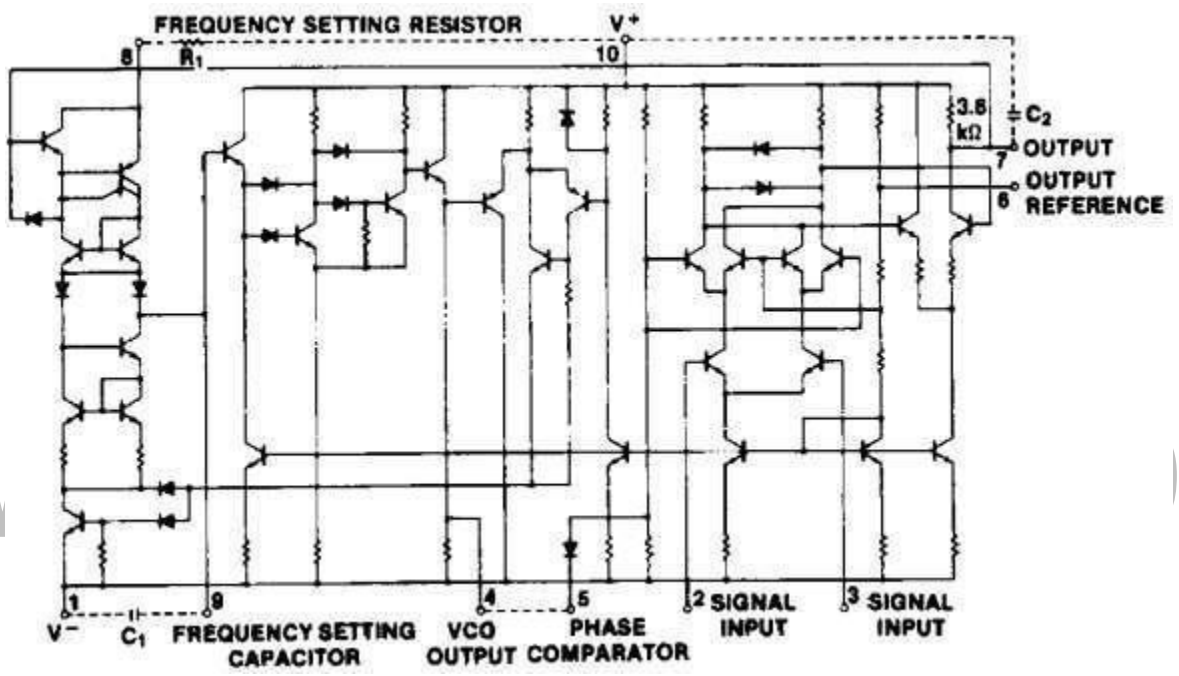
$$f_L = \pm \frac{8 \text{ fout}}{V} \text{ Hz} \quad \text{---------- (2)}$$

Where f_{OUT} = free running frequency of VCO (Hz)

V = (+V)-(-V) volts

$$f_C = \pm\left[\frac{f_L}{(2\Pi)(3.6)(10^3)C_2}\right]^{1/2} \quad (3)$$

The circuit diagram of LM565 PLL



Monolithic PLL IC 565 applications :

The output from a PLL system can be obtained either as the voltage signal $v_c(t)$ corresponding to the error voltage in the feedback loop, or as a frequency signal at VCO output terminal. The voltage output is used in frequency discriminator applications whereas the frequency output is used in signal conditioning, frequency synthesis or clock recovery applications.

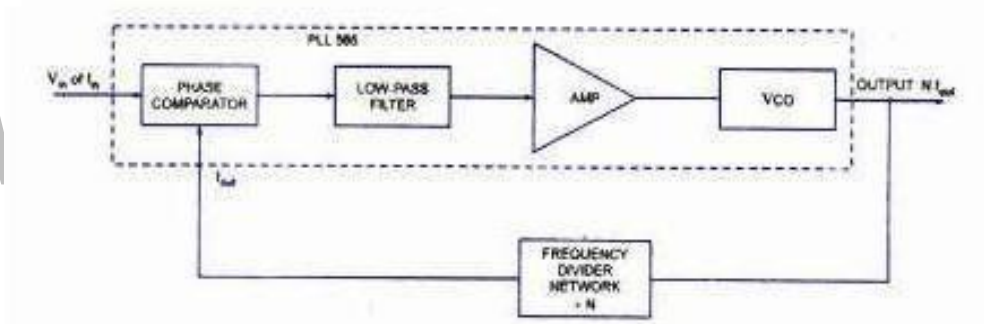
Consider the case of voltage output. When PLL is locked to an input frequency, the error voltage $v_c(t)$ is proportional to (f_s-f_o). If the input frequency is varied as in the case of FM signal, v_c will also vary in order to maintain the lock. Thus the voltage output serves as a frequency discriminator which converts the input frequency changes to voltage changes.

In the case of frequency output, if the input signal is comprised of many frequency co mponents corrupted with noise and other disturbances, the PLL can be made to lock, selectively on one

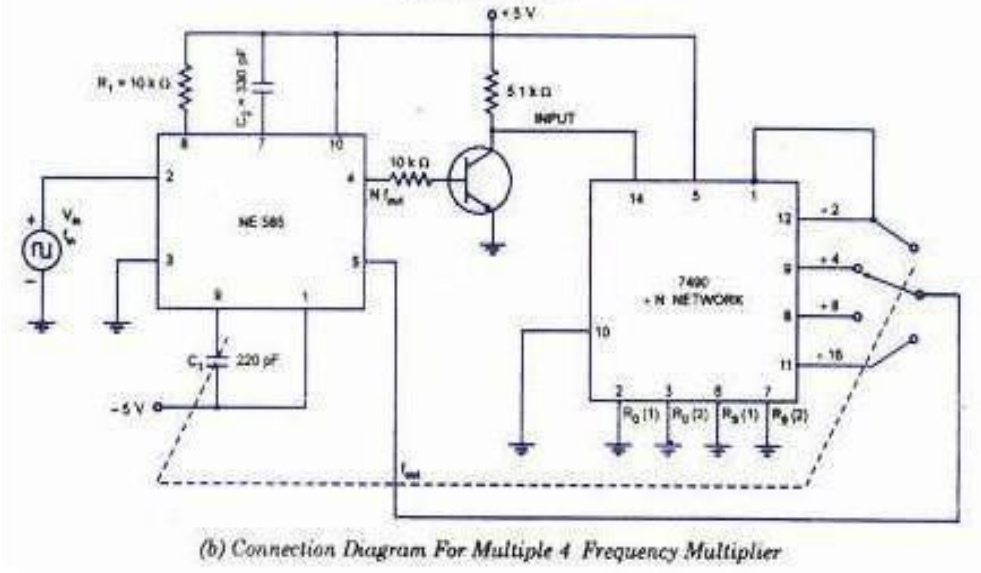
particular frequency component at the input. The output of VCO would then regenerate that particular frequency (because of LPF which gives output for beat frequency) and attenuate heavily other frequencies. VCO output thus can be used for regenerating or reconditioning a desired frequency signal (which is weak and buried in noise) out of many undesirable frequency signals. Some of the typical applications of PLL are discussed below.

(i) Frequency Multiplier:

- Frequency divider is inserted between the VCO & phase comparator. Since the output of the divider is locked to the f_{IN}, VCO is actually running at a multiple of the input frequency.
- The desired amount of multiplication can be obtained by selecting a proper divide-by-N network, where N is an integer.



(a) Block Diagram

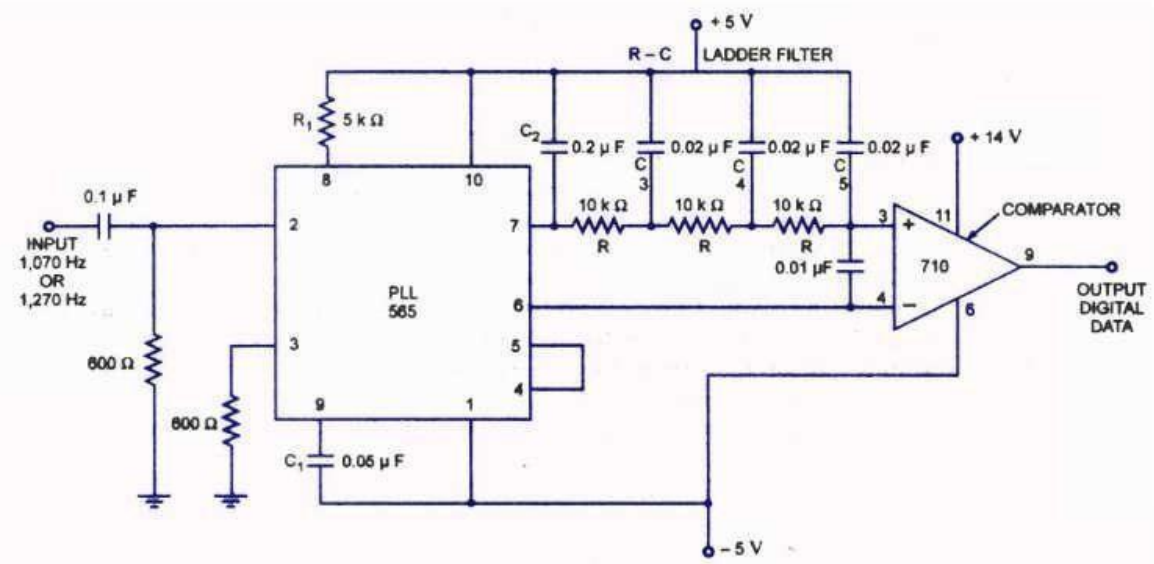


(b) Connection Diagram For Multiple 4 Frequency Multiplier

(ii) Frequency Shift Keying (FSK) demodulator:

In computer peripheral & radio (wireless) communication the binary data or code is transmitted by means of a carrier frequency that is shifted between two preset frequencies. Since a carrier frequency is shifted between two preset frequencies, the data transmission is said to use a FSK. The frequency corresponding to logic 1 & logic 0 states are commonly called the mark & space frequency.

For example, When transmitting teletype writer information using a modulator-demodulator (modem) a 1070-1270 (mark-space) pair represents the originate signal, while a 2025-2225 Hz (mark-space) pair represents the answer signal.



565 As An FSK Demodulator

FSK Generator:

- The FSK generator is formed by using a 555 as an astable multivibrator, whose frequency is controlled by the sate of transistor Q1.
- In other words, the output frequency of the FSK generator depends on the logic state of the digital data input.
- 150 Hz is one the standards frequencies at which the data are commonly transmitted.
- When the input is logic 1, the transistor Q1 is off. Under the condition, 555 timer works in its normal mode as an astable multivibrator i.e., capacitor C charges through R_A & R_B to 2/3 Vcc & discharges through R_B to 1/3 Vcc.

  Thus capacitor C charges & discharges between 2/3 Vcc & 1/3 Vcc as long as the input is logic

□ The frequency of the output waveform is given by,

$$fo = \frac{1.45}{(R_A + 2R_B)C} = 1070 \text{ Hz (mark frequency)}$$

□ When the input is logic 0, (Q1 is ON saturated) which inturn connects the resistance Rc across R_A. This action reduces the charging time of capacitor C1 increases the output frequency, which is given by,

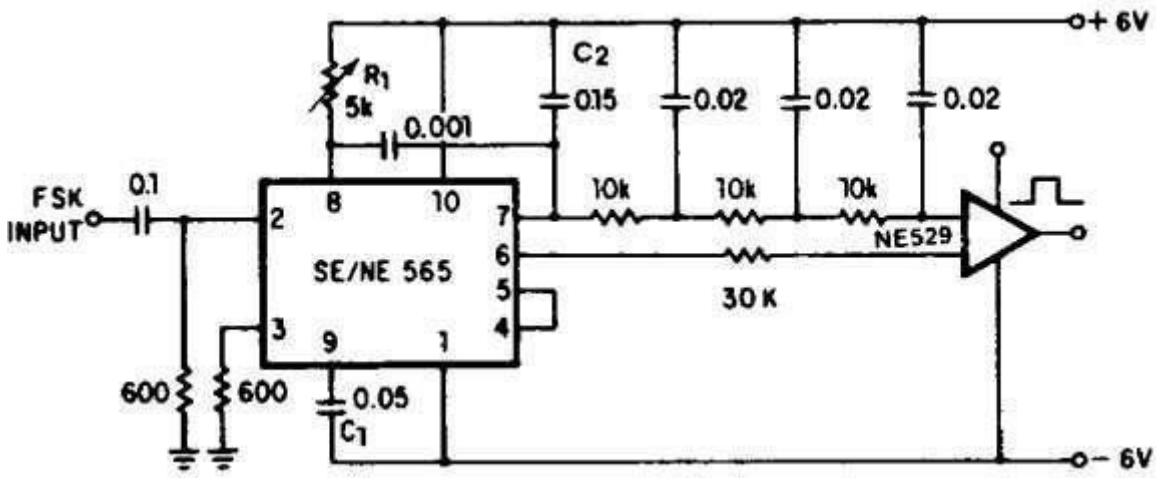
$$fo = \frac{1.45}{(R_A \,||\, R_C + 2 R_B)C} = 1270 \text{ Hz (space frequency)}$$

- By proper selection of resistance Rc, this frequency is adjusted to equal the space frequency of 1270 Hz. The difference between the FSK signals of 1070 Hz & 1270 Hz is 200 Hz, this difference is called -frequency shift.
- The output 150 Hz can be made by connecting a voltage comparator between the output of the ladder filter and pin 6 of PLL.
- The VCO frequency is adjusted with R1 so that at f_{IN} = 1070 Hz.

FSK Demodulator:

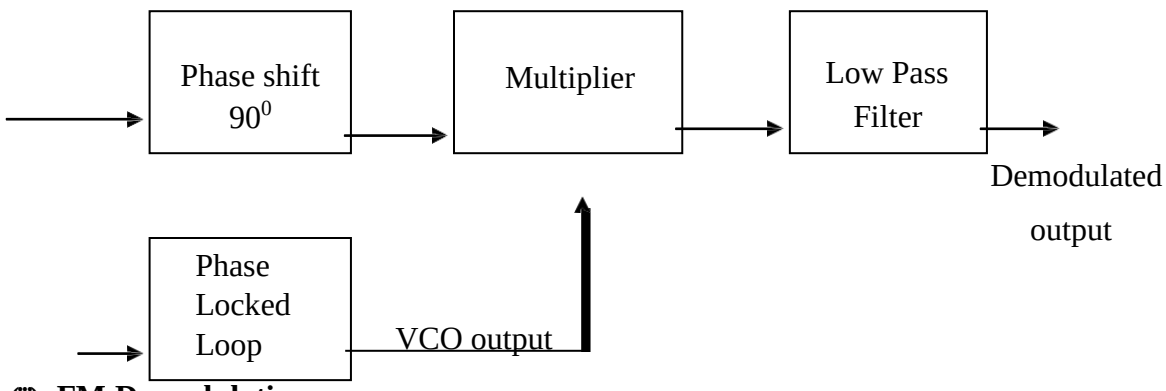
- The output of 555 FSK generator is applied to the 565 FSK demodulator.
- Capacitive coupling is used at the input to remove dc line.
- At the input of 565, the loop locks to the input frequency & tracks it between the 2 frequencies.
- R1 & C1 determine the free running frequency of the VCO, 3 stage RC ladder filter is used to remove the carrier component from the output.

In digital data communication and computer peripheral, binary data is transmitted by means of a carrier frequency which is shifted between two preset frequencies. This type of data transmission is called frequency shift keying (FSK) technique. The binary data can be retrieved using FSK demodulator. The figure below shows FSK demodulator using PLL for tele-typewriter signals of 1070 Hz and 1270 Hz. As the signal appears at the input, the loop locks to the input frequency and tracks it between the two frequencies with a corresponding dc shift at the output. A three stage filter removes the carrier component and the output signal is made logic compatible by a voltage comparator.



- AM Demodulation:

A PLL may be used to demodulate AM signals as shown in the figure below. The PLL is locked to the carrier frequency of the incoming AM signal. The output of VCO which has the same frequency as the carrier, but unmodulated is fed to the multiplier. Since VCO output is always 90^0 before being fed to the multiplier. This makes both the signals applied to the multiplier and the difference signals, the demodulated output is obtained after filtering high frequency components by the LPF. Since the PLL responds only to the carrier frequencies which are very close to the VCO output, a PLL AM detector exhibits high degree of selectivity and noise immunity which is not possible with conventional peak detector type AM modulators.



(iii) FM Demodulation:

If PLL is locked to a FM signal, the VCO tracks the instantaneous frequency of the input signal. The filtered error voltage which controls the VCO and maintains lock with the input signal is the demodulated FM output. The VCO transfer characteristics determine the linearity of the demodulated output. Since, VCO used in IC PLL is highly linear, it is possible to realize highly linear FM demodulators.

(iv) frequency multiplication/division:

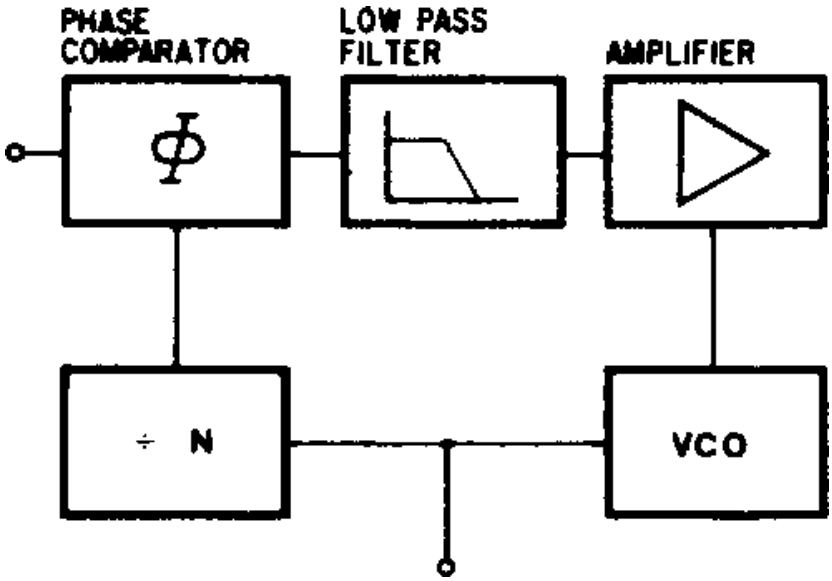
The block diagram shown below shows a frequency multiplier/divider using PLL. A divide by N network is inserter between the VCO output and the phase comparator input. In the locked state, the VCO output frequency f_o is given by

$f_o = Nf_s$. The multiplication factor can be obtained by selecting a proper scaling factor N of the counter.

Frequency multiplication can also be obtained by using PLL in its harmonic locking mode. If the input signal is rich in harmonics e.g. square wave, pulse train etc., then the VCO can be directly locked to the n-th harmonic of the input signal without connecting any frequency divider in between. However, as the amplitude of the higher order harmonics becomes less, effective locking may not take place for high values of n. Typically n is kept less than 10.

The circuit of the figure above can also be used for frequency division. Since the VCO output (a square wave) is rich in harmonics, it is possible to lock the m-th harmonic of the VCO output with the input signal f_s. The output fo of VCO is now given by

$f_o=f_s/m$

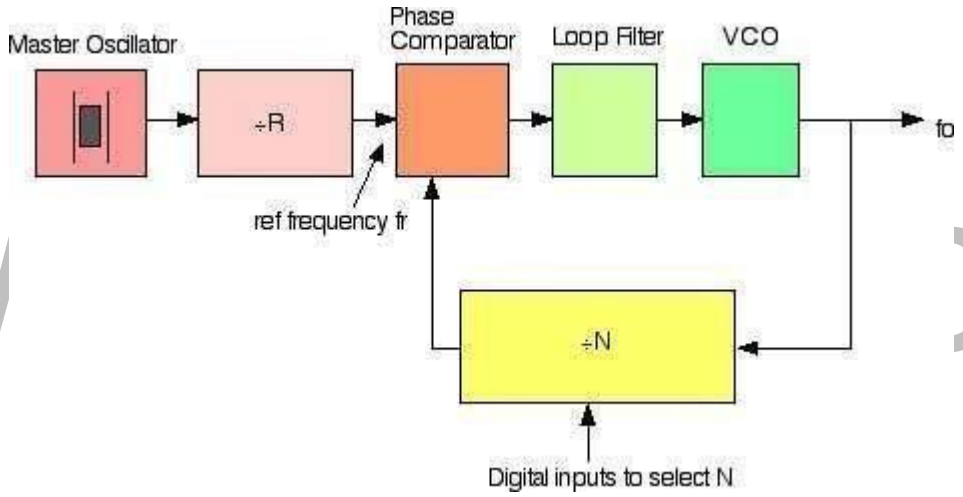


(v) PLL Frequency Synthesis:

In digital wireless communication systems (GSM, CDMA etc), PLL's are used to provide the Local Oscillator (LO) for up-conversion during transmission, and down-conversion during reception. In most cellular handsets this function has been largely integrated into a single integrated circuit to reduce the cost and size of the handset. However due to the high performance required of base station terminals, the transmission and reception circuits are built with discrete components to achieve the levels of performance required. GSM LO modules are typically built with a Frequency Synthesizer integrated circuit, and discrete resonator VCO's.

Frequency Synthesizer manufacturers include Analog Devices, National Semiconductor and Texas Instruments. VCO manufacturers include Sirenza, Z-Communications, Inc. (Z-COMM) Principle of PLLsynthesizers

A phase locked loop does for frequency what the Automatic Gain Control does for voltage. It compares the frequencies of two signals and produces an error signal which is proportional to the difference between the input frequencies. The error signal is then low pass filtered and used to drive a voltage-controlled oscillator (VCO) which creates an output frequency. The output frequency is fed through a frequency divider back to the input of the system, producing a negative feedback loop. If the output frequency drifts, the error signal will increase, driving the frequency in the opposite direction so as to reduce the error. Thus the output is *locked* to the frequency at the other input. This input is called the reference and is derived from a crystal oscillator, which is very stable in frequency. The block diagram below shows the basic elements and arrangement of a PLL based frequency synthesizer.



The key to the ability of a frequency synthesizer to generate multiple frequencies is the divider placed between the output and the feedback input. This is usually in the form of a digital counter, with the output signal acting as a clock signal. The counter is preset to some initial count value, and counts down at each cycle of the clock signal. When it reaches zero, the counter output changes state and the count value is reloaded. This circuit is straightforward to implement using flip- flops, and because it is digital in nature, is very easy to interface to other digital components or a microprocessor. This allows the frequency output by the synthesizer to be easily controlled by a digital system.

Example:

Suppose the reference signal is 100 kHz, and the divider can be preset to any value between 1 and 100. The error signal produced by the comparator will only be zero when the output of the divider is also 100 kHz. For this to be the case, the VCO must run at a frequency which is 100 kHz x the divider count value. Thus it will produce an output of 100 kHz for a count of 1, 200 kHz for a count of 2, 1 MHz for a count of 10 and so on. Note that only whole multiples of the reference frequency can be obtained with the simplest integer N dividers. Fractional N dividers are readily available

Practical considerations:

In practice this type of frequency synthesizer cannot operate over a very wide range of frequencies, because the comparator will have a limited bandwidth and may suffer from aliasing problems. This would lead to false locking situations, or an inability to lock at all. In addition, it is hard to make a high frequency VCO that operates over a very wide range. This is due to several factors, but the primary restriction is the limited capacitance range of varactor diodes. However, in most systems where a synthesiser is used, we are not after a huge range, but rather a finite number over some defined range, such as a number of radio channels in a specific band.

Many radio applications require frequencies that are higher than can be directly input to the digital counter. To overcome this, the entire counter could be constructed using high-speed logic such as ECL, or more commonly, using a fast initial division stage called a *prescaler* which reduces the frequency to a manageable level. Since the prescaler is part of the overall division ratio, a fixed prescaler can cause problems designing a system with narrow channel spacings - typically encountered in radio applications. This can be overcome using a dual- modulus prescaler.[11]

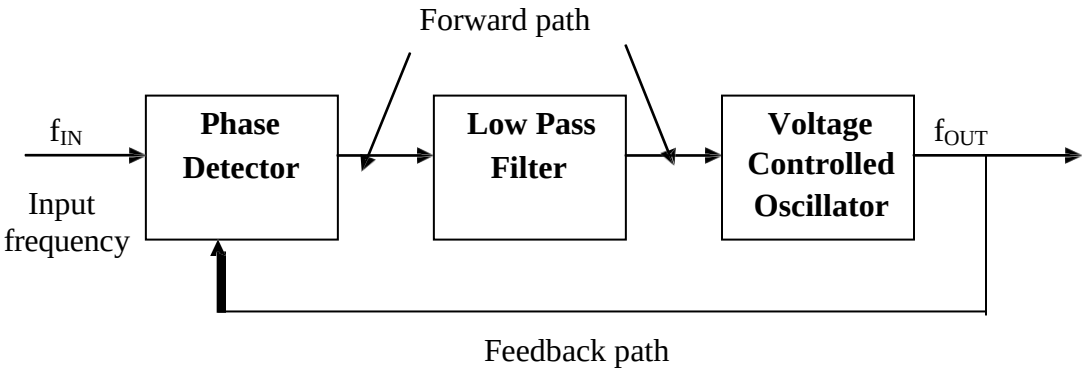
Further practical aspects concern the amount of time the system can switch from channel to channel, time to lock when first switched on, and how much noise there is in the output. All of these are a function of the *loop filter* of the system, which is a low-pass filter placed between the output of the frequency comparator and the input of the VCO. Usually the output of a frequency comparator is in the form of short error pulses, but the input of the VCO must be a smooth noise-

free DC voltage. (Any noise on this signal naturally causes frequency modulation of the VCO.).

Heavy filtering will make the VCO slow to respond to changes, causing drift and slow response time, but light filtering will produce noise and other problems with harmonics. Thus the design of the filter is critical to the performance of the system and in fact the main area that a designer will concentrate on when building a synthesizer system.

PHASE LOCKED LOOP:

Basic Block Diagram of a PLL



phase locked loop construction and operation:

- The PLL consists of i) Phase detector ii) LPF iii) VCO. The phase detector or comparator compares the input frequency f_{IN} with feedback frequency $f_{OUT.}$
- The output of the phase detector is proportional to the phase difference between f_{IN} & $f_{OUT.}$ The output of the phase detector is a dc voltage & therefore is often referred to as the error voltage.
- The output of the phase detector is then applied to the LPF, which removes the high frequency noise and produces a dc level. This dc level in turn, is input to the VCO.
- The output frequency of VCO is directly proportional to the dc level. The VCO frequency is compared with input frequency and adjusted until it is equal to the input frequencies.
- PLL goes through 3 states, i) free running ii) Capture iii) Phase lock.

Before the input is applied, the PLL is in free running state. Once the input frequency is applied the VCO frequency starts to change and PLL is said to be in the capture mode. The VCO frequency continuous to change until it equals the input frequency and the PLL is in phase lock mode. When Phase locked, the loop tracks any change in the input frequency through its repetitive action. If an input signal v_s of frequency f_s is applied to the PLL, the phase detector compares the phase and frequency of the incoming signal to that of the output v_o of the VCO. If the two signals differ in frequency of the incoming signal to that of the output v_o of the VCO. If the two signals differ in frequency and/or phase, an error voltage v_e is generated.

The phase detector is basically a multiplier and produces the sum (fs + fo) and difference (fs - fo) components at its output. The high frequency component (fs + fo) is removed by the low pass filter and the difference frequency component is amplified then applied as control voltage vc to VCO. The signal vc shifts the VCO frequency in a direction to reduce the frequency difference between fs and fo. Once this action starts, we say that the signal is in the capture range. The VCO continues to change frequency till its output frequency is exactly the same as the input signal frequency. The circuit is then said to be locked. Once locked, the output frequency fo of VCO is identical to fs except for a finite phase difference φ. This phase difference φ generates a corrective control voltage vc to shift the VCO frequency from f0 to fs and thereby maintain the lock. Once locked, PLL tracks the frequency changes of the input signal. Thus, a PLL goes through three stages (i) free running, (ii) capture and (iii) locked or tracking.

Capture range: the range of frequencies over which the PLL can acquire lock with an input signal is called the capture range. This parameter is also expressed as percentage of fo.

Pull- in time: the total time taken by the PLL to establish lock is called pull- in time. This depends on the initial phase and frequency difference between the two signals as well as on the overall loop gain and loop filter characteristics.

Phase Detector:

Phase detector compares the input frequency and VCO frequency and generates DC voltage i.e., proportional to the phase difference between the two frequencies. Depending on whether the analog/digital phase detector is used, the PLL is called either an analog/digital type respectively. Even though most monolithic PLL integrated circuits use analog phase detectors.

Ex for Analog: Double-balanced mixer

Ex for Digital: Ex-OR, Edge trigger, monolithic Phase detector.

Ex-OR Phase Detector:

This uses an exclusive OR gate. The output of the Ex-OR gate is high only when fIN or fOUT is high.The DC output voltage of the Ex-OR phase detector is a function of the phase difference between its two outputs. The maximum dc output voltage occurs when the phase difference is Π radians 180 degrees. The slope of the curve between 0 or Π radians is the conversion gain kp of the phase detector for eg; if the Ex-OR gate uses a supply voltage Vcc = 5V, the conversion gain Kp is

KP = 5V= 1.59V / RAD

Edge Triggered Phase Detector:

Advantages of Edge Triggered Phase Detector over Ex-OR are

The dc output voltage is linear over 2Π radians or 360 degrees, but in Ex-OR it is Π radians or 180 degrees.

Better Capture, tracking & locking characteristics.

Edge triggered type of phase detector using RS Flip – Flop. It is formed from a pair of cross coupled NOR gates.

RS FF is triggered, i.e, the output of the detector changes its logic state on the positive edge of the inputs fIN & fOUT

Monolithic Phase detector:

It consists of 2 digital phase detector, a charge pump and an amplifier.

Phase detector 1 is used in applications that require zero frequency and phase difference at lock.

Phase detector 2, if quadrature lock is desired, when detector 1 is used in the main loop, detector can also be used to indicate whether the main loop is in lock or out of lock. R Reference

V Variable or 0feedback input PU Pump Up signal
PD Pump Down signal
UF Up frequency output

DF – Down frequency output

Low – Pass filter:

The function of the LPF is to remove the high frequency components in the output of the phase detector and to remove the high frequency noise. LPF controls the characteristics of the phase locked loop. i.e, capture range, lock ranges, bandwidth

Lock range(Tracking range):

The lock range is defined as the range of frequencies over which the PLL system follows the changes in the input frequency fIN.

Capture range:

Capture range is the frequency range in which the PLL acquires phase lock. Capture range is always smaller than the lock range.

Filter Bandwidth:

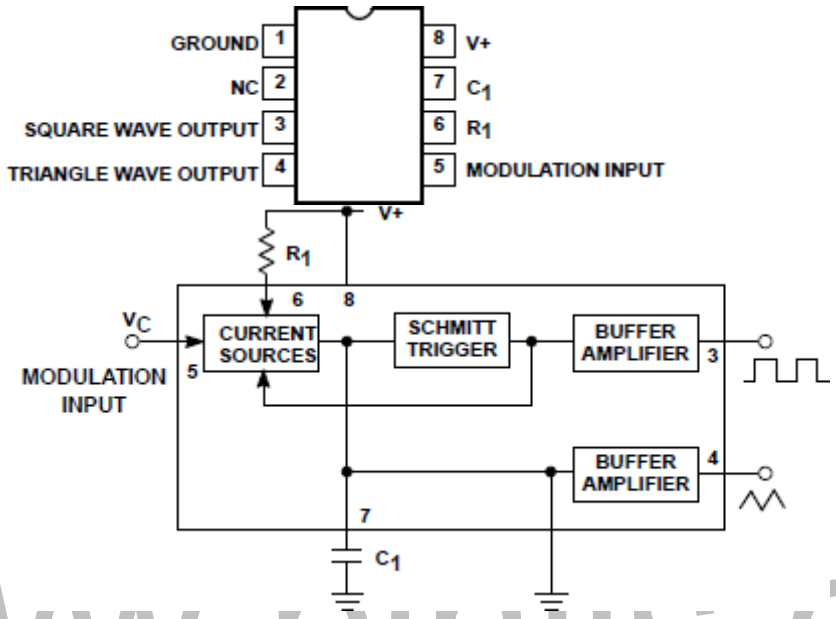
Filter Bandwidth is reduced, its response time increases. However reduced Bandwidth reduces the capture range of the PLL. Reduced Bandwidth helps to keep the loop in lock through momentary losses of signal and also minimizes noise.

(a) Voltage Controlled Oscillator (VCO):

The third section of PLL is the VCO; it generates an output frequency that is directly proportional to its input voltage. The maximum output frequency of NE/SE 566 is 500 Khz.

VOLTAGE CONTROLLED OSCILLATOR:

A common type of VCO available in IC form is Signetics NE/SE566. The pin configuration and basic block diagram of 566 VCO are shown in figures below.



Referring to the circuit in the above figure, the capacitor c_1 is linearly charged or discharged by a constant current source/sink. The amount of current can be controlled by changing the voltage v_c applied at the modulating input (pin 5) or by changing the timing resistor R_1 external to the IC chip. The voltage at pin 6 is held at the same voltage as pin 5. Thus, if the modulating voltage atpin 5 is increased, the voltage at pin 6 also increases, resulting in less voltage across R_1 and thereby decreasing the charging current.

The voltage across the capacitor C_1 is applied to the inverting input terminal of Schmitt trigger via buffer amplifier. The output voltage swing of the Schmitt trigger is designed to V_{cc} and V_{cc}. If $R_a = R_b$ in the positive feedback loop, the voltage at the non- inverting input terminal of Schmitt trigger swings from 0.5 V_{cc} to 0.25 V_{cc}. When the voltage on the capacitor c_1 exceeds 0.5 V_{cc} during charging, the output of the Schmitt trigger goes LOW (0.5 V_{cc}). The capacitor now discharges and when it is at 0.25 V_{cc}, the output of Schmitt trigger goes HIGH (V_{cc}). Since the source and sink currents are equal, capacitor charges and discharges for the same amount of time. This gives a triangular voltage waveform across c_1 which is also available at pin 4. The square wave output of the

Schmitt trigger is inverted by buffer amplifier at pin 3. The output waveforms are shown near the pins 4 and 3.

The output frequency of the VCO can be given as follows:

$$f_o = \frac{2\,[(V+) - (V_C)]}{R_1\,C_1\,V+}$$

where V+ is V_{cc}.

The output frequency of the VCO can be changed either by (i) R_1, (ii) c_1 or (iii) the voltage v_c at the modulating input terminal pin 5. The voltage v_c can be varied by connecting a R_1R_2circuit as shown in the figure below. The components $R_1$and c_1 are first selected so that VCO output frequency lies in the centre of the operating frequency range. Now the modulating input voltage is usually varied from 0.75 V_{cc} to V_{cc} which can produce a frequency variation of about 10 to 1.