HIGH SPEED SAMPLE AND HOLD CIRCUITS

Introduction:

Sample-and- hold (S/H) is an important analog building block with many applications, ncluding analog-to-digital converters (ADCs) and switched-capacitor filters. The function of the S/H circuit is to sample an analog input signal and hold this value over a certain length of time for subsequent processing.

Taking advantages of the excellent properties of MOS capacitors and switches, traditional switched capacitor techniques can be used to realize different S/H circuits [1]. The simplest S/H circuit in MOS technology is shown in Figure 1, where Vin is the input signal, M1 is an MOS transistor operating as the sampling switch, Ch is the hold capacitor, ck is the clock signal, and Vout is the resulting sample-and-hold output signal.Ch

As depicted by Figure 1, in the simplest sense, a S/H circuit can be achieved using only one MOS transistor and one capacitor. The operation of this circuit is very straightforward. Whenever

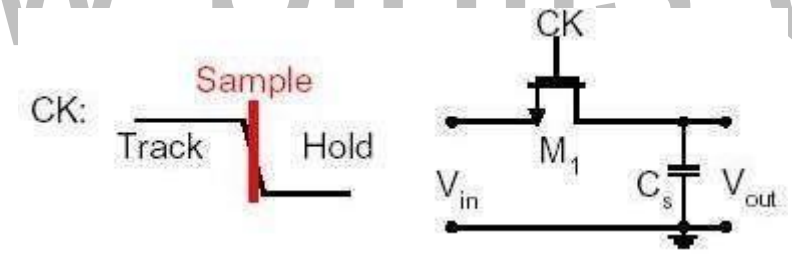


Figure 1: Simplest sample-and-hold circuit in MOS technology.

As depicted by Figure 1, in the simplest sense, a S/H circuit can be achieved using only one MOS transistor and one capacitor. The operation of this circuit is very straightforward. Whenever ck is high, the MOS switch is on, which in turn allows Vout to track Vin. On the other hand, when ck is low, the MOS switch is off. During this time, Ch will keep Vout equal to the value of Vin at the instance when ck goes low.

Unfortunately, in reality, the performance of this S/H circuit is not as ideal as descr ibed

above. The two major types of errors occur. They are charge injection and clock feed through, that are associated with this S/H implementation. Three new S/H techniques, all of which try to minimize the errors caused by charge injection and/or clock feed through.

Alternative CMOS Sample-and-Hold Circuits:

This section covers three alternative CMOS S/H circuits that are developed with the intention to minimize charge injection and/or clock feedthrough.

Series Sampling:

The S/H circuit of Figure 1 is classified as parallel sampling because the hold capacitor is in parallel with the signal. In parallel sampling, the input and the output are dc-coupled.

On the other hand, the S/H circuit shown in Figure 2 is referred to as series sampling because the hold capacitor is in series with the signal.

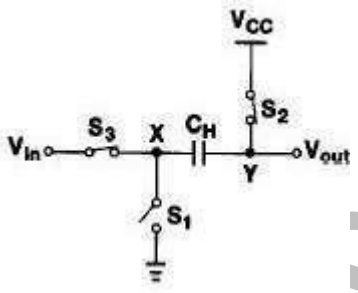


Figure 2: Series sampling.

When the circuit is in sample mode, both switches *S2* and *S3* are on, while *S1* is off. Then,*S2* is turned off first, which means *Vout* is equal to *VCC* (or *VDD* for most circuits) and the voltage drop across *Ch* will be *VCC – Vin*. Subsequently, *S3* is turned off and *S1* is turned on simultaneously. By grounding node *X*, *Vout* is now equal to *VCC – Vin*, and the drop from *VCC* to *VCC – Vin* is equal to the instantaneous value of the input.

As a result, this is actually an inverted S/H circuit, which requires inversion of the signal at a later stage. Since the hold capacitor is in series with the signal, series sampling can isolate the common-mode levels of the input and the output. This is one advantage of series sampling over parallel sampling. In addition, unlike parallel sampling, which suffers from signal-dependent charge injection, series sampling does not exhibit such behavior because *S2* is turned off before *S3*. Thus, the fact that the gate-to-source voltage, *VGS*, of *S2* is constant means that charge injection coming from *S2* is also constant (as opposed to being signal-dependent), which means this error can be easily eliminated through differential operation.

On the other hand, series sampling suffers from the nonlinearity of the parasitic capacitance at node *Y*. This parasitic capacitance introduces distortion to the sample-and hold value, thus mandating that *Ch* be much larger than the parasitic capacitance. On top of this disadvantage, the settling time of the S/H circuit during hold mode is longer for series sampling than for parallel sampling. The reason for this is because the value of *Vout* in series sampling is being reset to *VCC* (or *VDD*) for every sample, but this is not the casefor parallel sampling.

Switched Op-Amp Based Sample-and-Hold Circuit:

This S/H technique takes advantage of the fact that when a MOS transistor is in the saturation region, the channel is pinched off and disconnected from the drain. Therefore, if the hold capacitor is connected to the drain of the MOS transistor, charge injection will only go to the source junction, leaving the drain unaffected. Based on this concept, a switched op-amp (SOP) based S/H circuit, as shown in Figure 3.

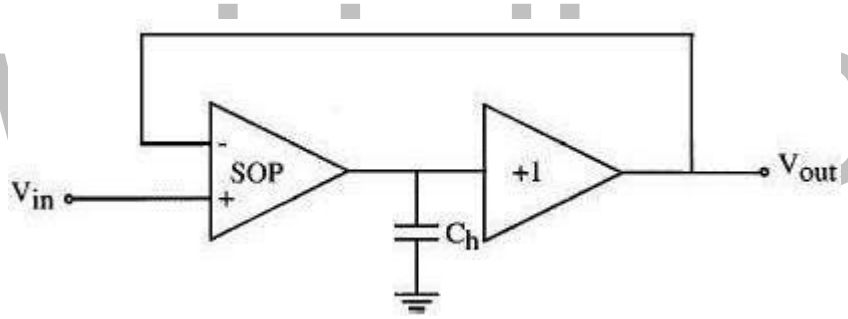


Figure 3: Switched op-amp based sample and hold circuit.

During sample mode, the SOP behaves just like a regular op-amp, in which the value of the output follows the value of the input. During hold mode, the MOS transistors at the output node of the SOP are turned off while they are still operating in saturation, thus preventing any channel charge from flowing into the output of the SOP. In addition, the SOP is shut off and its output is held at high impedance, allowing the charge on Ch to be preserved throughout the hold mode. On the other hand, the output buffer of this S/H circuit is always operational during sample and hold mode and is always providing the voltage on Ch to the output of the S/H circuit.

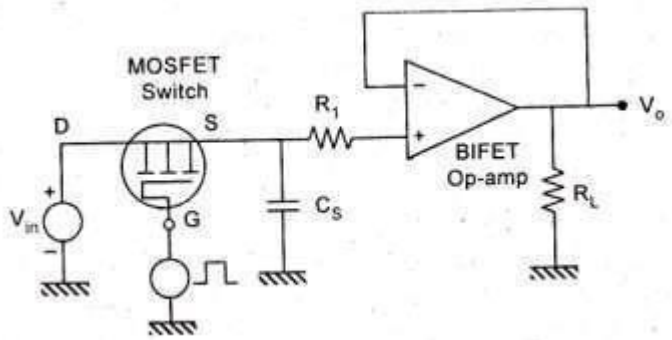
With the increasing demand for high-resolution and high-speed in date acquisition systems, the performance of the S/H circuits is becoming more and more important. This is especially true in ADCs since the performance of S/H circuits greatly affects the speed and accuracy of ADCs. The fastest S/H circuits operate in open loop, but when such circuits are implemented in CMOS technology, their accuracy is low. S/H circuits

that operate in closed loop configuration can achieve high resolution, but their requirements for high gain circuit block, such as an op-amp, limits the speed of the circuits. As a result, better and faster S/H circuits must be developed.

At the same time, the employment of low-voltage in VLSI technology requires that the analog circuits be low-voltage as well. As a result of this, new researches in analog

circuits are now shifted from voltage- mode to current-mode. The advantages of current mode circuits include low- voltage, low-power, and high-speed. Therefore, future

researches of S/H circuit should also shift toward current-mode S/H techniques.

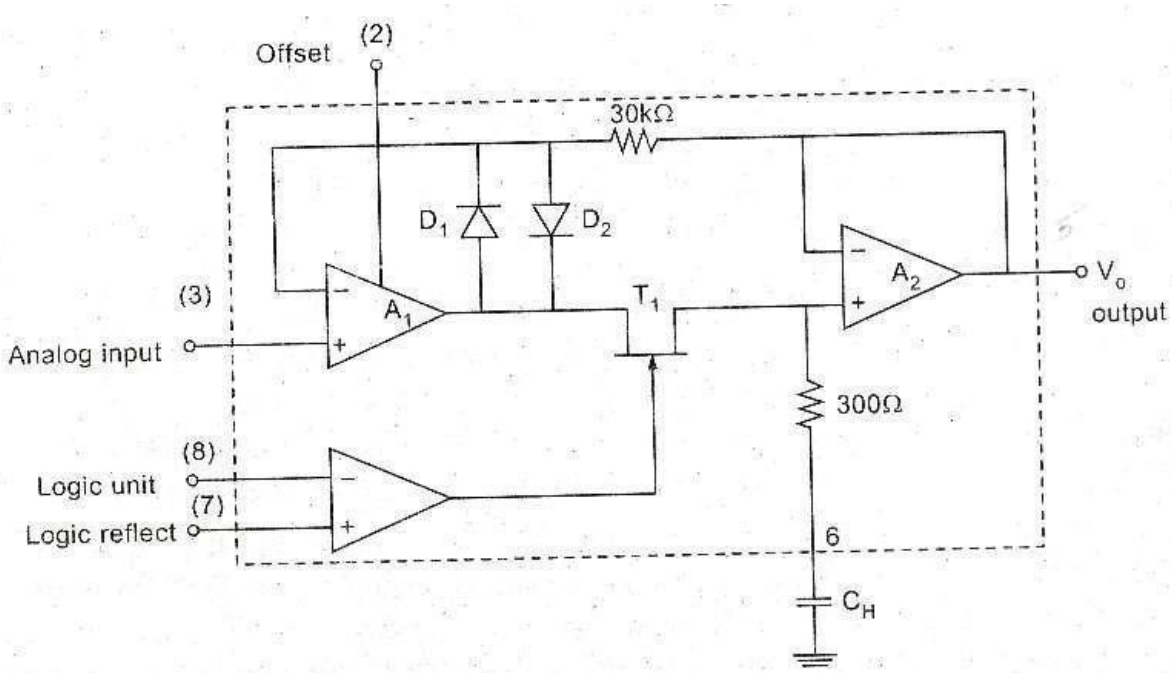


The above figure shows a sample and hold circuit with MOSFET as Switch acting as a sampling device and also consists of a holding capacitor Cs to store the sample values until the next sample comes in. This is a high speed circuit as it is apparent that CMOS switch has a very negligible propagation delay.

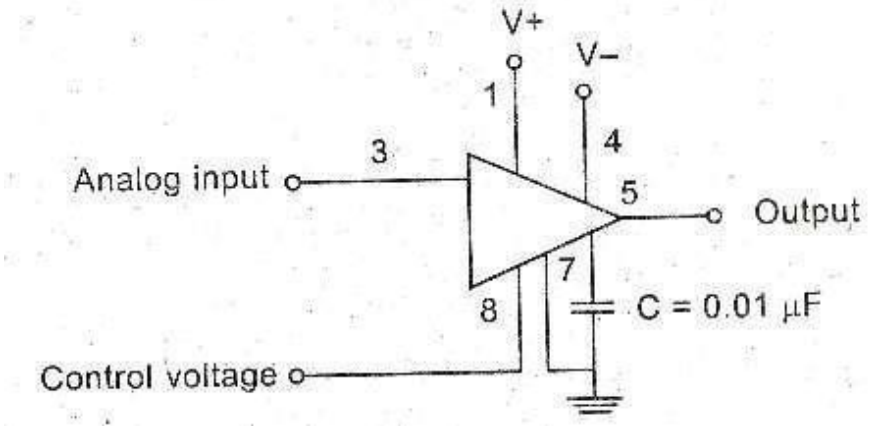
Sample-and- hold (S/H) is an important analog building block that has many applications. The simplest S/H circuit can be constructed using only one MOS transistor and one hold capacitor.

However, due to the limitations of the MOS transistor switches, errors due to charge injection and clock feed through restrict the performance of S/H circuits. As a result, different S/H techniques and architectures are developed with the intention to reduce or eliminate these errors. Three of these alternative S/H circuits: series sampling, SOP based S/H circuit, and bottom plate S/H circuit with bootstrapped switch, more new S/H techniques and architectures need to be proposed in order to meet the increasing demand for high-speed, low-power, and low voltage S/H circuits for data acquisition systems.

LF 398 IC- Functional Diagram



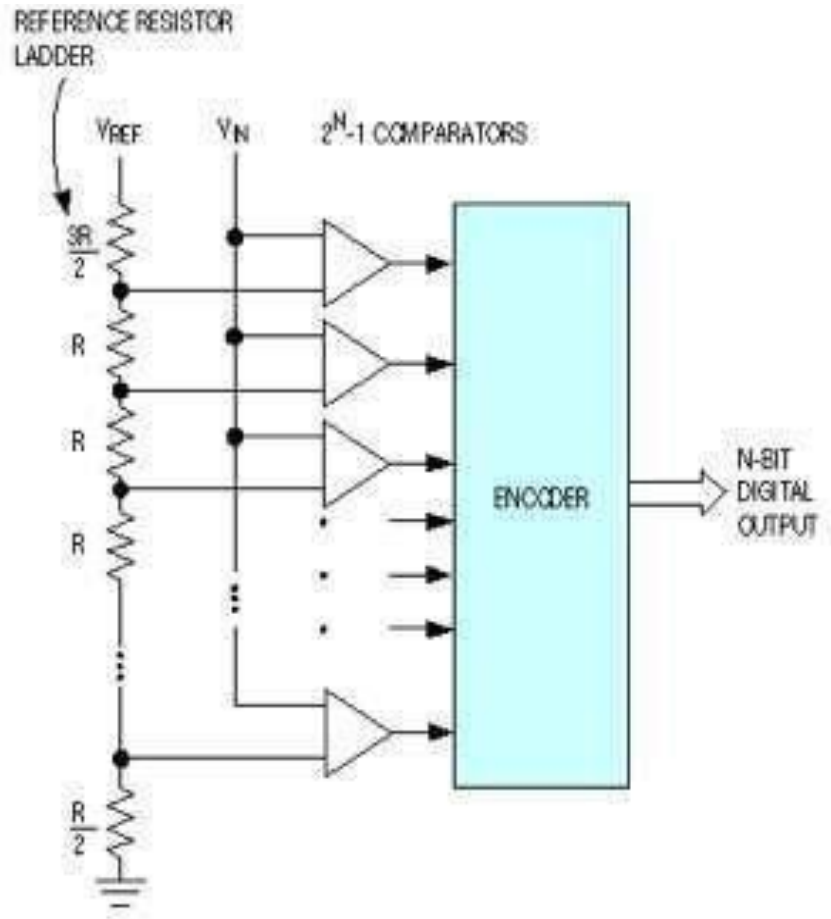
Connection Diagram



Types of ADC

Direct-conversion ADC/Flash type ADC:

This process is extremely fast with a sampling rate of up to 1 GHz. The resolution is however, limited because of the large number of comparators and reference voltages required. The input signal is fed simultaneously to all comparators. A priority encoder then generates a digital output that corresponds with the highest activated comparator.

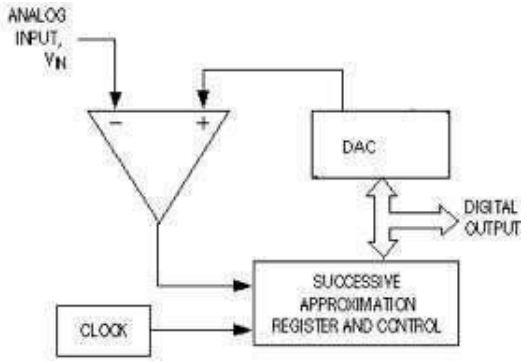


Successive-approximationADCs

Successive-approximation ADC is a conversion technique based on a successive-approximation register (SAR). This is also called bit-weighing conversion that employs a comparator to weigh the applied input voltage against the output of an N-bit digital-to-analog converter (DAC). The final result is obtained as a sum of N weighting steps, in which each step is a single-bit conversion using the DAC output as a reference. SAR converters sample at rates up to 1Mbps, requires a low supply current, and the cheapest in terms of production cost.

A successive-approximation ADC uses a comparator to reject ranges of voltages, eventually settling on a final voltage range. Successive approximation works by constantly comparing the input voltage to the output of an internal digital to analog converter (DAC, fed by the current value of the approximation) until the best approximation is achieved. At each step in this process, a binary value of the approximation is stored in a successive approximation register (SAR). The SAR uses a reference voltage (which is the largest signal the ADC is to convert) for comparisons. For example if the input voltage is 60 V and the reference voltage is 100 V, in the 1st clock cycle, 60 V is compared to 50 V (the reference, divided by two. This is the voltage at the output of the internal DAC when the input is a '1' followed by zeros), and the voltage from the comparator is positive (or '1') (because 60 V is greater than 50 V). At this point the first binary digit (MSB) is set to a '1'. In the 2nd clock cycle the input voltage is compared to 75 V (being halfway between 100 and 50 V: This is the output of the internal DAC when its input is '11' followed by zeros) because 60 V is less than 75 V, the comparator output is now negative (or '0'). The second binary digit is therefore set to a '0'. In the 3rd clock cycle, the input voltage is compared with 62.5 V (halfway between 50 V and 75 V: This is the output of the internal DAC when its input is '101' followed by zeros). The output of the comparator is negative or '0' (because 60 V is less than 62.5 V) so the third binary digit is set to a 0. The fourth clock cycle similarly results in the fourth digit being a '1' (60 V is greater than 56.25 V, the DAC output for '1001' followed by zeros). The result of this would be in the binary form 1001. This is also called *bit-weighting conversion*, and is similar to a binary. The analogue value is rounded to the nearest binary value below, meaning this converter type is mid-rise (see above). Because the approximations are successive (not simultaneous), the conversion takes one clock-cycle for each bit of resolution desired. The clock frequency must be equal to the sampling frequency multiplied by the number of bits of resolution desired. For example, to sample audio at 44.1 kHz with 32 bit resolution, a clock frequency of over 1.4 MHz

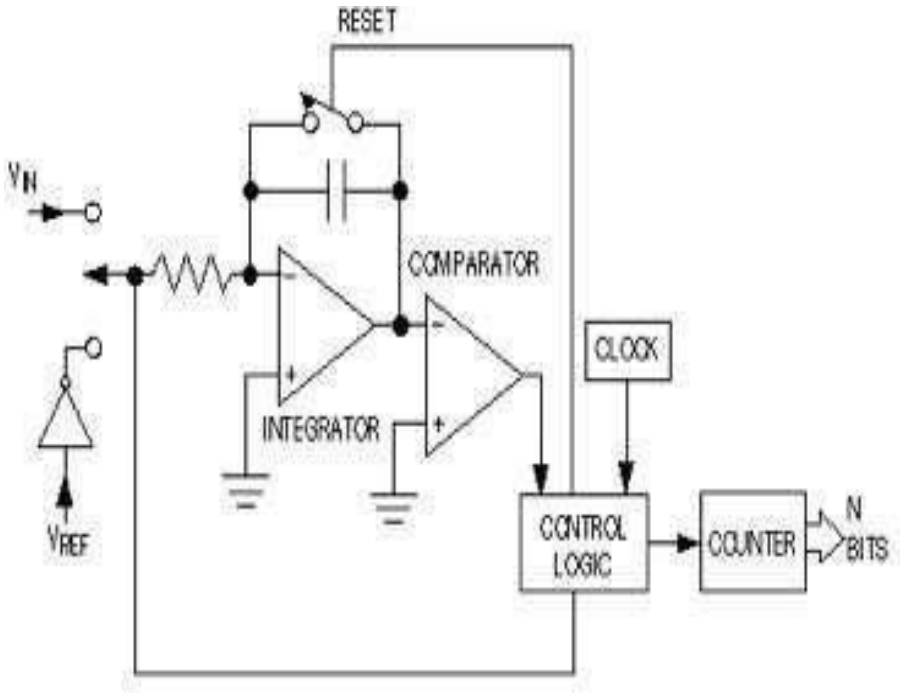
would be required. ADCs of this type have good resolutions and quite wide ranges. They are more complex than some other designs.



IntegratingADCs

In an integrating ADC, a current, proportional to the input voltage, charges a capacitor for a fixed time interval T charge. At the end of this interval, the device resets its counter and applies an opposite-polarity negative reference voltage to the integrator input. Because of this, the capacitor is discharged by a constant current until the integrator output voltage zero again. The T discharge interval is proportional to the input voltage level and the resultant final count provides the digital output, corresponding to the input signal. This type of ADCs is extremely slow devices with low input bandwidths. Their advantage, however, is their ability to reject high- frequency noise and AC line noise such as 50Hz or 60Hz. This makes them useful in noisy industrial environments and typical application is in multi-meters.

An integrating ADC (also dual-slope or multi-slope ADC) applies the unknown input voltage to the input of an integrator and allows the voltage to ramp for a fixed time period (the run- up period). Then a known reference voltage of opposite polarity is applied to the integrator and is allowed to ramp until the integrator output returns to zero (the run-down period). The input voltage is computed as a function of the reference voltage, the constant run- up time period, and the measured run-down time period. The run-down time measurement is usually made in units of the converter's clock, so longer integration times allow for higher resolutions. Likewise, the speed of the converter can be improved by sacrificing resolution. Converters of this type (or variations on the concept) are used in most digital voltmeters for their linearity and flexibility.



Sigma-delta ADCs/ Over sampling Converters:

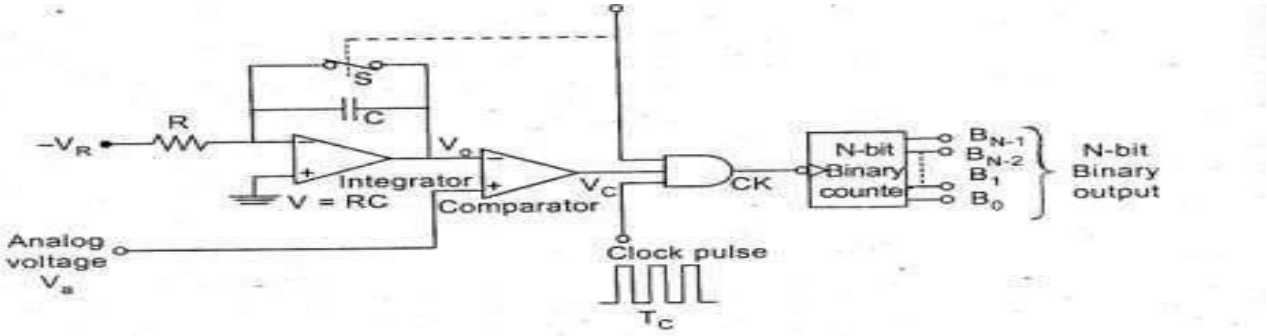
It consist of 2 main parts - modulator and digital filter. The modulator includes an integrator and a comparator with a feedback loop that contains a 1-bit DAC. The modulator oversamples the input signal, converting it to a serial bit stream with a frequency much higher than the required sampling rate. This is then transform by the output filter to a sequence of parallel digital words at the sampling rate. The characteristics of sigma-delta converters are high resolution, high accuracy, low noise and low cost. Typical applications are for speech and audio.

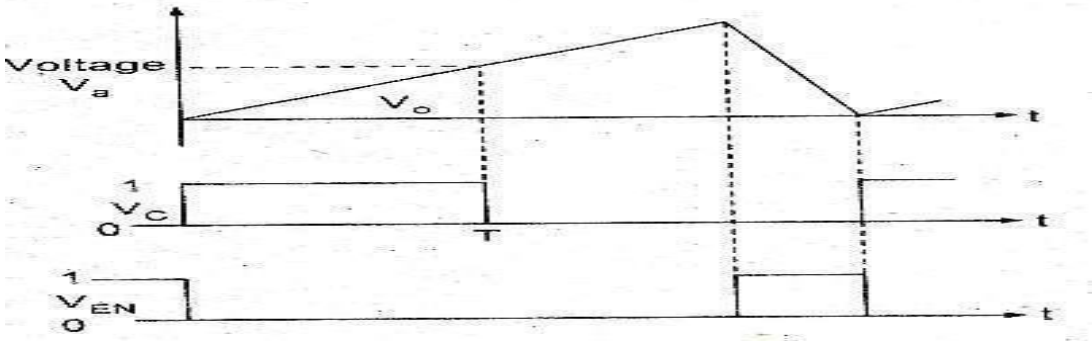
A **Sigma-Delta ADC** (also known as a Delta-Sigma ADC) oversamples the desired signal by a large factor and filters the desired signal band. Generally a smaller number of bits than required are converted using a Flash ADC after the Filter. The resulting signal, along with the error generated by the discrete levels of the Flash, is fed back and subtracted from the input to the filter. This negative feedback has the effect of noise shaping the error due to the Flash so that it does not appear in the desired signal frequencies. A digital filter (decimation filter) follows the ADC which reduces the sampling rate, filters off unwanted noise signal and increases the resolution of the output. (sigma-delta modulation, also called delta-sigma modulation)

A/D Using Voltage to time conversion:

The Block diagram shows the basic voltage to time conversion type of A to D converter. Here the cycles of variable frequency source are counted for a fixed period. It is possible to make an A/D converter by counting the cycles of a fixed- frequency source for a variable period. For this, the analog voltage required to be converted to a proportional time period.

As shown in the diagram, A negative reference voltage -VR is applied to an integrator, whose output is connected to the inverting input of the comparator. The output of the comparator is at 1 as long as the output of the integrator Vo is less than Va. At t = T, Vc goes low and switch S remains open. When VEN goes high, the switch S is closed, thereby discharging the capacitor. Also the NAND gate is disabled. The waveforms are shown here.





ANALOG TO DIGITAL & DIGITAL TO ANALOG CONVERTERS

D TO A CONVERTER- SPECIFICATIONS

D/A converters are available with wide range of specifications specified by manufacturer. Some of the important specifications are Resolution, Accuracy, linearity, monotonicity, conversion time, settling time and stability.

Resolution:

Resolution is defined as the number of different analog output voltage levels that can be provided by a DAC. Or alternatively resolution is defined as the ratio of a change in output voltage resulting for a change of 1 LSB at the digital input. Simply, resolution is the value of LSB.

Resolution (Volts) = $Vo_{FS} / (2^n - 1)$ = 1 LSB increment

Where _n' is the number of input bits

_Vo_{FS}' is the full scale output voltage.

Example:

Resolution for an 8 – bit DAC for example is said to have

: 8 – bit resolution

: A resolution of 0.392 of full-Scale (1/255)

: A resolution of 1 part in 255.

Thus resolution can be defined in many different ways.

The following table shows the resolution for 6 to 16 bit DACs

S.No.	Bits	Intervals	LSB size (% of full-scale)	LSB size (For a 10 V full-scale)
1.	6	63	1.588	158.8 mV
2.	8	255	0.392	39.2 mV
3.	10	1023	0.0978	9.78 mV
4.	12	4095	0.0244	2.44 mV
5.	14	16383	0.0061	0.61 mV
6.	16	65535	0.0015	0.15 mV

Accuracy:

Absolute accuracy is the maximum deviation between the actual converter output and the ideal converter output. The ideal converter is the one which does not suffer from any problem. Whereas, the actual converter output deviates due to the drift in component values, mismatches, aging, noise and other sources of errors.

The relative accuracy is the maximum deviation after the gain and offset erro rs have been removed. Accuracy is also given in terms of LSB increments or percentage of full-scale voltage. Normally, the data sheet of a D/A converter specifies the relative accuracy rather than absolute accuracy.

Linearity:

Linearity error is the maximum deviation in step size from the ideal step size. Some D/A converters are having a linearity error as low as 0.001% of full scale. The linearity of a D/A converter is defined as the precision or exactness with which the digital input is converted into analog output. An ideal D/A converter produces equal increments or step sizes at output for every change in equal increments of binary input.

Monotonicity:

A Digital to Analog converter is said to be monotonic if the analog output increases for an increase in the digital input. A monotonic characteristics is essential in control applications. Otherwise it would lead to oscillations. If a DAC has to be monotonic, the error should be less than ± (1/2) LSB at each output level. Hence all the D/A converters are designed such that the linearity error satisfies the above condition.

When a D/A Converter doesn‘t satisfy the condition described above, then, the output voltage may decrease for an increase in the binary input.

Conversion Time:

It is the time taken for the D/A converter to produce the analog output for the given binary input signal. It depends on the response time of switches and the output of the
Amplifier. D/A converters speed can be defined by this parameter. It is also called as setting time.

Settling time:

It is one of the important dynamic parameter. It represents the time it takes for the output to settle within a specified band ± (1/2) LSB of its final value following a code change at the input (Usually a full-scale change). It depends on the switching time of the logic circuitry due to internal parasitic capacitances and inductances. A typical settling time ranges from 100 ns to 10 μs depending on the word length and type of circuit used.

Stability:

The ability of a DAC to produce a stable output all the time is called as Stability. The performance of a converter changes with drift in temperature, aging and power supply variations. So all the parameters such as offset, gain, linearity error & monotonicity may change from the values specified in the datasheet. Temperature sensitivity defines the stability of a D/A converter.

DIGITAL TO ANALOG CONVERSION

A DAC converts an abstract finite-precision number (usually a fixed-point binary number) into a concrete physical quantity (e.g., a voltage or a pressure). In particular, DACs are often used to convert finite-precision time series data to a continually-varying physical signal.

A typical DAC converts the abstract numbers into a concrete sequence of impulses that are then processed by a reconstruction filter using some form of interpolation to fill in data between the impulses. Other DAC methods (e.g., methods based on Delta-sigma modulation) produce a pulse-density modulated signal that can then be filtered in a similar way to produce a smoothly-varying signal.

By the Nyquist–Shannon sampling theorem, sampled data can be reconstructed perfectly provided that its bandwidth meets certain requirements (e.g., a baseband signal with bandwidth less than the Nyquist frequency). However, even with an ideal reconstruction filter, digital sampling introduces quantization that makes perfect reconstruction practically impossible. Increasing the digital resolution (i.e., increasing the number of bits used in each sample) or introducing sampling dither can reduce this error.

DACs are at the beginning of the analog signal chain, which makes them very important to system performance. The most important characteristics of these devices are:

Resolution: This is the number of possible output levels the DAC is designed to reproduce. This is usually stated as the number of bits it uses, which is the base two logarithm of the number of levels. For instance a 1 bit DAC is designed to reproduce 2 (2^1) levels while an 8 bit DAC is designed for 256 (2^8) levels. Resolution is related to the **effective number of bits**(ENOB) which is a measurement of the actual resolution attained by the DAC.

Maximum sampling frequency: This is a measurement of the maximum speed at which the DACs circuitry can operate and still produce the correct output. As stated in the Nyquist–Shannon sampling theorem, a signal must be sampled at over twice the frequency of the desired signal. For instance, to reproduce signals in all the audible spectrum, which includes frequencies of up to 20 kHz, it is necessary to use DACs that operate at over 40 kHz. The CD standard samples audio at 44.1 kHz, thus DACs of this frequency are often used. A common frequency in cheap computer sound cards is 48 kHz—many work at only this frequency, offering the use of other

sample rates only through (often poor) internal resampling.

Monotonicity: This refers to the ability of a DAC's analog output to move only in the direction that the digital input moves (i.e., if the input increases, the output doesn't dip before asserting the correct output.) This characteristic is very important for DACs used as a low frequency signal source or as a digitally programmable trim element.

THD+N : This is a measurement of the distortion and noise introduced to the signal by the DAC. It is expressed as a percentage of the total power of unwanted harmonic distortion and noise that accompany the desired signal. This is a very important DAC characteristic for dynamic and small signal DAC applications.

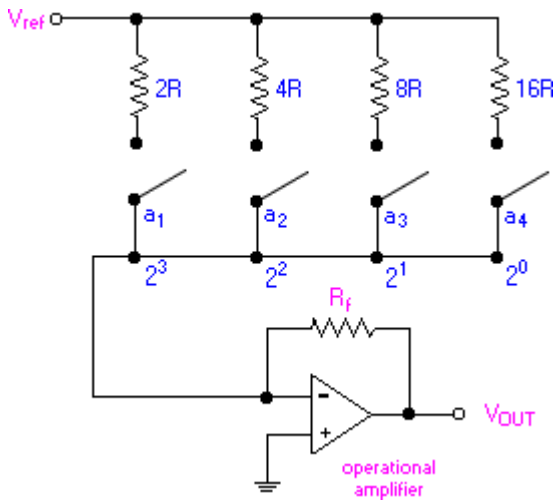
Dynamic range : This is a measurement of the difference between the largest and smallest signals the DAC can reproduce expressed in decibels. This is usually related to DAC resolution and noise floor.

Other measurements, such as phase distortion and sampling period instability, can also be very important for some applications.

BINARY-WEIGHTED RESISTOR DAC

The binary-weighted-resistor DAC employs the characteristics of the inverting summer Op Amp circuit. In this type of DAC, the output voltage is the inverted sum of all the input voltages. If the input resistor values are set to multiples of two: 1R, 2R and 4R, the output voltage would be equal to the sum of V1, V2/2 and V3/4. V1 corresponds to the most significant bit (MSB) while V3 corresponds to the least significant bit (LSB).

The circuit for a 4-bit DAC using binary weighted resistor network is shown below:



The binary inputs, a_i (where i = 1, 2, 3 and 4) have values of either 0 or 1. The value, 0, represents an open switch while 1 represents a closed switch.

The operational amplifier is used as a summing amplifier, which gives a weighted sum of the binary input based on the voltage, V_{ref}.

For a 4-bit DAC, the relationship between V_{out} and the binary input is as follows:

$$
\begin{aligned}
V_{OUT} &= -iR_f \\
&= -\left[V_{ref}\left(\frac{a_1}{2R}+\frac{a_2}{4R}+\frac{a_3}{8R}+\frac{a_4}{16R}\right)\right]R_f \\
&= -\frac{V_{ref}R_f}{R}\left(\frac{a_1}{2}+\frac{a_2}{4}+\frac{a_3}{8}+\frac{a_4}{16}\right) \\
&= -\frac{V_{ref}R_f}{R}\left(\frac{a_1}{2^1}+\frac{a_2}{2^2}+\frac{a_3}{2^3}+\frac{a_4}{2^4}\right)
\end{aligned}
$$

The negative sign associated with the analog output is due to the connection to a summing amplifier, which is a polarity- inverting amplifier. When a signal is applied to the latter type of amplifier, the polarity of the signal is reversed (i.e. a + input becomes -, or vice versa).

For a n-bit DAC, the relationship between V_{out} and the binary input is as follows:

$$V_{OUT} = -\frac{V_{ref} R_f}{R} \sum_{i=1}^{n} \frac{a_i}{2^i}$$

Analog Voltage Output: An Example

As an example, consider the following given parameters: $V_{ref} = 5$ V, R = 0.5 k and $R_f = 1$ k. The voltage outputs, V_{out}, corresponding to the respective binary inputs are as follows:

Digital Input				V_{OUT} (Volts)
a_1	a_2	a_3	a_4	
0	0	0	0	**0**
0	0	0	1	**- 0.625**
0	0	1	0	**- 1.250**
0	0	1	1	**- 1.875**
0	1	0	0	**- 2.500**
0	1	0	1	**- 3.125**
0	1	1	0	**- 3.750**
0	1	1	1	**- 4.375**
1	0	0	0	**- 5.000**
1	0	0	1	**- 5.625**
1	0	1	0	**- 6.250**

1	0	1	1	**- 6.875**
1	1	0	0	**- 7.500**
1	1	0	1	**- 8.125**
1	1	1	0	**- 8.750**
1	1	1	1	**- 9.375**

Table 1: Voltage Output of 4-bit DAC using Binary Weighted Resistor Network

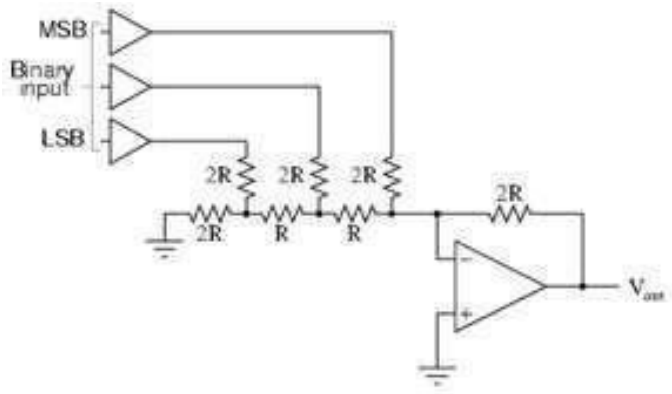
The LSB, which is also the incremental step, has a value of - 0.625 V while the MSB or the full scale has a value of - 9.375 V.

Practical Limitations:

- The most significant problem is the large difference in resistor values required between the LSB and MSB, especially in the case of high resolution DACs (i.e. those that has large number of bits). For example, in the case of a 12-bit DAC, if the MSB is 1 k□, then the LSBis a staggering 2 M
- The maintanence of accurate resistances over a large range of values is problematic. With the current IC fabrication technology, it is difficult to manufacture resistors over a wide resistance range that maintain an accurate ratio especially with variations in temperature.

R-2R LADDER DAC

An enhancement of the binary-weighted resistor DAC is the R-2R ladder network. This type of DAC utilizes Thevenin‘s theorem in arriving at the desired output voltages. The R-2R network consists of resistors with only two values - R and 2xR. If each input is supplied either 0 volts or reference voltage, the output voltage will be an analog equivalent of the binary value of the three bits. VS2 corresponds to the most significant bit (MSB) while VS0 corresponds to the least significant bit (LSB).

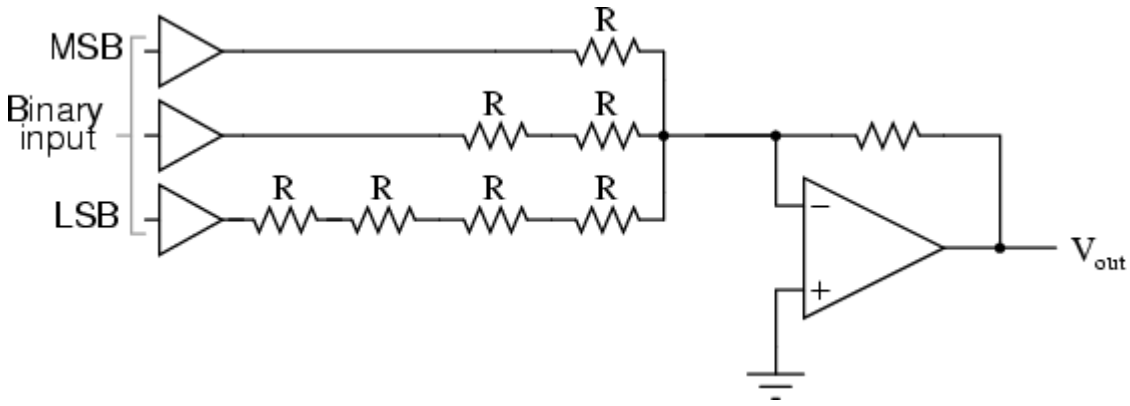


Vout = - (VMSB + Vn + VLSB) = - (VRef + VRef/2 + VRef/ 4)

The R/2R DAC

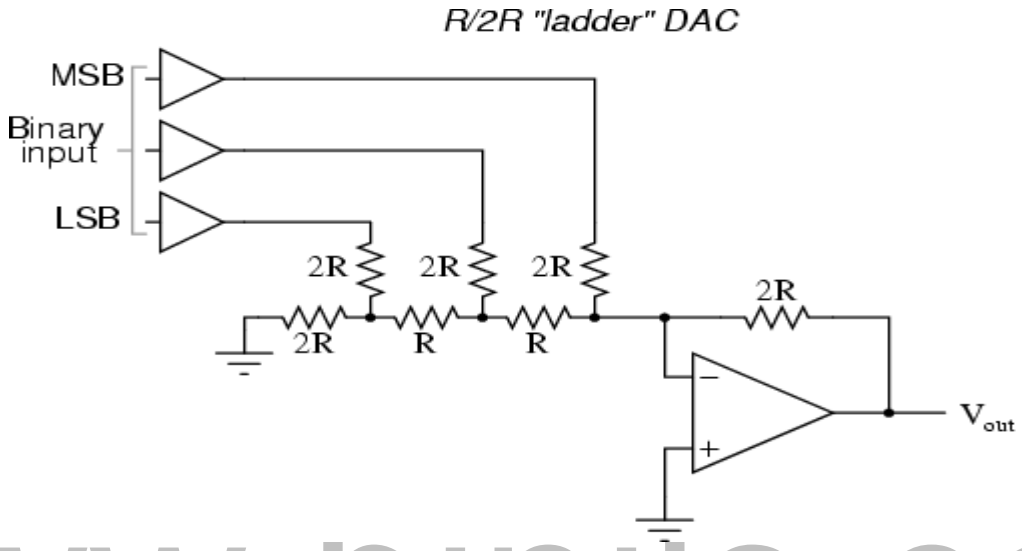
An alternative to the binary-weighted- input DAC is the so-called R/2R DAC, which uses fewer unique resistor values. A disadvantage of the former DAC design was its requirement of several different precise input resistor values: one unique value per binary input bit. Manufacture may be simplified if there are fewer different resistor values to purchase, stock, and sort prior to assembly.

Of course, we could take our last DAC circuit and modify it to use a single input resistance value, by connecting multiple resistors together in series:



Unfortunately, this approach merely substitutes one type of complexity for another: volume of

components over diversity of component values. There is, however, a more efficient design methodology. By constructing a different kind of resistor network on the input of our summing circuit, we can achieve the same kind of binary weighting with only two kinds of resistor values, and with only a modest increase in resistor count. This "ladder" network looks like this:



Mathematically analyzing this ladder network is a bit more complex than for the previous circuit, where each input resistor provided an easily-calculated gain for that bit. For those who are interested in pursuing the intricacies of this circuit further, you may opt to use Thevenin's theorem for each binary input (remember to consider the effects of the *virtual ground*), and/or use a simulation program like SPICE to determine circuit response. Either way, you should obtain the following table of figures:

Binary	Output voltage
000	0.00 V
001	-1.25 V
010	-2.50 V
011	-3.75 V
100	-5.00 V

101	-6.25 V
110	-7.50 V
111	-8.75 V

As was the case with the binary-weighted DAC design, we can modify the value of the feedback resistor to obtain any "span" desired. For example, if we're using +5 volts for a "high" voltage level and 0 volts for a "low" voltage level, we can obtain an analog output directly corresponding to the binary input (011 = -3 volts, 101 = -5 volts, 111 = -7 volts, etc.) by using a feedback resistance with a value of 1.6R instead of 2R.

INVERTED OR CURRENT MODE DAC

As the name implies, Current mode DACs operates based on the ladder currents. The ladder is formed by resistance R in the series path and resistance 2R in the shunt path. Thus the current is divided into $i1$, $i2$, $i3$.....in in each arm. The currents are either diverted to the ground bus (io) or to the Virtual- ground bus (io).

The currents are given as

$i1 = VREF/2R = (VREF/R)\ 2^{-1}$, $i2 = (VREF)/2)/2R = (VREF/R)\ 2^{-2}$ ..... $i_n = (VREF/R)\ 2^{-n}$.

And the relationship between the currents are given as

$$i2 = i_1/2$$

$$i3 = i_1/4$$

$$i4 = i_1/8$$

$$in = i_1/2^{n-1}$$

Using the bits to identify the status of the switches, and letting $V_0 = -R_f i_o$ gives

$$V_0 = -(R_f/R)\ V_{REF}\ (b_1 2^{-1} + b_2 2^{-2} + ... + b_n 2^{-n})$$

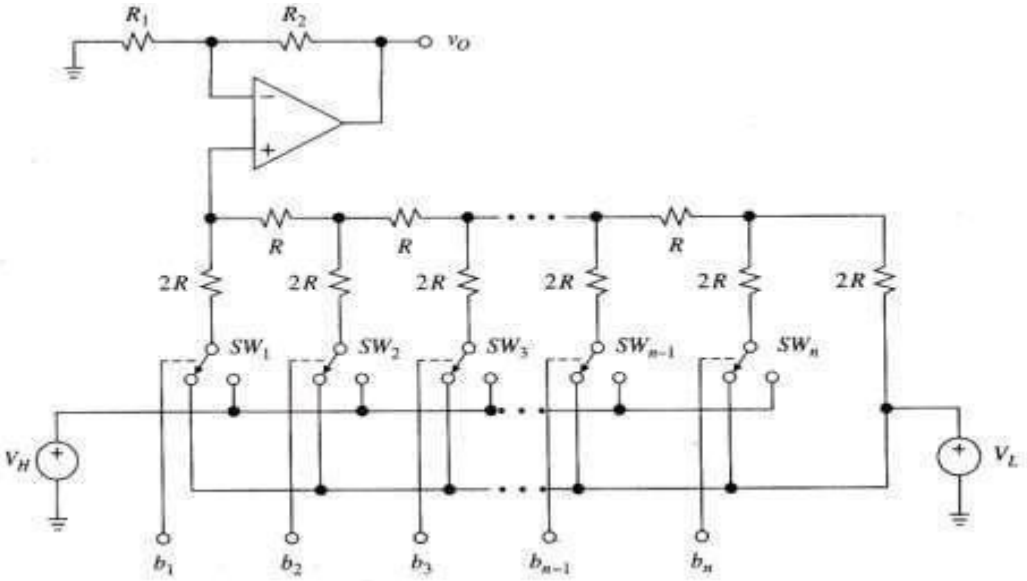
The two currents *io* and *io* are complementary to each other and the potential of *io* bus must be sufficiently close to that of the *io* bus. Otherwise, linearity errors will occur. The final op-amp is used as current to voltage converter.

Advantages

1. The major advantage of current mode D/A converter is that the voltage change across each switch is minimal. So the charge injection is virtually eliminated and the switch driver design is made simpler.
2. In Current mode or inverted ladder type DACs, the stray capacitance do not affect the speed of response of the circuit due to constant ladder node voltages. So improved speed performance.

VOLTAGE MODE DAC

This is the alternative mode of DAC and is called so because, the 2R resistance in the shunt path is switched between two voltages named as V_L and V_H. The output of this DAC is obtained from the leftmost ladder node. As the input is sequenced through all the possible binary state starting from All 0s (0… 0) to all 1s (1… 1). The voltage of this node changes in steps of $2^{-n}\ (V_H - V_L)$ from the



The diagram also shows a non- inverting amplifier from which the final output is taken. Due to thisbuffering with a non- inverting amplifier, a scaling factor defined by $K = 1 + (R_2/R_1)$ results.

Advantages

1. The major advantage of this technique is that it allows us to interpolate between any twovoltages, neither of which need not be a zero.
2. More accurate selection and design of resistors R and 2R are possible and simple construction.
3. The binary word length can be easily increased by adding the required number orR-2R sections.
4. minimum voltage of $Vo = V_L$ to the maximum of $Vo = V_H - 2^{-n} (V_H - V_L)$.

Clippers and Clampers:

Waveshaping circuits are commonly used in digital computers and communication such as TV and FM receiver. Waveshaping technique include clipping and clamping. In op-amp clipper circuits a rectifier diode may be used to clip off a certain portion of the input signal to obtain a desired o/p waveform. The diode works as an ideal diode (switch) because when on -> the voltage drop across the diode is divided by the open loop gain of the op-amp. When off(reverse biased) -> the diode is an open circuit.

In an op-amp clamper circuits, however a predetermined dc level is deliberately inserted in the o/p volt. For this reason, the clamper is sometimes called a dc inverter.

Positive and Negative Clipper:

Positive Clipper:

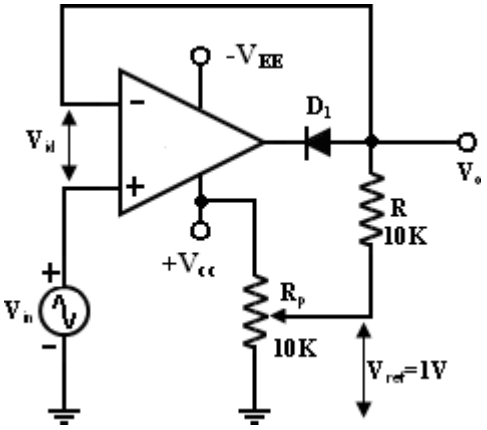
A Circuit that removes positive parts of the input signal can be formed by using an op-amp with a rectifier diode. The clipping level is determined by the reference voltage Vref, which should less than the i/p range of the op-amp (Vref < Vin). The Output voltage has the portions of the positive half cycles above Vref clipped off.

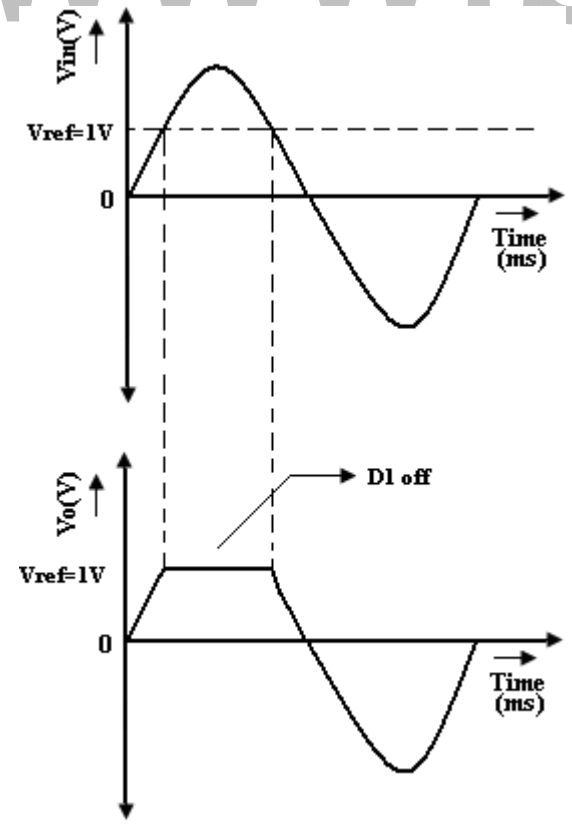
The circuit works as follows:

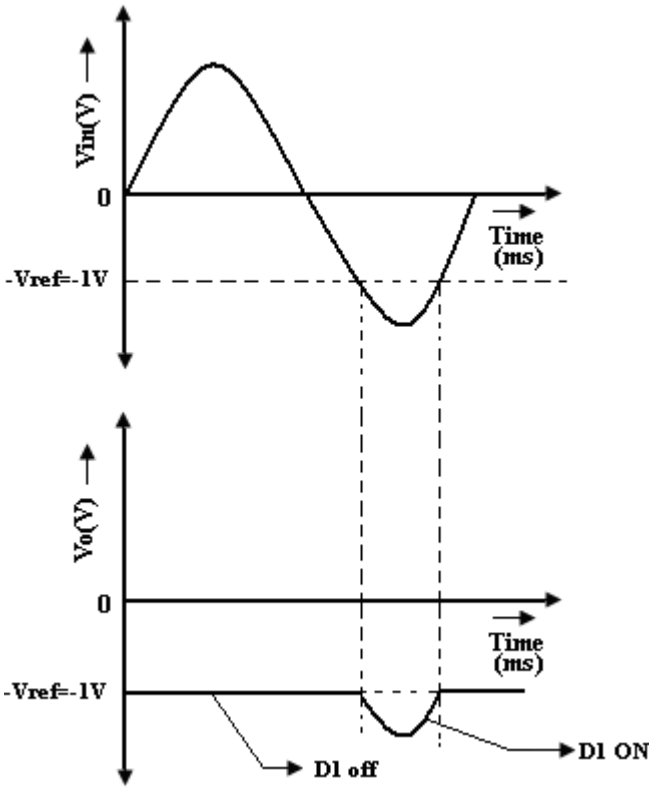
During the positive half cycle of the input, the diode D_1 conducts only until Vin = Vref. This happens because when Vin <Vref, the output volts V_0 _ of the op-amp becomes negative to device D_1 into conduction when D_1 coonducts it closes feedback loop and op-amp operates as a voltage follower. (i.e) Output V_0 follows input until Vin = Vref.

When Vin > Vref => the V'_0 becomes +ve to derive D_1 into off. It open the feedback loop and op-amp operates open loop. When Vin drops below Vref (Vin<Vref) the o/p of the op-amp V'_0 again becomes –ve to device D_1 into conduction. It closed the f/b. (o/p follows the i/p). Thus diode D_1 is

on for vin<Vref (o/p follows the i/p) and D_1 is off for Vin>Vref. The op-amp alternates between open loop (off) and closed loop operation as the D_1 is turned off and on respectively. For this reason the op-amp used must be high speed and preferably compensated for unitygain.

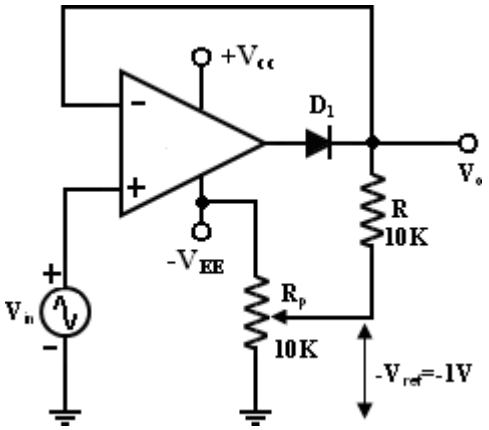


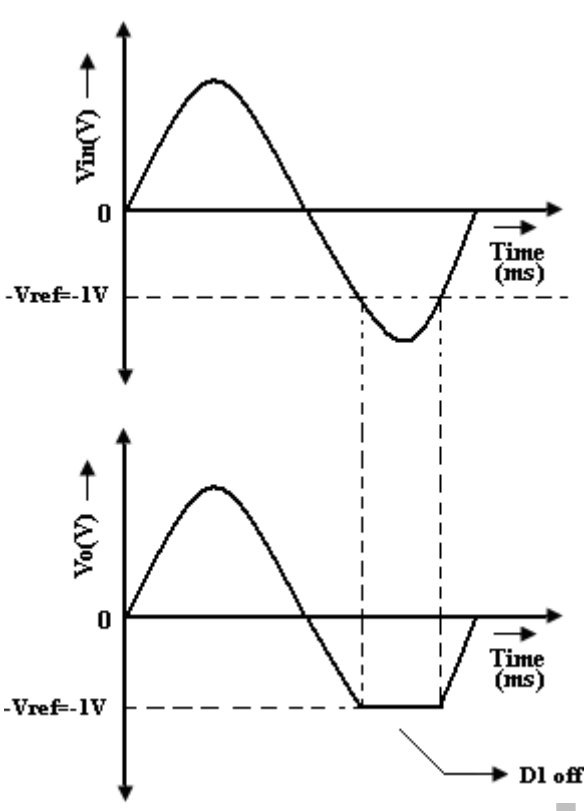


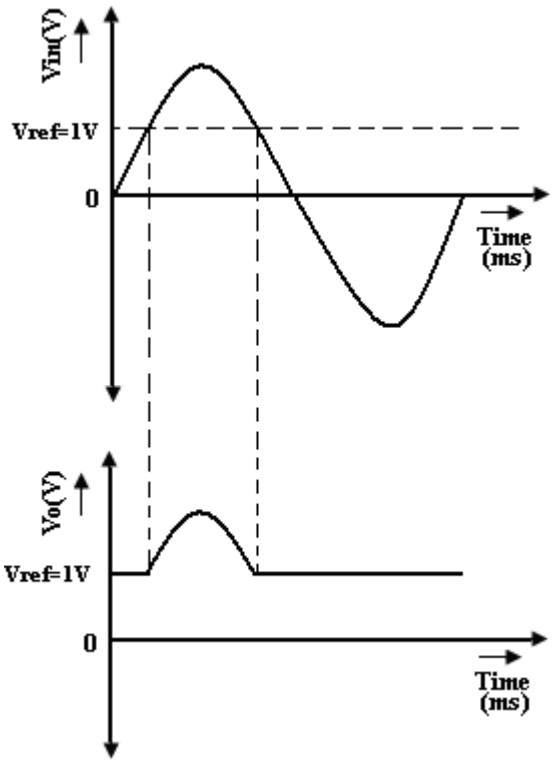


Ex: for high speed op-amp HA 2500, LM310, µA 318. In addition the difference input voltage (Vid=high) is high during the time when the feedback loop is open (D_1 is off) hence an op-amp with a high difference input voltage is necessary to prevent input breakdown. If R_p (pot) is connected to $-V_{EE}$ instead of +Vcc, the ref voltage Vref will be negative (Vref = - ve). This will cause the entire o/p waveform above –Vref to be clipped off.

Negative Clipper:







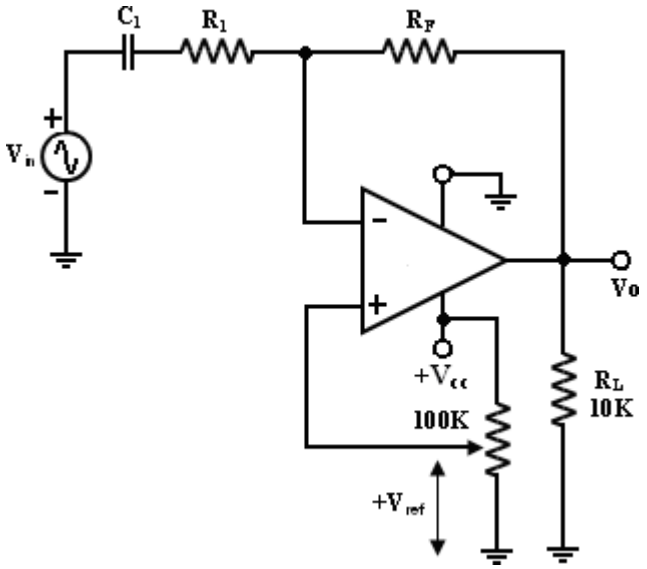
The positive clipper is converted into a –ve clipper by simply reversing diode D_1 and changing the polarity of Vref voltage. The negative clipper -> clips off the –ve parts of the input signal belo w the reference voltage. Diode D_1 conducts -> when Vin > -Vref and therefore during this period o/p volt V_0 follows the i/p volt Vin. The –Ve portion of the output volt below –Vref is clipped off because (D_1 is off) Vin<-Vref. If –Vref is changed to –Vref by connecting the potentiometer R_p to the +Vcc, the V_0 below +Vref will be clipped off. The diode D_1 must be on for Vin > Vref and off for Vin.

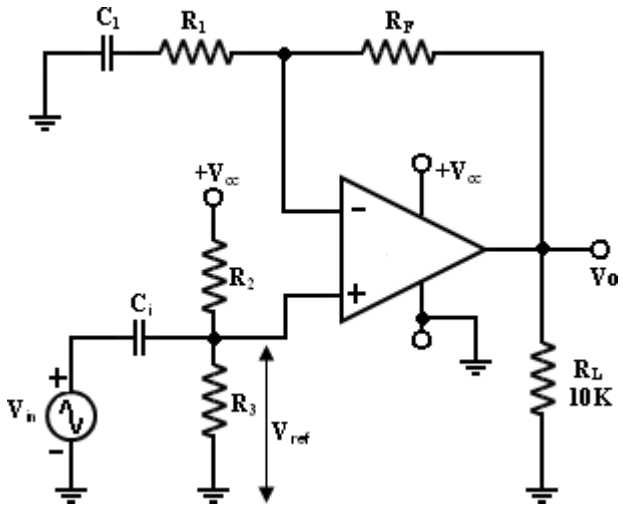
Positive and Negative Clampers:

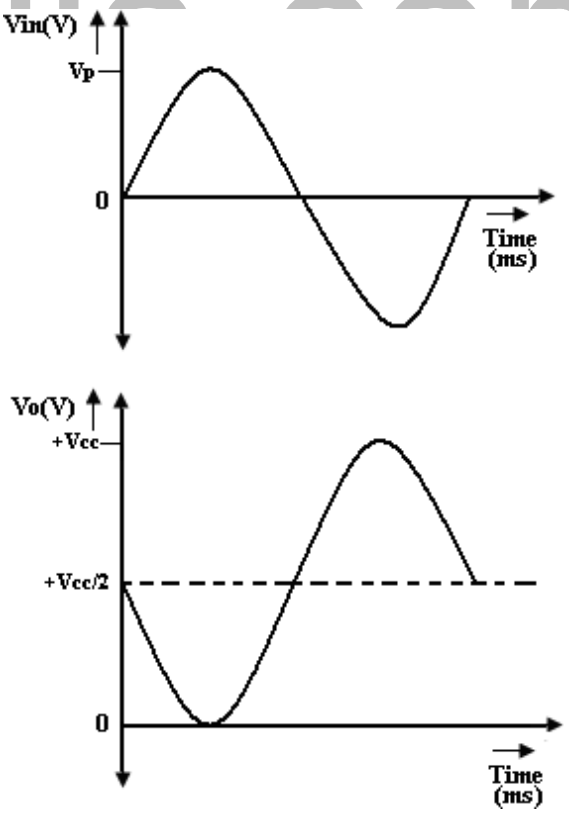
In clamper circuits a predetermined dc level is added to the output voltage. (or) The output is clamped to a desired dc level.

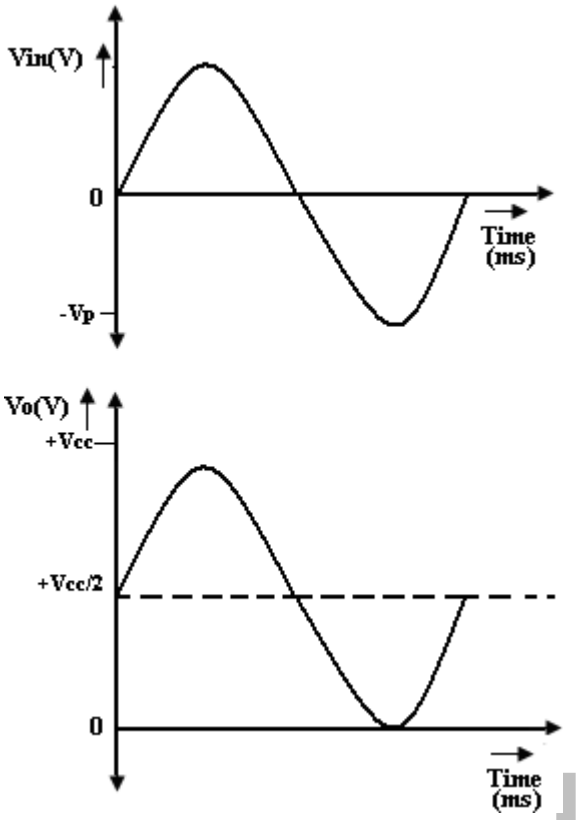
1. If the clamped dc level is +ve, the clamper is positive clamper
2. If the clamped dc level is –ve, the clamper is negative clamper.

Other equivalent terms used for clamper are dc inserter or restorer. Inverting and Non-Inverting that use this technique.









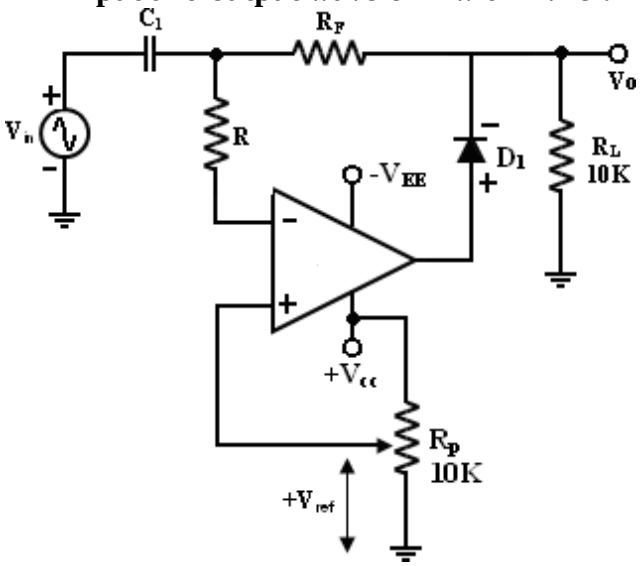
Capacitor:

The Value of the capacitors in these circuits depends on different input rates and pulse widths.

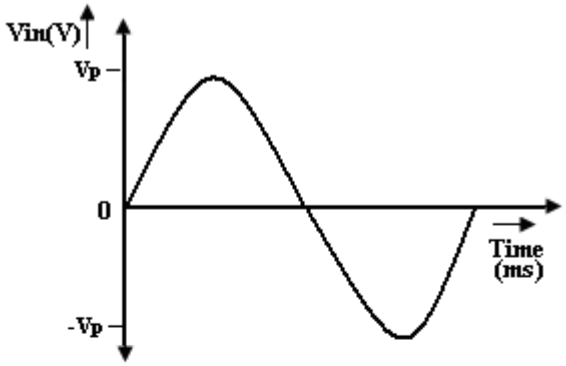
1. In both circuits the dc level added to the o/p voltage is approximately equal to Vcc/2.
2. This +ve fixed dc level is needed to obtain a maximum undistored symmetrical sine wave.

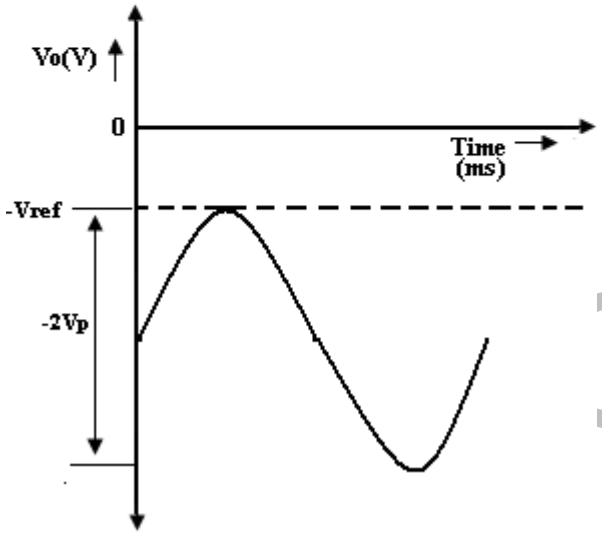
Peak clamper circuit:

Input and output waveform with +Vref:



Input and Output Waveform with –Vref:





In this circuit, the input waveform peak is clamped at Vref. For this reason, the circuit is called the peak clamper.

First consider the input voltage Vref at the (+) input: since this volt is +ve, V'_0 is also +ve which forward biases D_1 . This closed the feedback loop.

Voltage Vin at the (-) input: During its –ve half cycle, diode D_1 conducts, charging c; to the –ve peak value of V_p . During the +ve half cycle, diode D_1 in reverse biased. Since this voltage V_p is in series with the +ve peak volt V_p the o/p volt $V_0 = 2\ V_p$. Thus the nett o/p is Vref plus 2 V_p. so the –ve peak of 2 V_p is at Vref. For precision clamping, $C_iR_d << T/2$

Where R_d = resistance of diode D_1 when it is forward biased.

T = time period of the input waveform.

Resistor r => is used to protect the op-amp against excessive discharge currents from capacitor C_i especially when the dc supply voltages are switched off. A +ve peak c lamping is accomplished by reversing D_1 and using –ve reference voltage (-Vref).

Note:

Inv and Non-Inv clamper – Fixed dc level

Peak clamper – Variable dc level

Active filters:

Another important field of application using op-amp.

Filters and Oscillators:

An electric filter is often a frequency selective circuit that passes a specified band of frequencies and blocks or alternates signal and frequencies outside this band.

Filters may be classified as

1. Analog or digital.
2. Active or passive
3. Audio (AF) or Radio Frequency (RF)

1. Analog or digital filters:

Analog filters are designed to process analog signals, while digital filters process analog signals using digital technique.

2. Active or Passive:

Depending on the type of elements used in their construction, filter may be classified as passive or Active elements used in passive filters are Resistors, capacitors, inductors. Elements used in active filters are transistor, or op-amp.

Active filters offers the following advantages over a passive filters:

1. Gain and Frequency adjustment flexibility:

Since the op-amp is capable of providing a gain, the i/p signal is not attenuated as it is in a passive filter. [Active filter is easier to tune or adjust].

2. No loading problem:

Because of the high input resistance and low o/p resistance of the op-amp, the active filter does not cause loading of the source or load.

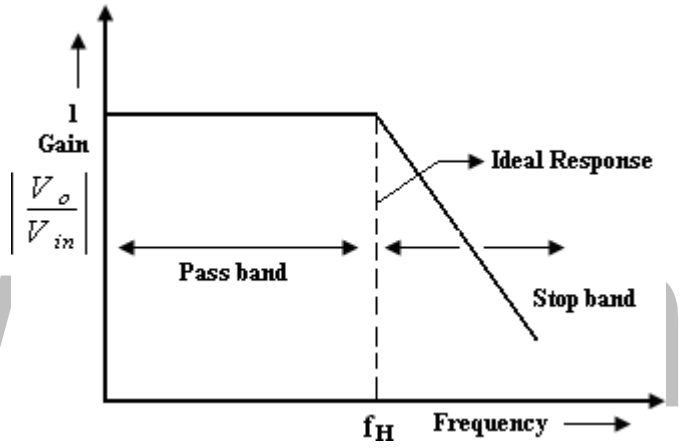
3. Cost:

Active filters are more economical than passive filter. This is because of the variety of cheaper op-amps and the absence of inductors.

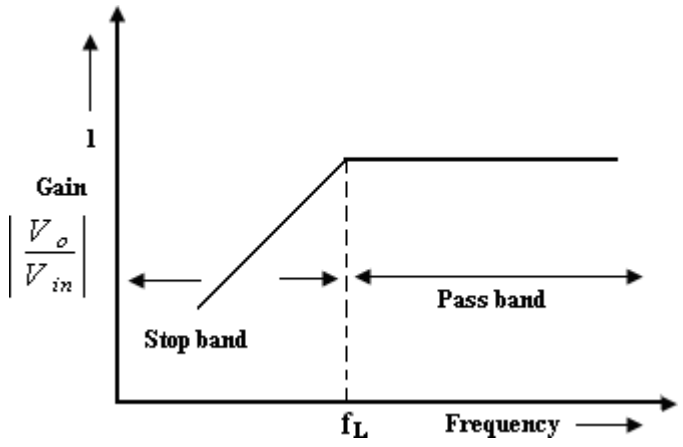
The most commonly used filters are these:

1. Low pass Filters
2. High pass Filters
3. Band pass filters
4. Band –reject filters
5. All pass filters.

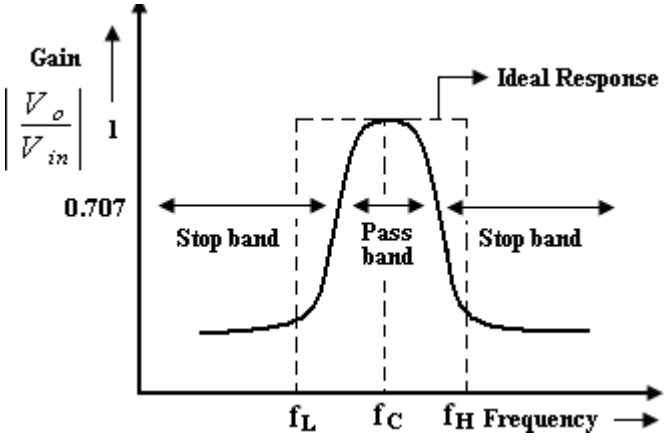
Frequency response of the active filters:



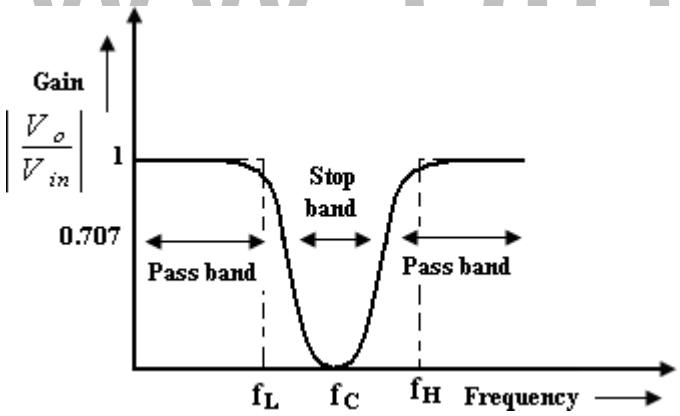
Low pass Filter



High pass Filter



Band Pass Filters



Band Reject

Low pass filters:

1. It has a constant gain from 0 Hz to a high cutoff frequency f_1.
2. At f_H the gain in down by 3db.

3. The frequency between 0hz and f_H are known as the passband frequencies. Where as the range of frequencies those beyond f_H, that are attenuated includes the stopband frequencies.
4. Butterworth, clebyshev and cauer filter are some of the most commonly used practical filters.
5. The key characteristics of the butter worth filter is that it has a flat pass band as well as stop band. For this reason, it is sometimes called a flat- flat filters.
6. Chebyshev filter -> has a ripple pass band & flat stop band.
7. Causer Filter -> has a ripple pass band & ripple stopband. It gives best stopband response among the three.

High pass filter:

High pass filter with a stop band $0<f< f_L$ and a pass band $f> f_L$

f_L -> low cut off frequency

f -> operating frequency.

Band pass filter:

It has a pass band between 2 cut off frequencies f_H and f_L where $f_H > f_L$ and two, stop bands : $0<f< f_L$ and $f > f_H$ between the band pass filter (equal to $f_H - f_L$.

Band –reject filter: (Band stop or Band elimination)

It performs exactly opposite to the band pass. It has a band stop between 2 cut-off frequency f_L and f_H and 2 passbands: $0<f< f_L$ and $f> f_H$

f_C -> center frequency.

Note:

The actual response curves of the filters in the stopband either R or S or both with R in frequencies.

The rate at which the gain of the filter changes in the stopband is determined by the order of the filter.

Ex: 1st order low pass filter the gain rolls off at the rate of 20dB/decade in the stopband. (i.e) for $f > f_H$.

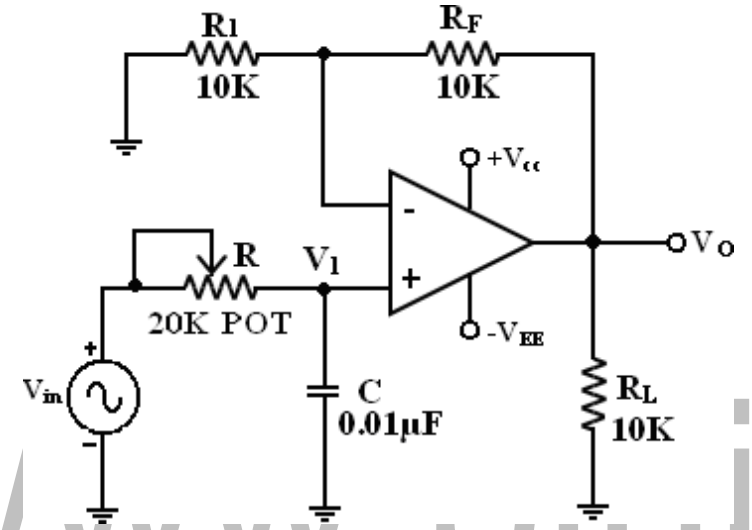
2nd order LPF -> the gain roll off rate is 40dB/decade.

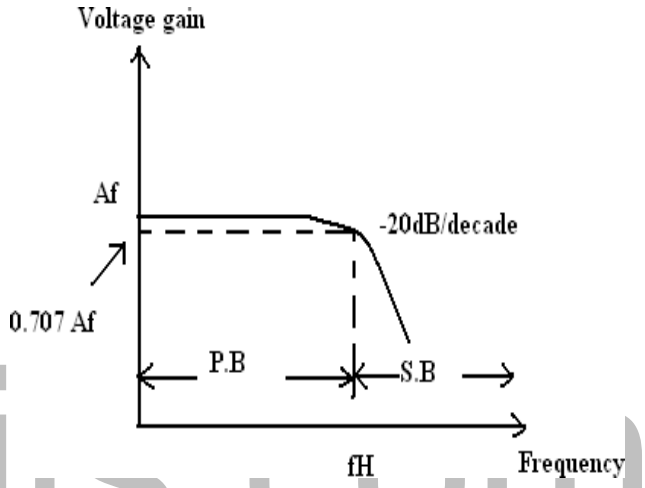
1st order HPF -> the gain Rs at the rate of 20dB (i.e) until f:f_L

2nd order HPF -> the gain Rs at the rate of 40dB/decade

First order LPF Butterworth filter:

First order LPF that uses an RC for filtering op-amp is used in the non inverting configuration. Resistor R1 & R_f determine the gain of the filter. According to the voltage –divider rule, the voltage at the non-inverting terminal (across capacitor) C is,

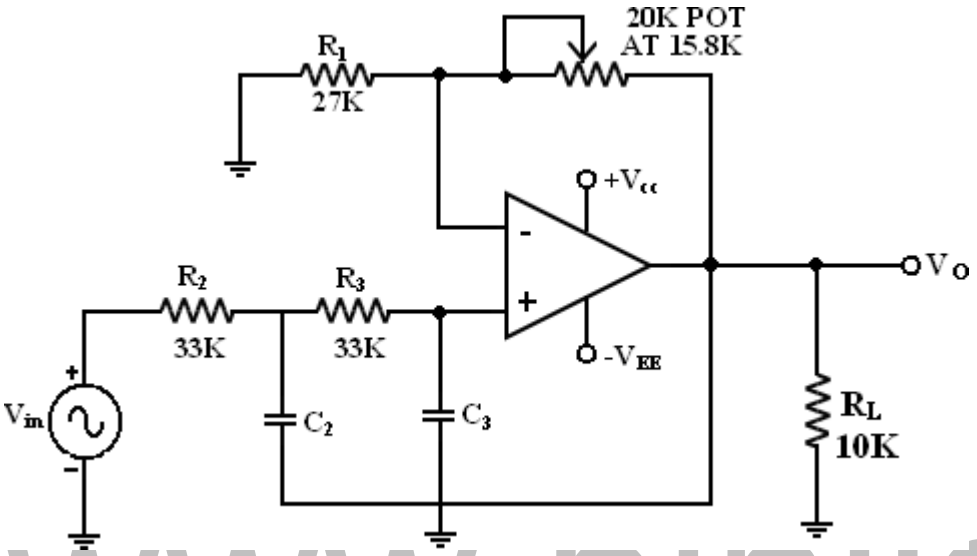


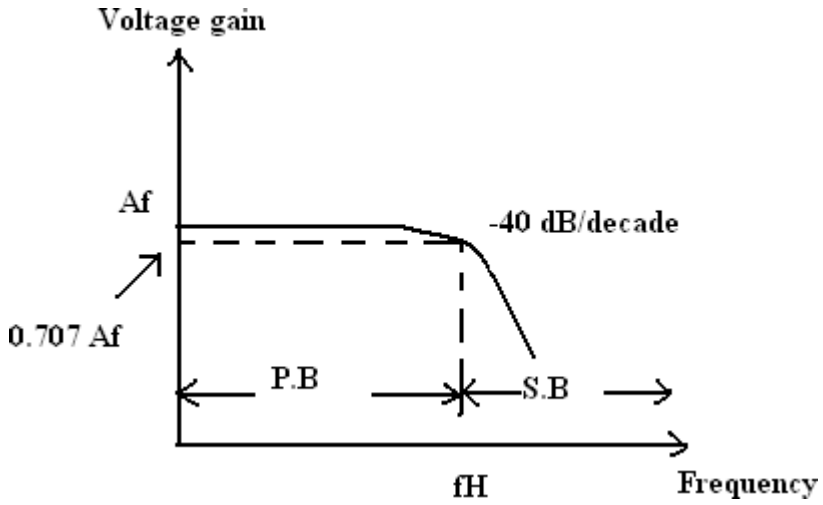


Second order LP Butterworth filter:

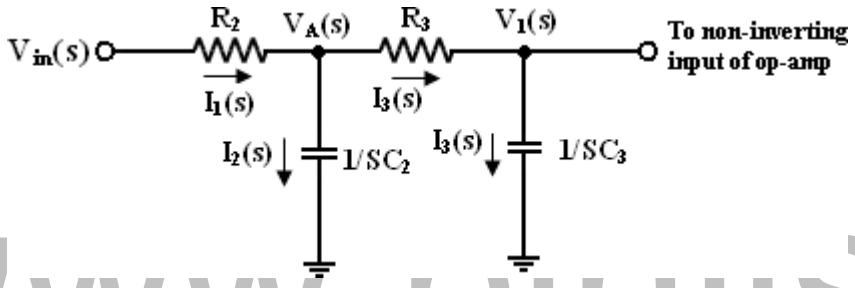
A second order LPF having a gain 40dB/decade in stop band. A First order LPF can be converted into a II order type simply by using an additional RC network.

The gain of the II order filter is set by R1 and R_F, while the high cut off frequency f_H is determined by R2,C2,R3 and C3.





This above fig transferred into S domain.



In this circuit all the components and the circuit parameters are expressed in the S-domain where S = j .

Writing Kirchoff's current law at node $V_A(S)$.

$$I_1 = I_2 + I_3$$

and solving for V_1 *, we get,*

The denominator quadratic in the gain (V_0/Vin) eqn must have two real and equal roots. This means that

Filter Design:

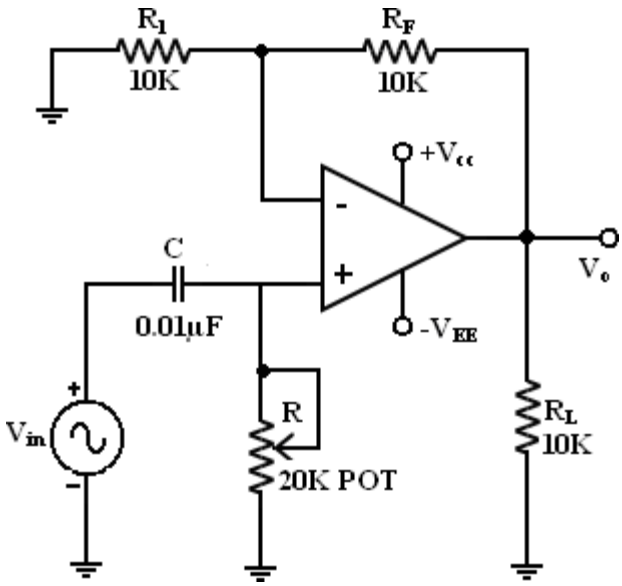
1. Choose a value for a high cut off freq (f_H).
2. To simplify the design calculations, set $R_2 = R_3 = R$ and $C_2 = C_3 = C$ then choose a value of c<=1μf.
4. Finally, because of the equal resistor ($R_2 = R_3$) and capacitor ($C_2 = C_3$) values, the pass band volt gain $A_F = 1 + R_F / R_1$ of the second order had to be = to 1.586. $R_F = 0.586\ R_1$. Hence choose a value of R_1 <=100kΩ and
5. Calculate the value of R_F.

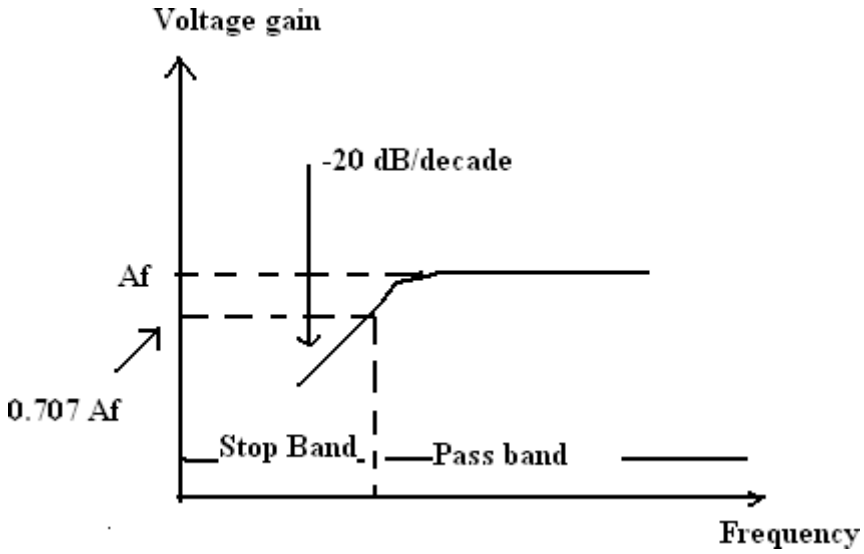
First order HP Butterworth filter:

High pass filters are often formed simply by interchanging frequency-determining resistors and capacitors in low-pass filters.

(i.e) I order HPF is formed from a I order LPF by interchanging components R & C.

Similarly II order HPF is formed from a II order LPF by interchanging R & C.



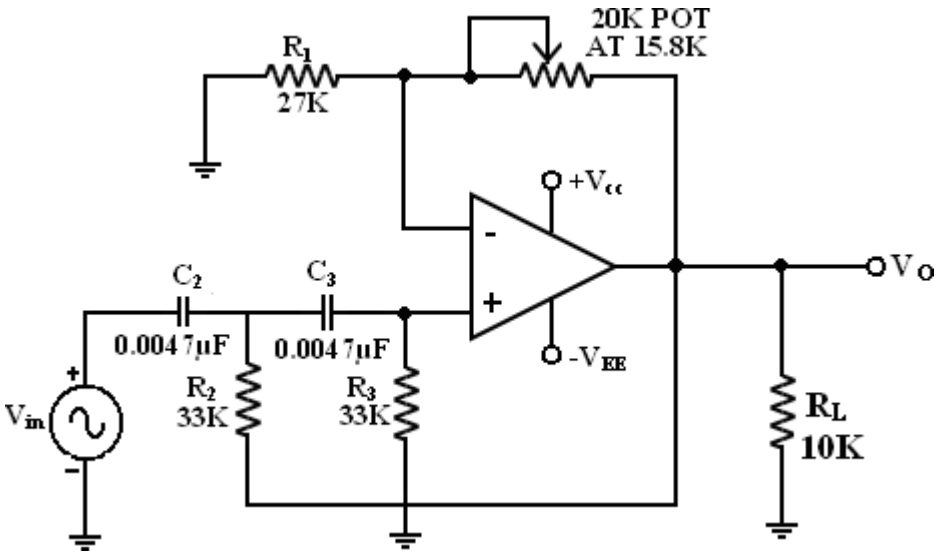


Here I order HPF with a low cut off frequency of f_L. This is the frequency at which the magnitude of the gain is 0.707 times its passband value.

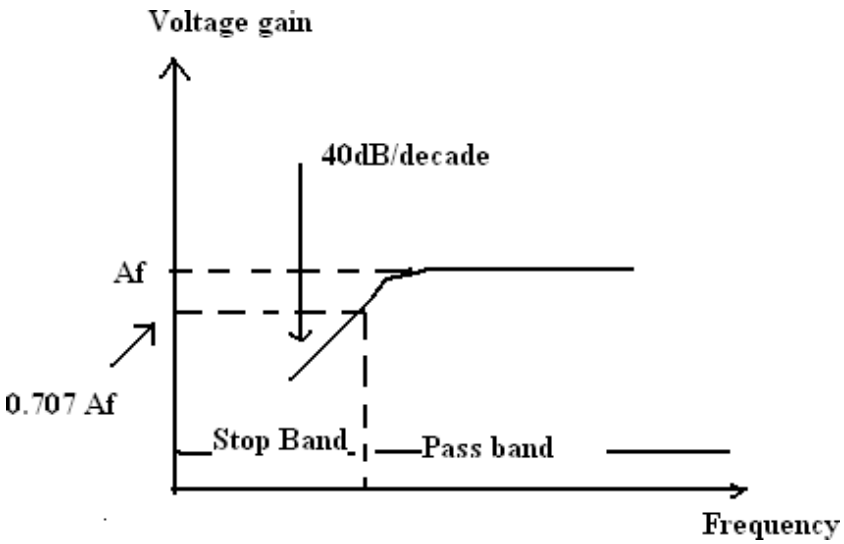
Here all the frequencies higher than f_L are passband frequencies.

Second – order High Pass Butterworth Filter:

I order Filter, II order HPF can be formed from a II order LPF by interchanging the frequency – determine resistors and capacitors.



II order HPF



Comparator

To obtain for better performance, we shall also look at integrated designed specifically as comparators and converters. A comparator as its name implies, compares a signal voltage on one input of an op-amp with a known voltage called a reference voltage on the other input. Comparators are used in circuits such as,

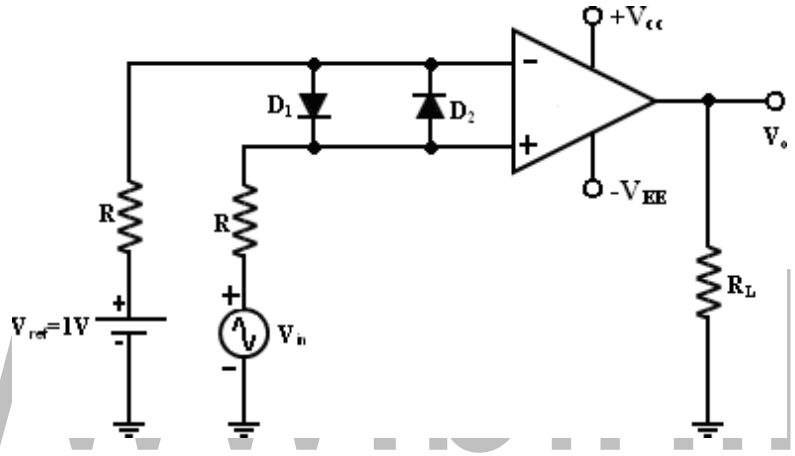
Digital Interfacing

Schmitt Trigger

Discriminator

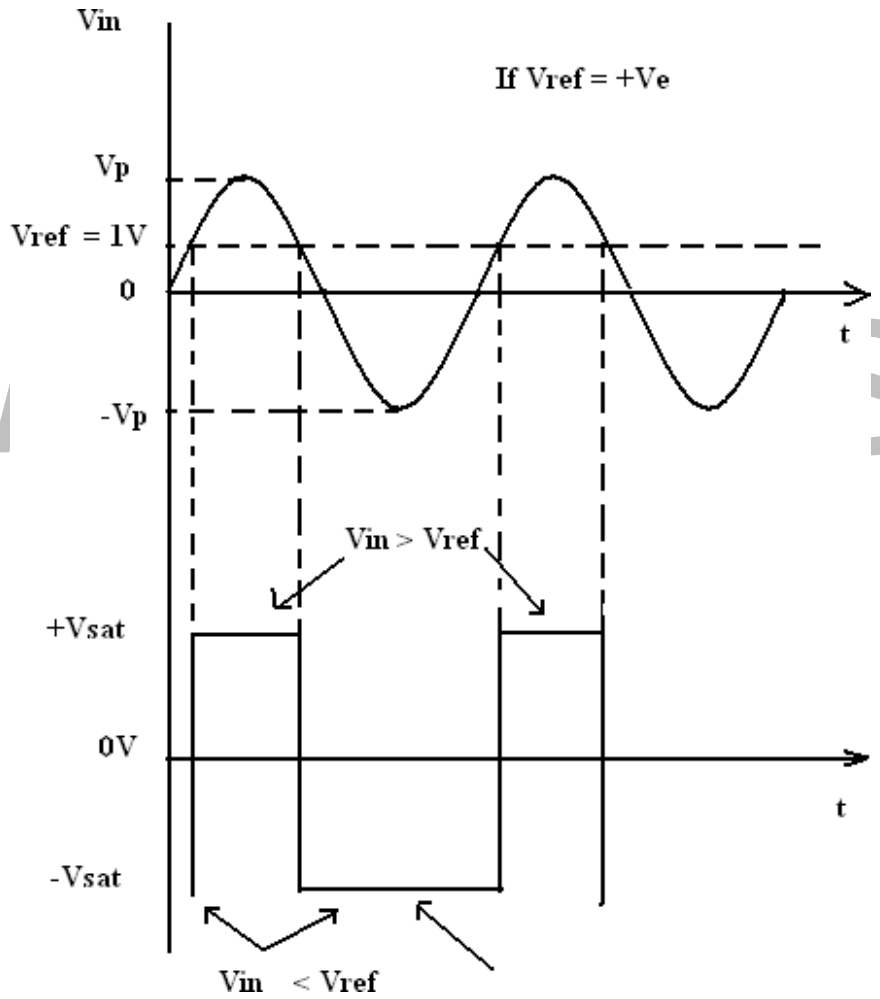
Voltage level detector and oscillators

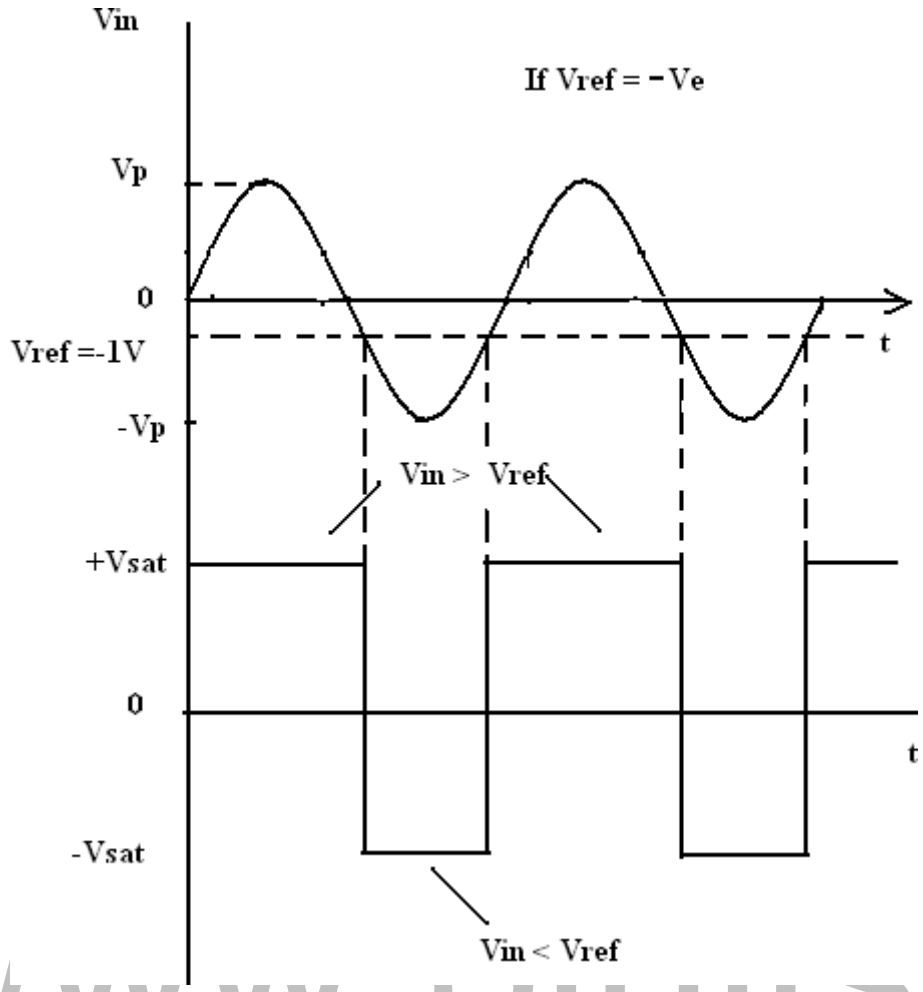
1. Non-inverting Comparator:



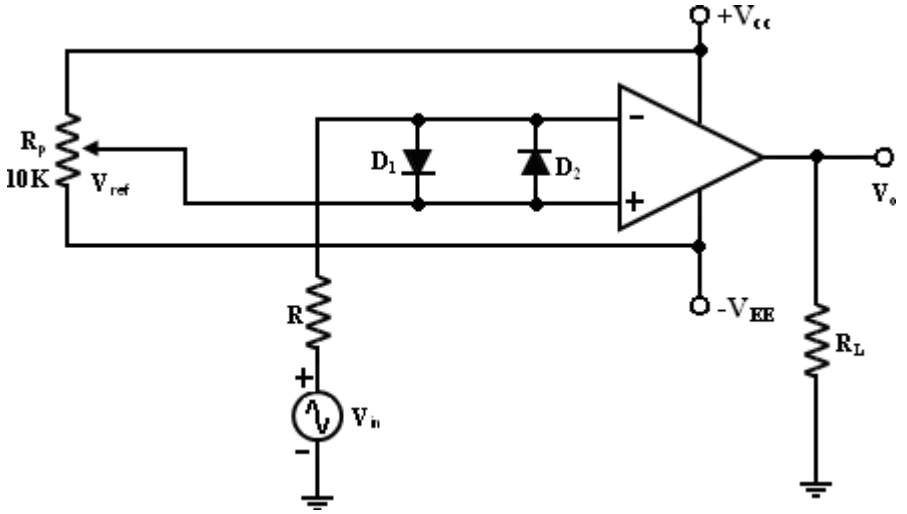
A fixed reference voltage Vref of 1 V is applied to the negative terminal and time varying signal voltage Vin is applied tot the positive terminal.When Vin is less than Vref the output becomes V_0 at –Vsat [Vin < Vref => V_0 (-Vsat)]. When Vin is greater than Vref, the (+) input becomes positive, the V_0 goes to +Vsat. [Vin > Vref => V_0 (+Vsat)]. Thus the V_0 changes from one saturation level to another. The diodes D_1 and D_2 protects the op-amp from damage due to the excessive input voltage Vin. Because of these diodes, the difference input voltage Vid of the op-amp diodes are called clamp diodes. The resistance R in series with Vin is used to limit the current through D_1 and D_2 . To reduce offset problems, a resistance Rcomp = R is connected between the (- ve) input and Vref.

Input and Output Waveforms:



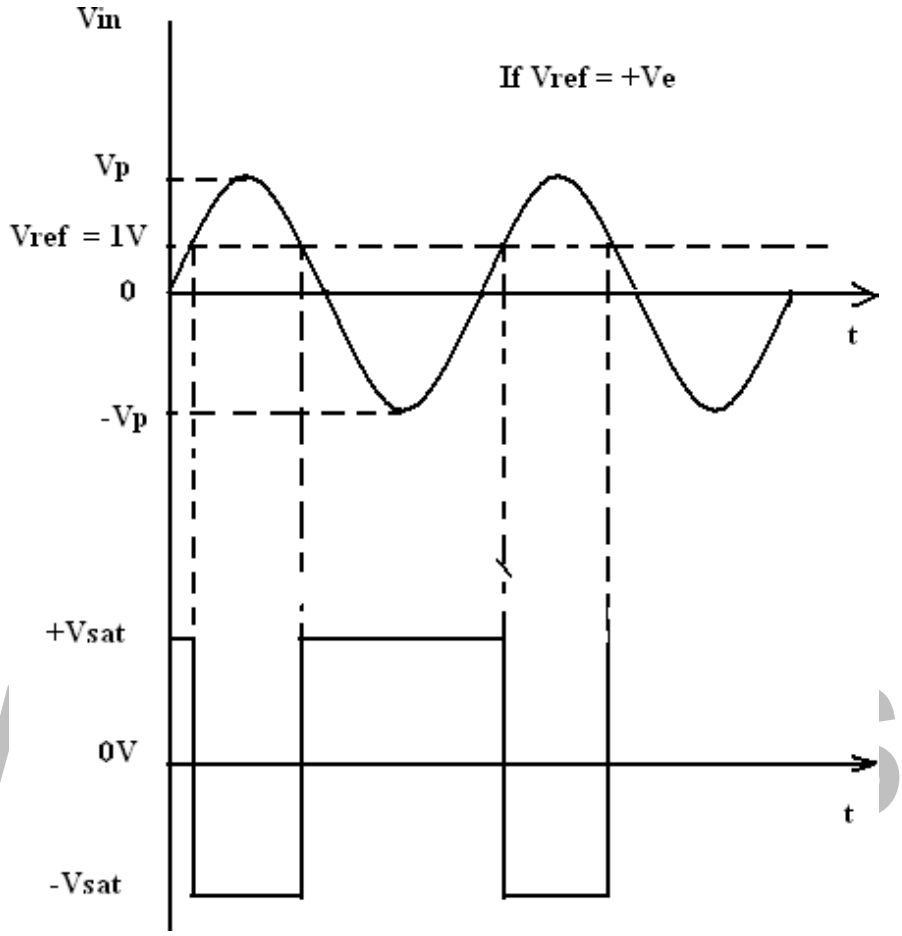


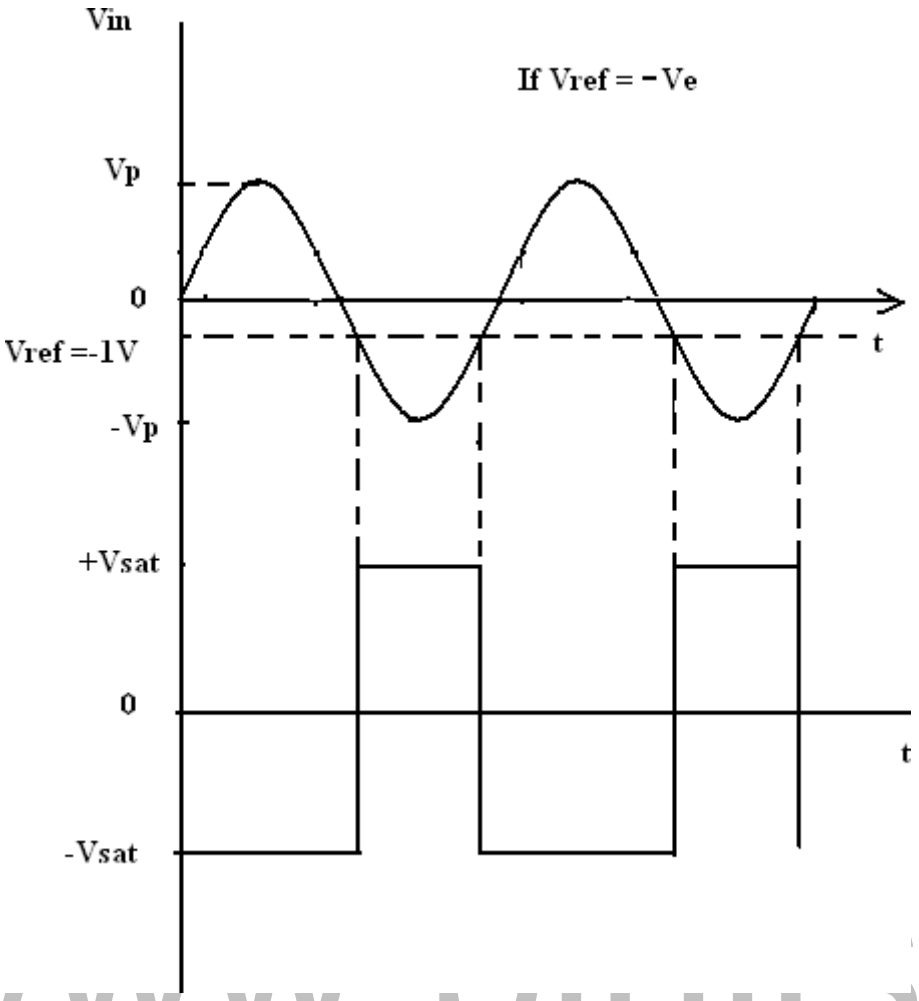
2. Inverting Comparator:



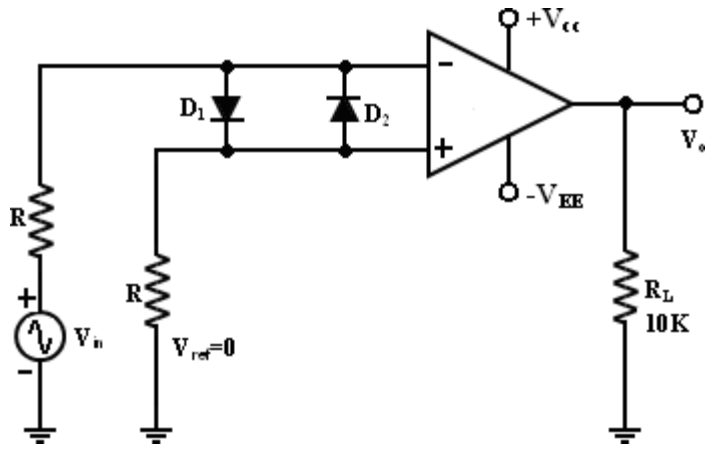
This fig shows an inverting comparator in which the reference voltage Vref is applied to the (+) input terminal and Vin is applied to the (-) input terminal. In this circuit Vref is obtained by using a

10K potentiometer that forms a voltage divider with dc supply volt +Vcc and -1 and the wiper connected to the input. As the wiper is moved towards +Vcc, Vref becomes more positive. Thus a Vref of a desired amplitude and polarity can be obtained by simply adjusting the 10k potentiometer.



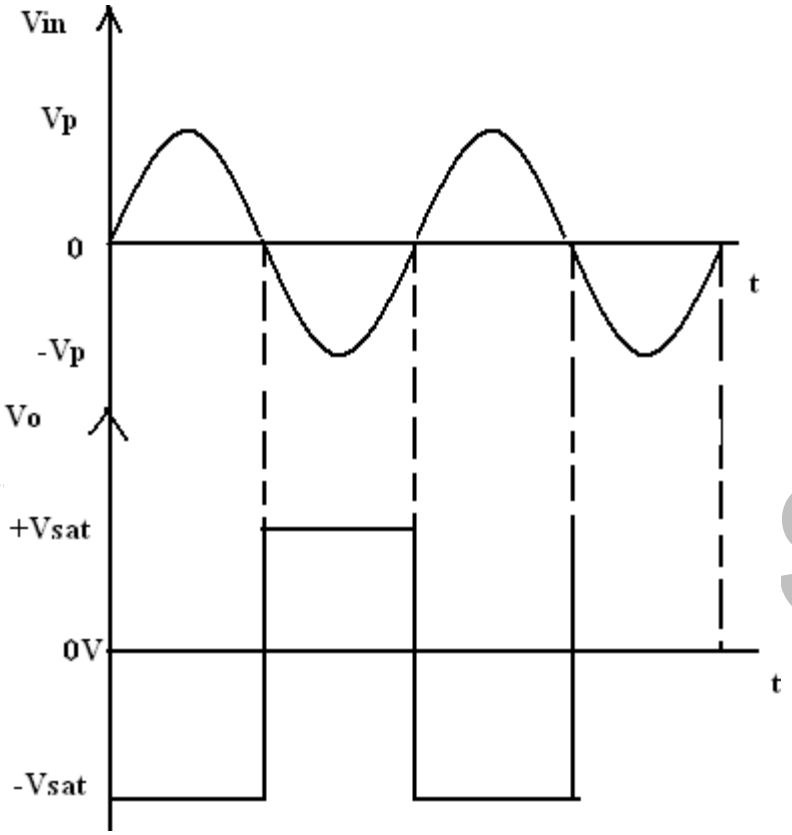


3. Ze ro Crossing Detector: [Sine wave to Square wave converter]



One of the application of comparator is the zero crossing detector or -sine wave to Square wave Converter‖. The basic comparator can be used as a zero crossing detector by setting Vref is set to Zero. (Vref =0V).

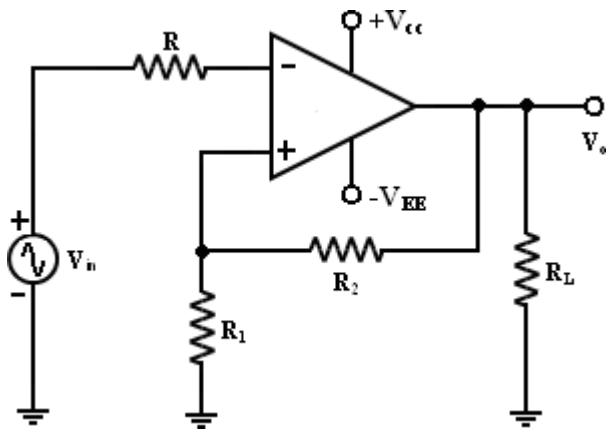
This Fig shows when in what direction an input signal Vin crosses zero volts. (i.e) the o/p V_0 is driven into negative saturation when the input the signal Vin passes through zero in positive direction. Similarly, when Vin passes through Zero in negative direction the output V_0 switches and saturates positively.

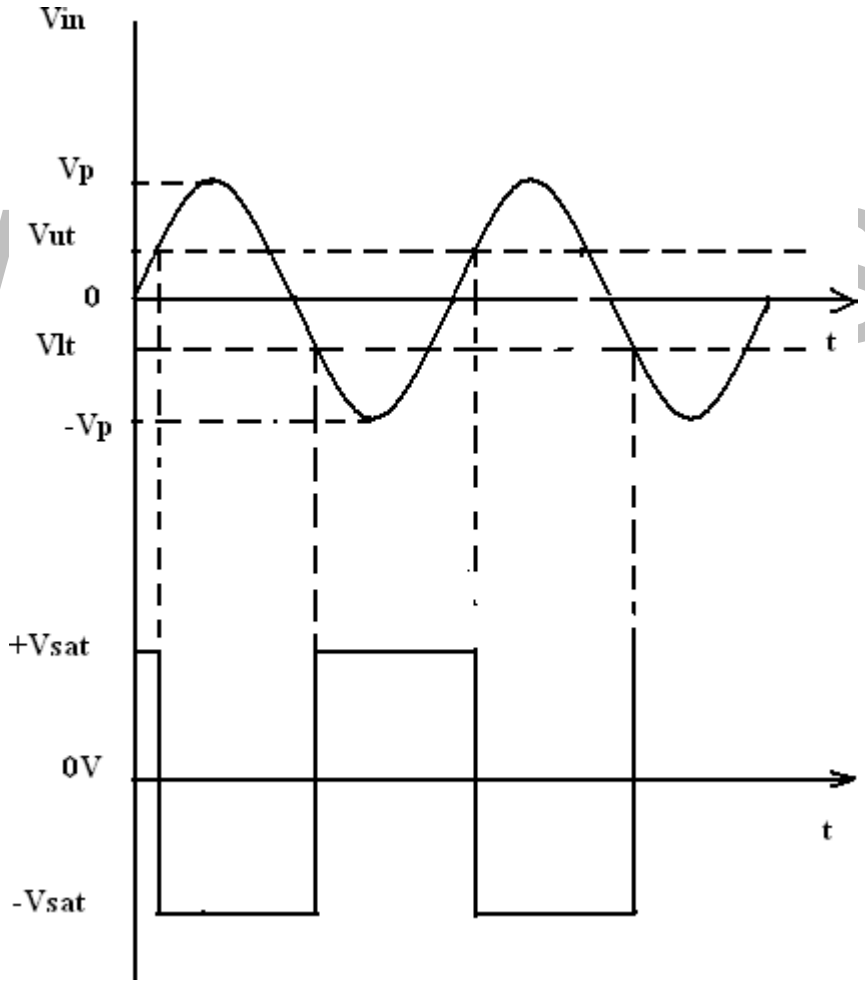


Drawbacks of Ze ro- crossing detector:

In some applications, the input Vin may be a slowly changing waveform, (i.e) a low frequency signal. It will take Vin more time to cross 0V, therefore V_0 may not switch quickly from one saturation voltage to the other. Because of the noise at the op-amp‘s input terminals the output V_0 may fluctuate between 2 saturations voltages +Vsat and –Vsat. Both of these problems can be cured with the use of regenerative or positive feedback that cause the output V_0 to change faster and eliminate any false output transitions due to noise signals at the input. Inverting comparator with positive feedback . This is known as ―Schmitt Trigger‖.

Schmitt Trigger: [Square Circuit]





This circuit converts an irregular shaped waveform to a square wave or pulse. The

circuit is known as Schmitt Trigger or squaring circuit. The input voltage Vin triggers (changes the state of) the o/p V_0 every time it exceeds certain voltage levels called the upper threshold Vut and lower threshold voltage. These threshold voltages are obtained by using theh voltage divider R_1 – R_2, where the voltage across R_1 is feedback to the (+) input. The voltage across R_1 is variable reference threshold voltage that depends on the value of the output voltage. When V0 = +Vsat, the voltage across R1 is called ―upper threshold‖ voltage Vut. The input voltage Vin must be more positive than Vut in order to cause the output V0 to switch from +Vsat to –Vsat. As long as Vin < Vut , V0 is at +Vsat, using voltage divider rule, Similarly, when V0 = -Vsat, the voltage across R1 is called lower threshold voltage Vlt . the vin must be more negative than Vlt in order to cause V0 to switch from –Vsat to +Vsat. In other words,for Vin >Vlt ,V0 is at –Vsat. Vlt is given by the following eqn.Thus, if the threshold voltages Vut and Vlt are made larger than the input noise voltages, the positive feedback will eliminate the false o/p transitions. Also the positive feedback, because of its regenerative action, will make V0 switch faster between +Vsat and –Vsat. Resistance Rcomp t R1 || R2 is used to minimize the offset problems. The comparator with positive feedback is said to exhibit hysteresis, a dead band condition. (i.e) when the input of the comparator exceeds Vut its output switches from +Vsat to –Vsat and reverts to its original state, +Vsat when the input goes below Vlt. The hysteresis voltage is equal to the difference between Vut and Vlt. Therefore

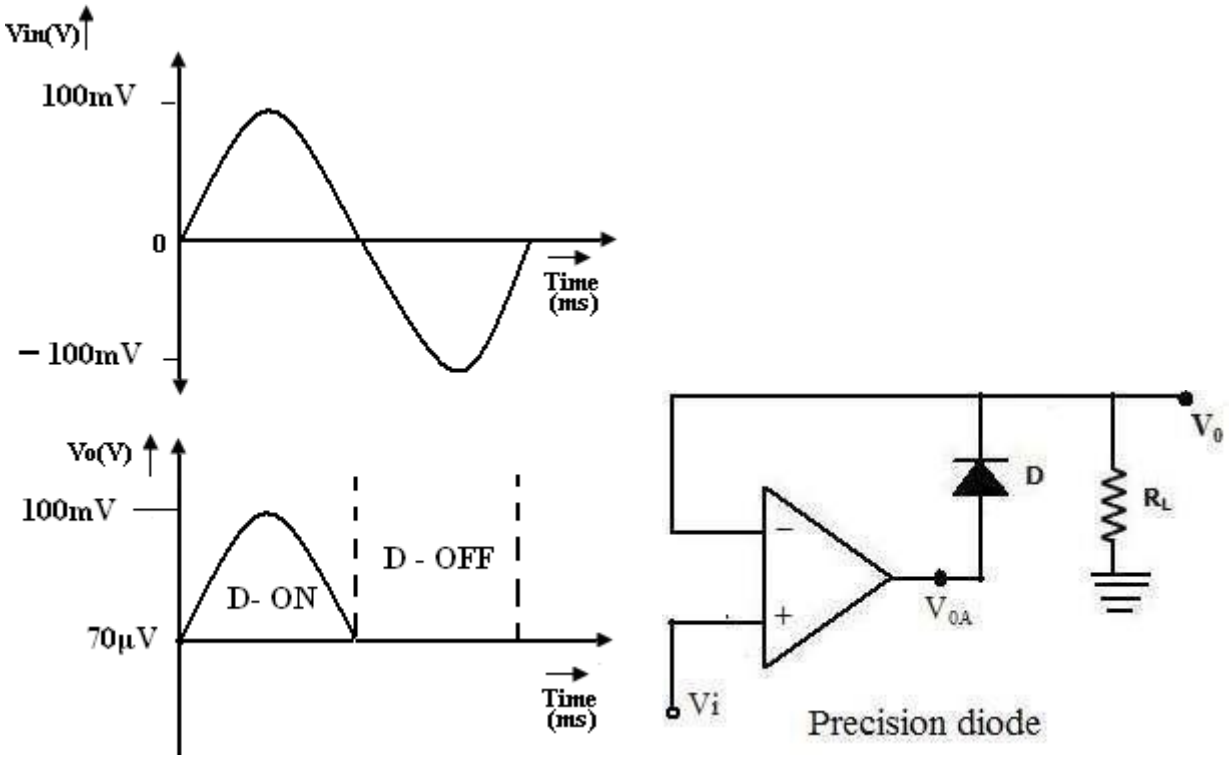
$$V_{ref} = V_{ut} - V_{lt} \quad V_{ref} = \frac{R_1}{R_1 + R_2}[+V_{sat} - (-V_{sat})]$$

Precision Rectifier:

The signal processing applications with very low voltage, current and power levels require rectifier circuits. The ordinary diodes cannot rectify voltages below the cut-in- voltage of the diode. A circuit which can act as an ideal diode or precision signal – processing rectifier circuit for rectifying voltages which are below the level of cut- in voltage of the diode can be designed by placing the diode in the feedback loop of an op-amp.

Precision diodes:

Figure shows the arrangement of a precision diode. It is a single diode arrangement and functions as a non- inverting precision half – wave rectifier circuit. If V_1 in the circuit of figure is positive, the op-amp output V_{OA} also becomes positive. Then the closed loop condition is achieved for the op-amp and the output voltage $V_0 = V_i$. when $V_i < 0$, the voltage V_{0A} becomes negative and the diode is reverse biased. The loop is then broken and the output $V_0 = 0$.



Input and Output Waveform

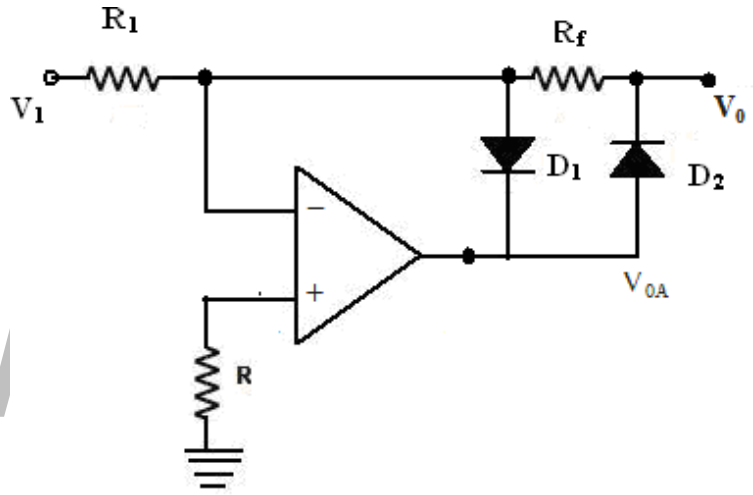
Consider the open loop gain A_{OL} of the op-amp is approximately 10^4 and the cut- in voltage V_γ for silicon diode is ≈ 0.7V. When the input voltage $V_i > V_\gamma / A_{OL}$, the output of the op-amp V_{OA} exceeds V_γ and the diode D conducts. Then the circuit acts like a voltage follower for input voltage level $V_i > V_\gamma / A_{OL}$,(i.e. when $V_i > 0.7/10^4 = 70\mu V$), and the output voltage V_0 follows the input voltage during the positive half cycle for input voltages higher than 70µV as shown in figure. When V_i is negative or less than V_γ / A_{OL}, the output of op-amp V_{OA} becomes negative, and the diode becomes reverse biased. The loop is then broken, and the op-amp swings down to negative saturation. However, the output terminal is now isolated from both the input signal and the output of the op-amp terminal thus $V_0 = 0$. No current is then delivered to the load R_L except for the small bias current of the op-amp and the reverse saturation current of the diode.

This circuit is an example of a non- linear circuit, in which linear operation is achieved over the remaining region ($V_i < 0$). Since the output swings to negative saturation level when $V_i < 0$, the circuit is basically of saturating form. Thus the frequency response is also limited. The precision diodes are used in half wave rectifier, Full-wave rectifier, peak value detector, clipper and clamper circuits.

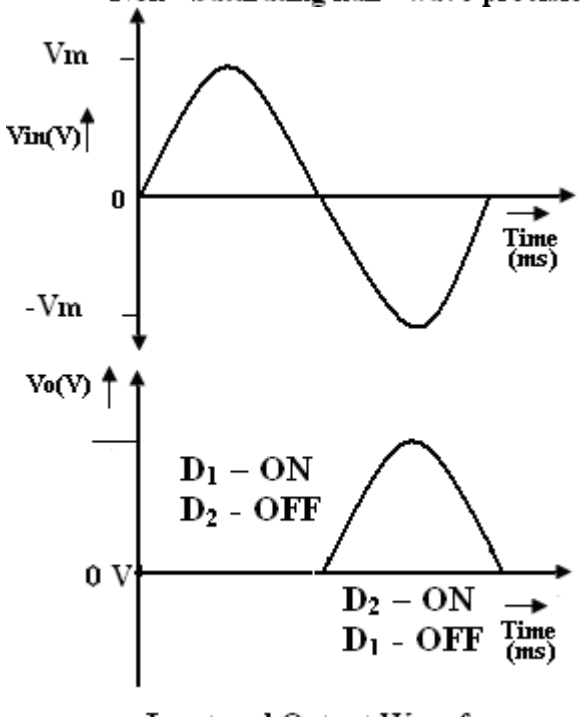
It can be observed that the precision diode as shown in figure operated in the first quadrant with $V_i > 0$ and $V_0 > 0$. The operation in third quadrant can be achieved by connecting the diode in reverse direction.

Half – wave Rectifier:

A non-saturating half wave precision rectifier circuit is shown in figure. When $V_i > 0V$, the voltage at the inverting input becomes positive, forcing the output V_{OA} to go negative. This results in forward biasing the diode D_1 and the op-amp output drops only by ≈ 0.7V below the inverting input voltage. Diode D_2 becomes reverse biased. The output voltage V_0 is zero when the input is positive. When $V_i > 0$, the op-amp output V_{OA} becomes positive, forward biasing the diode D_2 and reverse biasing the diode D_1 . The circuit then acts like an inverting amplifier circuit with a non-linear diode in the forward path. The gain of the circuit is unity when $R_f = R_i$.



Non - Saturating half - wave precision rectifier circuit



Input and Output Waveforms

The circuit operation can mathematically be expressed as

$V_0 = 0 \text{ when } V_i > 0$

and

$V_0 = -\frac{R}{R_i} V_i \text{ for } V_i < 0$

The voltage V_{OA} at the op @amp output is

$V_{OA} = 0.7 + V_i \text{ for } V_i > 0 \text{ and}$

$V_{OA} = -\frac{R}{R_i} V_i - 0.7 \text{ for } V_i < 0$

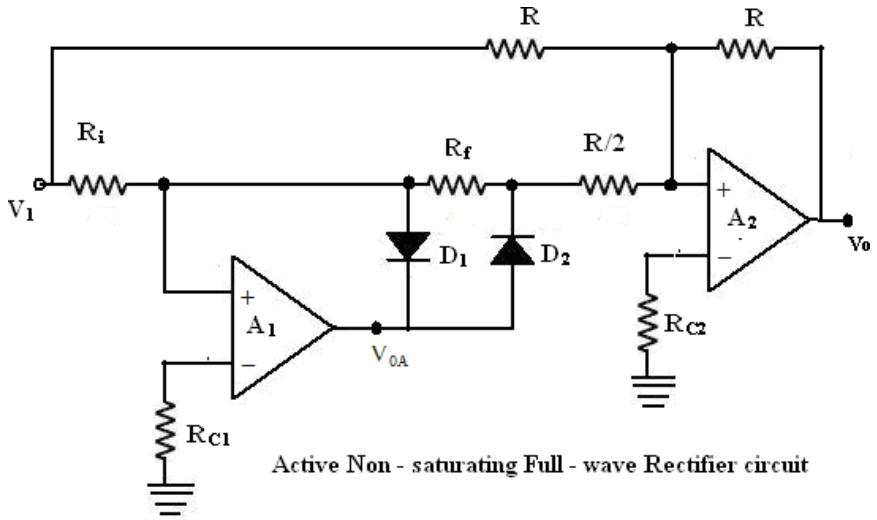
The input and output waveforms are shown in figure. The op-amp shown in the circuit must be a high speed op-amp. This accommodates the abrupt changes in the value of V_{OA} when V_i changes sign and improves the frequency response characteristics of the circuit.

The advantages of half wave rectifier are it is a precision half wave rectifier and it is a non saturating one.

The inverting characteristics of the output V_0 can be circumvented by the use of an additional inversion for achieving a positive output.

Full wave Rectifier:

The Full wave Rectifier circuit commonly used an absolute value circuit is shown in figure. The first part of the total circuit is a half wave rectifier circuit considered earlier in figure. The second part of the circuit is an inverting



Active Non - saturating Full - wave Rectifier circuit

.For positive input voltage $V_i > 0V$ and assuming that $R_F = R_i = R$, the output voltage $V_{OA} = V_i$. Thevoltage V_0 appears as (-) input to the summing op-amp circuit formed by A_2, The gain for the input V'_0 is R/(R/2), as shown in figure. The input V_i also appears as an input to the summing amplifier. Then, the net output is $V_0 = -V_i - 2V'_0$

$= -V_i - 2(-V_i) = V_i$

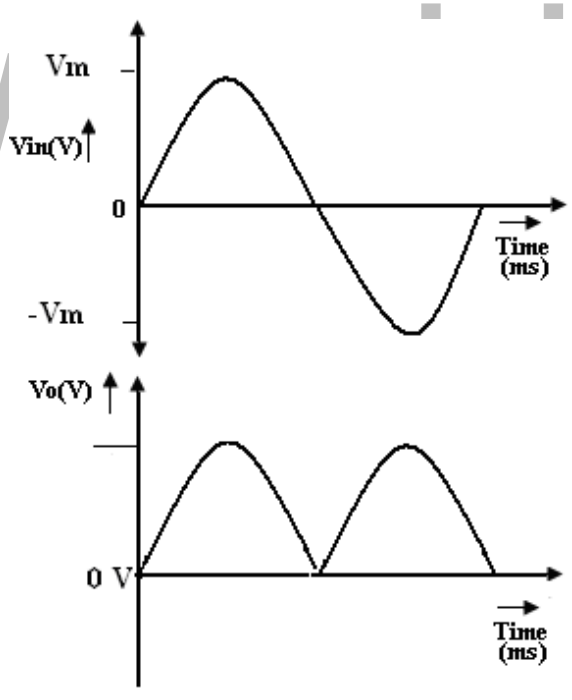
Since $V_i > 0V$, V'_0 will be positive, with its input output characteristics in first quadrant. For negative input $V_i < 0V$, the output V'_0 of the first part of rectifier circuit is zero. Thus, one input of the summing circuit has a value of zero. However, V_i is also applied as an input to the summer circuit formed by the op-amp A_2. The gain for this input id (-R/R) = -1, and hence the output is $V_0 = -V_i$. Since V_i is negative, v_0 will be inverted and will thus be positive. This corresponds to the second quadrant of the circuit.

To summarize the operation of the circuit,

$V_0 = V_i$ when $V_i < 0V$ and $V_0 = V_i$ for $V_i > 0V$, and hence $V_0 = |V_i|$

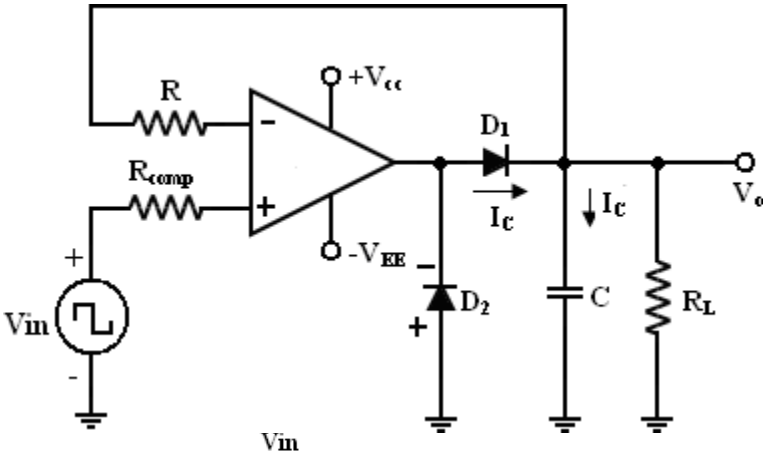
It can be observed that this circuit is of non-saturating form. The input and output waveforms are shown in the figure.

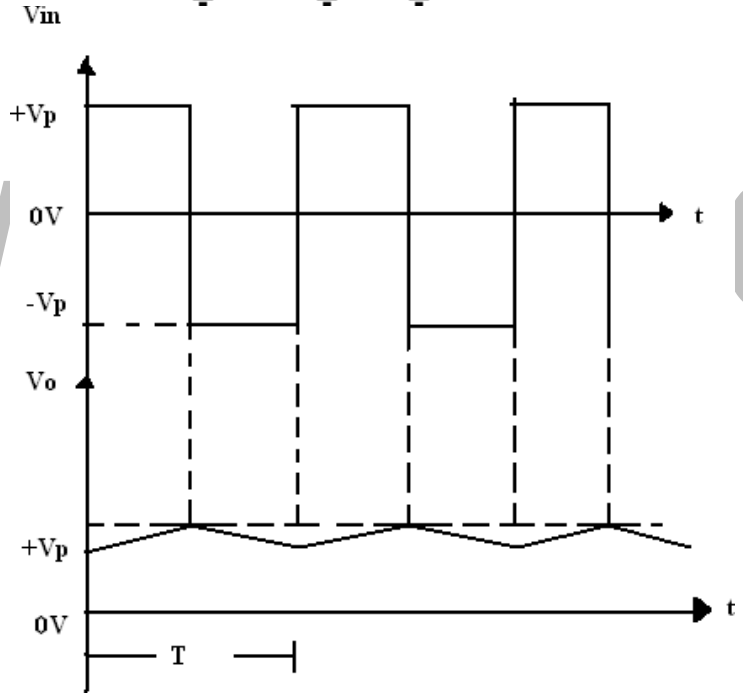
Peak detector:



Input and Output Waveforms

Square, Triangular, Sawtooth and pulse waves are typical examples of non-sinusoidal waveforms. A conventional ac voltmeter cannot be used to measure these sinusoidal waveforms because it is designed to measure the rms value of the pure sine wave. One possible solution to this problem is to measure the peak values of the non-sinusoidal waveforms. Peak detector measures the +ve peak value of the square wave input.





i) During the positive half cycle of Vin:

the o/p of the op-amp drives D_1 on. (Forward biased)

Charging capacitor C to the positive peak value V_p of the input volt Vin.

ii) During the negative half cycle of Vin:

D_1 is reverse biased and voltage across C is retained. The only discharge path for C isthrough R_L. since the input bias I_B is negligible.

For proper operation of the circuit, the charging time constant (CR_d) and discharging time constant(CR_L) must satisfy the following condition.

$CR_d <= T/10$ ----------(1)

Where R_d = Resistance of the forward-biased diode.

T = time period of the input waveform.

$CR_L >= 10T$ ----------(2)

Where R_L = load resistor. If R_L is very small so that eqn (2) cannot be satisfied.

Use a (buffer)voltage follower circuit between capacitor C and R_L load resistor.

R = is used to protect the op-amp against the excessive discharge currents.

Rcomp = minimizes the offset problems caused by input current

D2 = conducts during the –ve half cycle of Vin and prevents the op-amp from going into negative saturation.

Note: -ve peak of the input signal can be detected simply by reversing diode D_1 and D_2 .

Differentiator:

One of the simplest of the op-amp circuits that contains capacitor in the differentiating amplifier.

Differentiator:

As the name implies, the circuit performs the mathematical operation of differentiation (i.e) the output waveform is the derivative of the input waveform. The differentiator may be constructed from a basic inverting amplifier if an input resistor R_1 is replaced by a capacitor C_1 .

The expression for the output voltage can be obtained KCL eqn written at node V_2 as follows,

Since the differentiator performs the reverse of the integrator function.

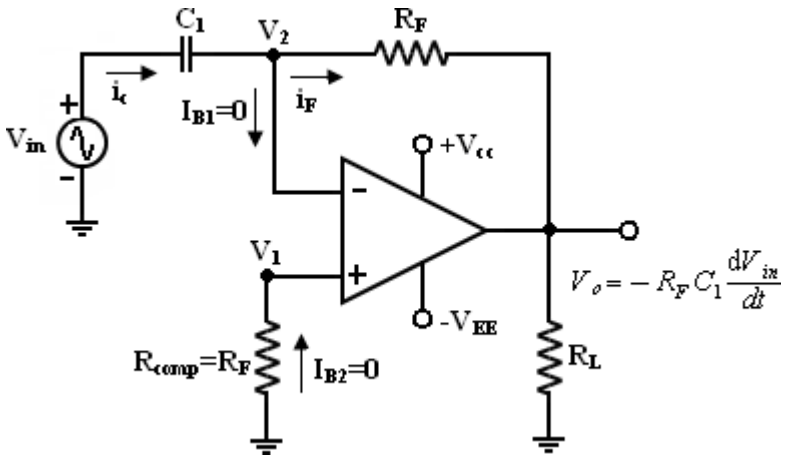
Thus the output V_0 is equal to $R_F C_1$ times the negative rate of change of the input voltage Vin with time.

The –sign => indicates a 180^0 phase shift of the output waveform V_0 with respect to the input signal.

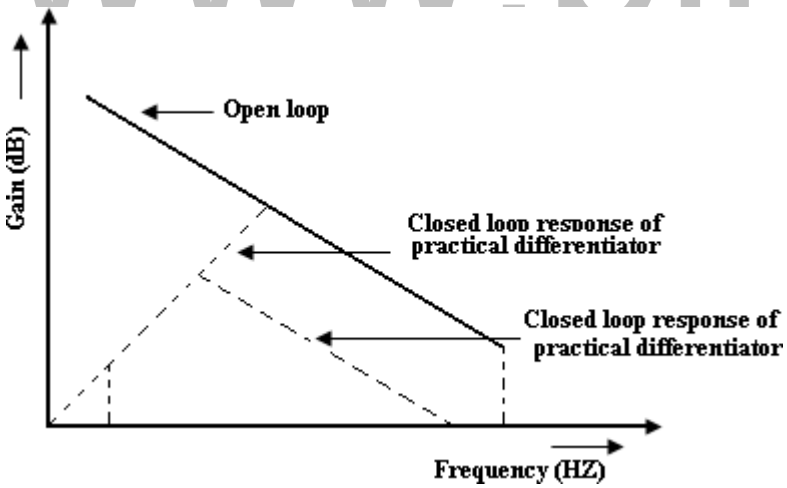
The below circuit will not do this because it has some practical problems.

The gain of the circuit (R_F/XC_1) R with R in frequency at a rate of 20dB/decade. This makes the circuit unstable.

Also input impedance XC_1 Swith Rin frequency which makes the circuit very susceptible to high frequency noise.



Basic Differetntiator



From the above fig, f_a = frequency at which the gain is 0dB and is given by,

Both stability and high frequency noise problems can be corrected by the addition of 2 components. R_1 and C_F. This circuit is a practicaldifferentiator.

From Frequency f to feedback the gain Rsat 20dB/decade after feedback the gain S at 20dB/decade. This 40dB/ decade change in gain is caused by the $R_1 C_1$ and $R_F C_F$ combinations. The gain limiting frequency f_b is given by,

Where $R_1 C_1 = R_F C_F$

$R_1 C_1$ and $R_F C_F$ => helps to reduce the effect of high frequency input, amplifier noise and offsets.

All $R_1 C_1$ and $R_F C_F$ make the circuit more stable by preventing the Rin gain with frequency.

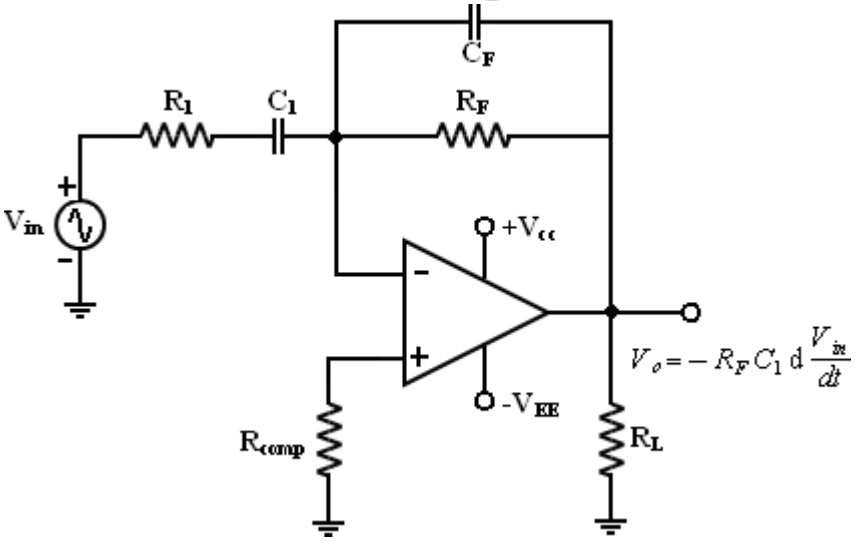
Generally, the value of Feedback and in turn $R_1 C_1$ and $R_F C_F$ values should be selected such that

$$f_a < f_b < f_C$$

where

f_c – *unity gain bandwidth*

The input signal will be differentiated properly, if the time period T of the input signal is larger than or equal to $R_F C_1$ (i.e) $T > R_F C_1$



Practical Differentiator

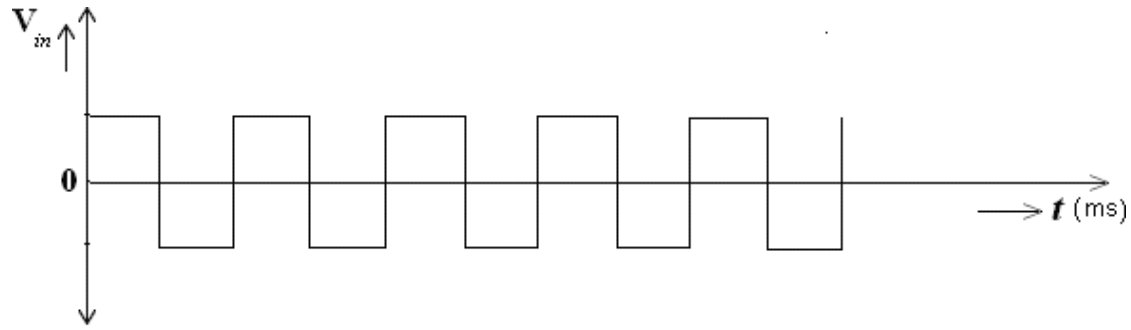
A workable differentiator can be designed by implementing the following steps.

1. Select fa equal to the highest frequency of the input signal to be differentiated then assuming a value of $C_1 < 1\mu f$. Calculate the value of R_F.

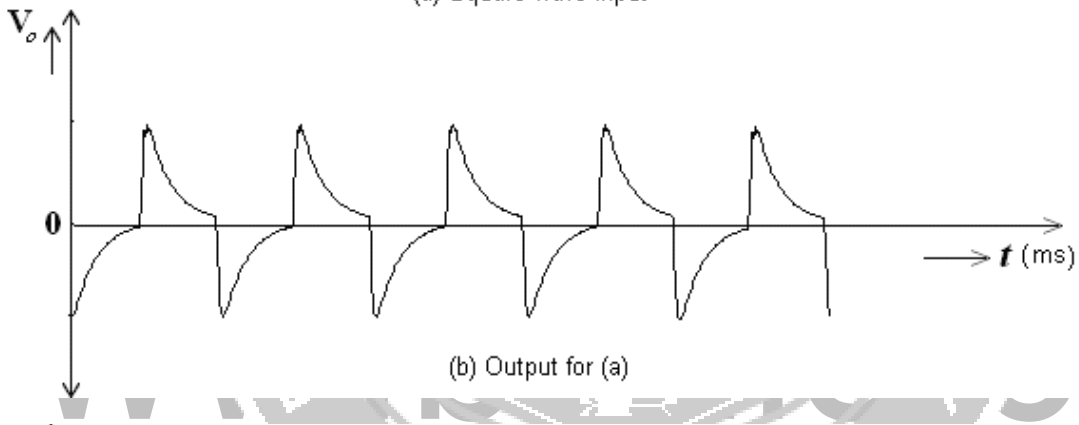
2. Choose fb = 20fa and calculate the values of R_1 and C_F so that $R_1 C_1 = R_F C_F$.

Uses:

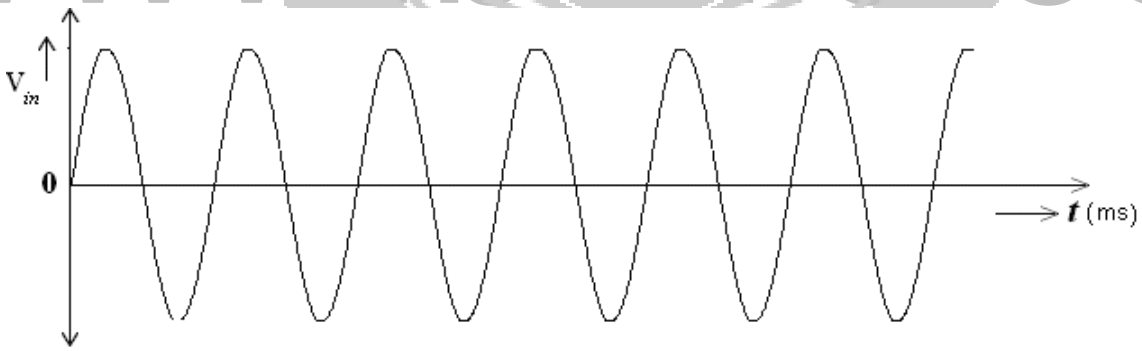
Its used in waveshaping circuits to detect high frequency components in an input signal and also as a rate of change and detector in FM modulators.



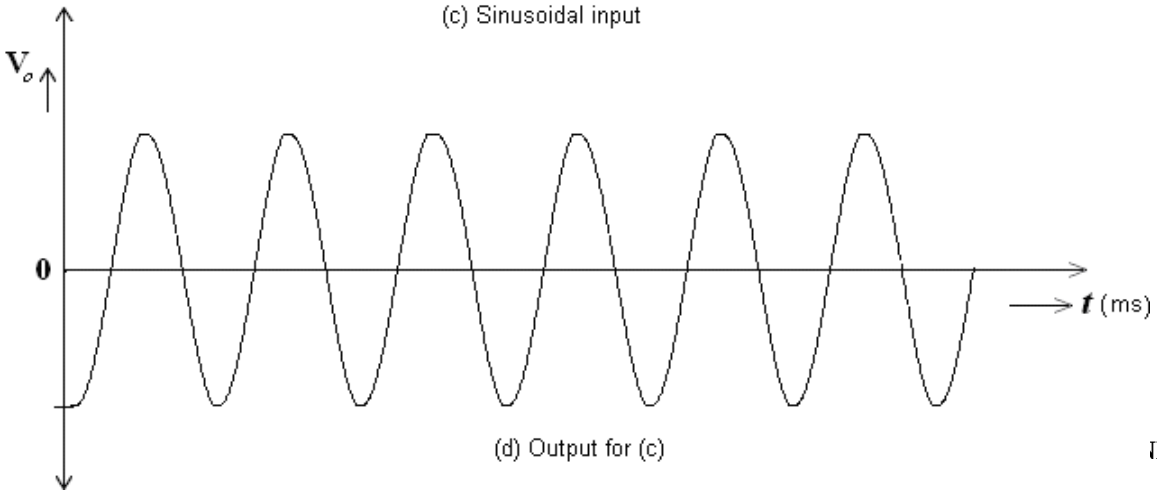
(a) Square wave input



(b) Output for (a)



(c) Sinusoidal input



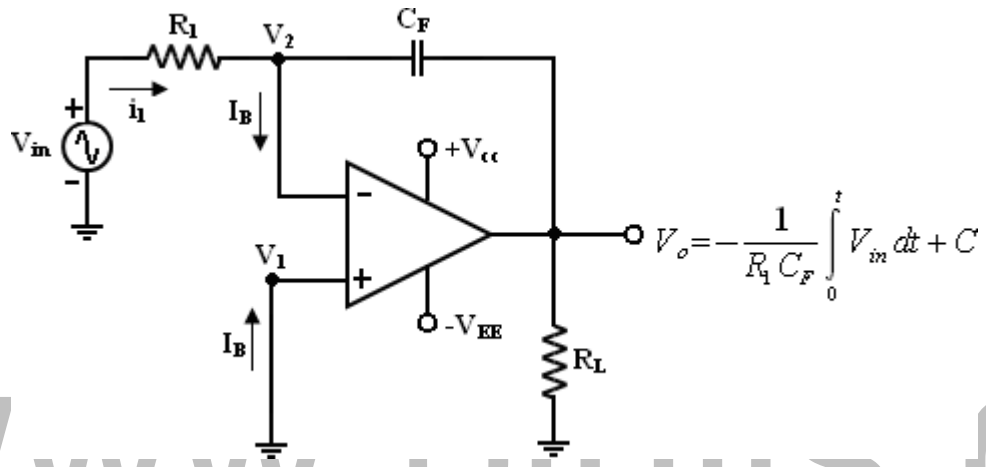
(d) Output for (c)

This o/p for practical differentiator.

Integrator:

A circuit in which the output voltage waveform is the integral of the input voltage waveform is the integrator or Integration Amplifier. Such a circuit is obtained by using a basic inverting amplifier configuration if the feedback resistor R_F is replaced by a capacitor C_F .

The expression for the output voltage V_0 can be obtained by KVL eqn at node V_2.



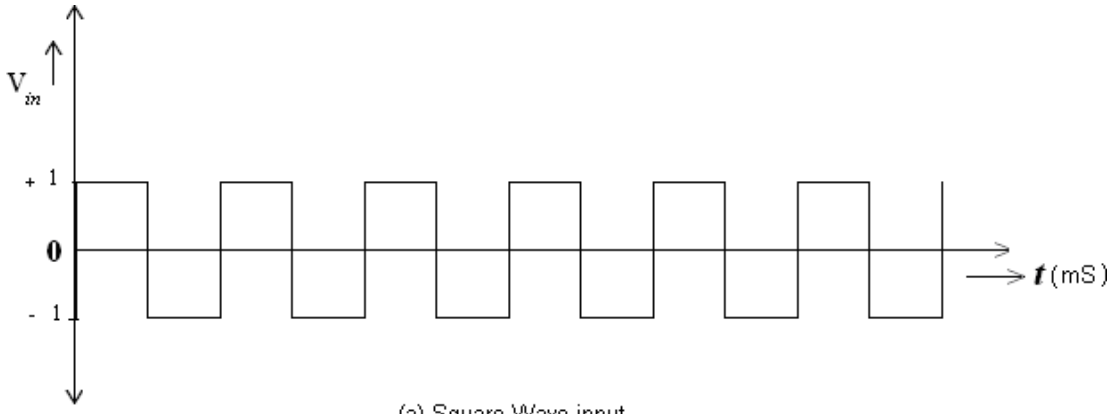
a

where C @integration constant A

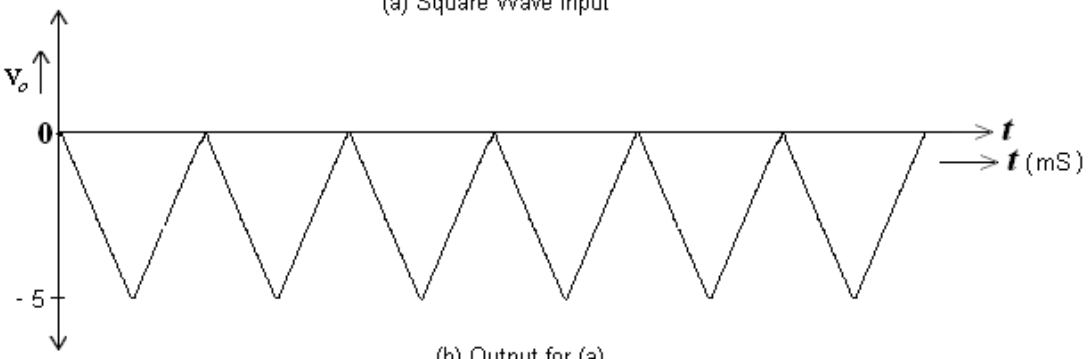
eqn (3) indicates that the output is directly proportional to the negative integral of the input volts and inversely proportional to the time constant $R_1 C_F$.

Ex: If the input is sine wave -> output is cosine wave.

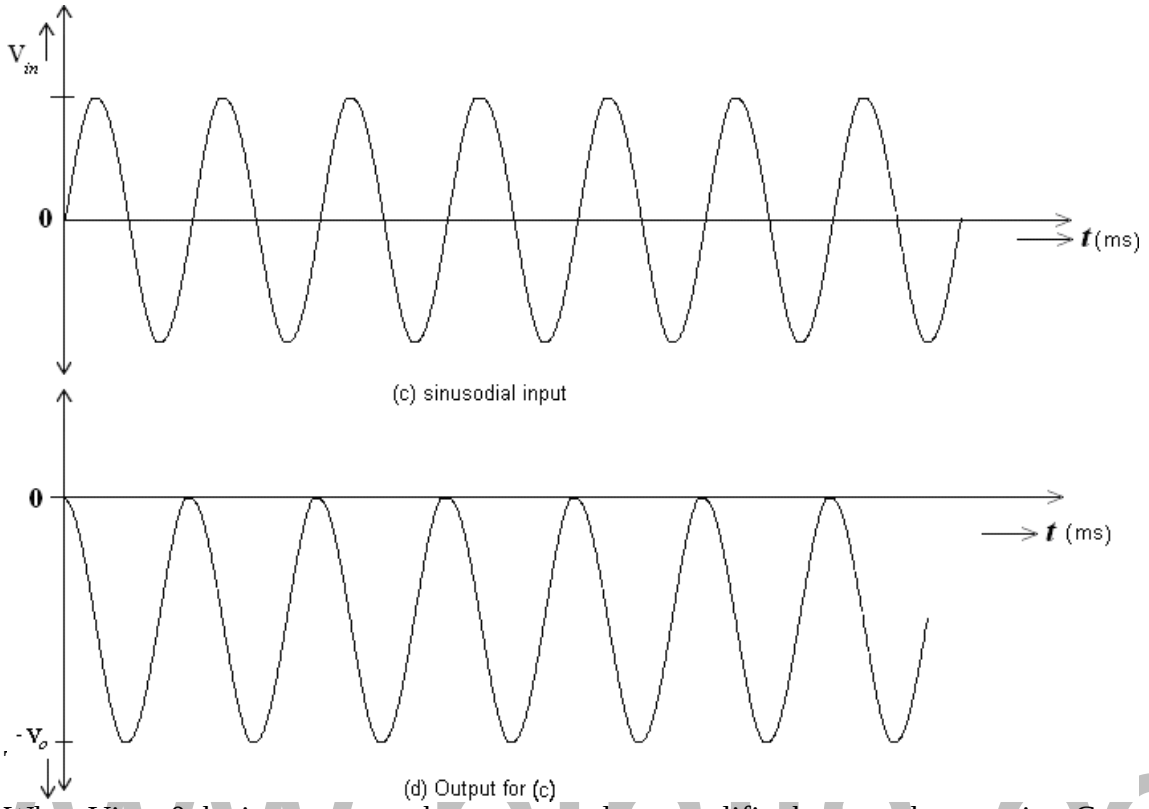
If the input is square wave -> output is triangular wave.



(a) Square Wave input



(b) Output for (a)

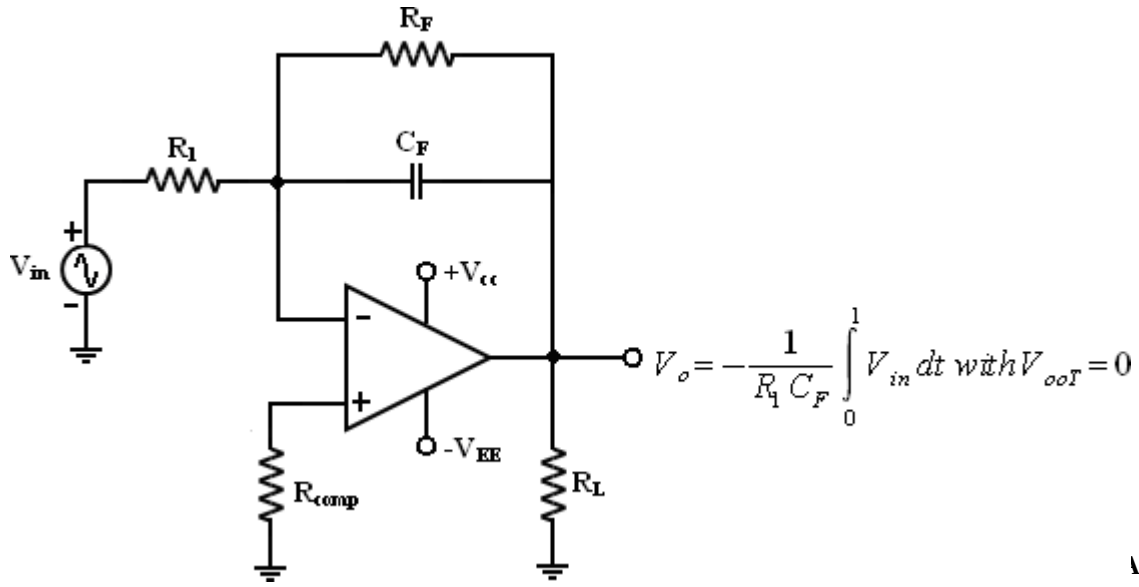


When Vin = 0 the integrator works as an open loop amplifier because the capacitor C_F acts an open circuit to the input offset voltage Vio.

Or

The Input offset voltage Vio and the part of the input are charging capacitor C_F produce the error voltage at the output of the integrator.

Practical Integrator:



Practical Integrator to reduce the error voltage at the output, a resistor R_F is connected across the feedback capacitor C_F .

Thus R_F limits the low frequency gain and hence minimizes the variations in the output voltages. The frequency response of the basic integrator, shown from this fb is the frequency at which the gain is dB and is given by,

Both the stability and low frequency roll-off problems can be corrected by the addition of a resistorR_F in the practical integrator.

Stability -> refers to a constant gain as frequency of an input signal is varied over a certain range.Low frequency -> refers to the rate of decrease in gain roll off at lower frequencies.

From the fig of practical Integrators,

f is some relative operating frequency and for frequencies f to fa to gain R_F / R_1 is constant. After fa the gain decreases at a rate of 20dB/decade or between fa and fb the circuit act as an integrator.Generally the value of fa and in turn $R_1 C_F$ and $R_F C_F$ values should be selected such that fa<fb.

In fact, the input signal will be integrated properly if the time period T of the signal is larger thanor

equal to $R_F C_F$, (i.e)

` a

$$T \geq R_F C_F @@@@6$$

Uses:

Most commonly used in analog

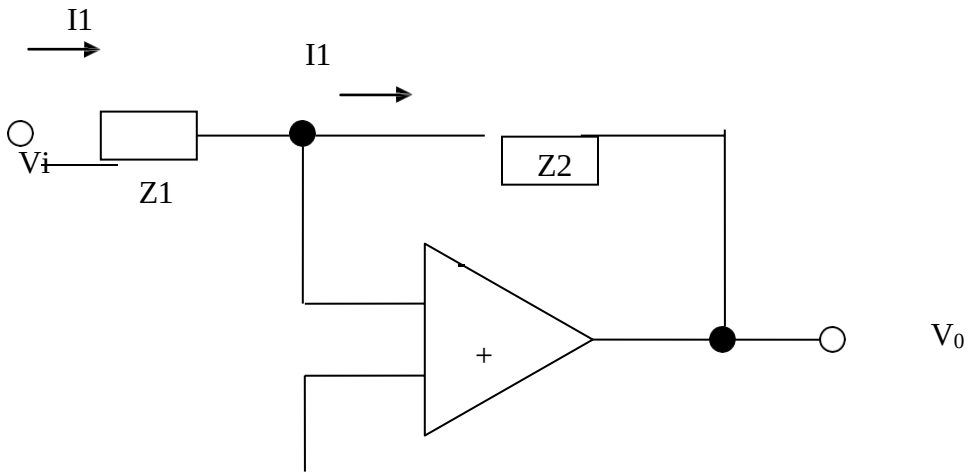
computers.ADC

Signal wave shaping circuits.

UNIT – III

APPLICATIONS OF OPERATIONAL AMPLIFIER

SIGN CHANGER (PHASE INVERTER)



The basic inverting amplifier configuration using an op-amp with input impedance Z_1 and feedback impedance Z_f.

If the impedance Z_1 and Z_f are equal in magnitude and phase, then the closed loop voltage gain is -1,and the input signal will undergo a 180^0 phase shift at the output. Hence, such circuit is also called phase inverter. If two such amplifiers are connected in cascade, then the output fromthe second stage is the same as the input signal without any change of sign.

Hence, the outputs from the two stages are equal in magnitude but opposite in phase and such a system is an excellent paraphase amplifier.

Scale Changer:

Referring the above diagram, if the ratio $Z_f / Z_1 = k$, a real constant, then the closed loop gain is –k, and the input voltage is multiplied by a factor –k and the scaled output is available at the output. Usually, in such applications, Z_f and Z_1 are selected as precision resistors for obtaining precise and scaled value of input voltage.

PHASE SHIFT CIRCUITS

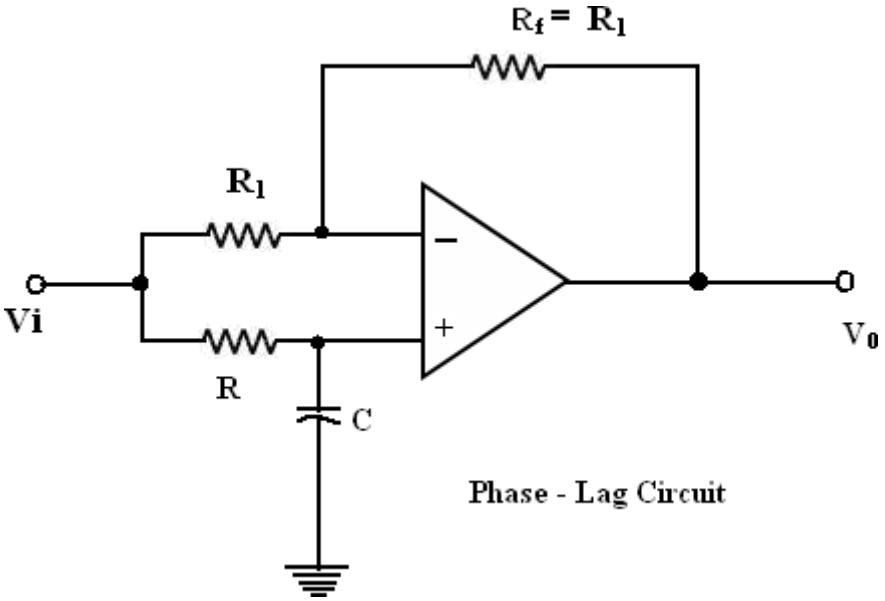
The phase shift circuits produce phase shifts that depend on the frequency and maintain a constant gain. These circuits are also called constant-delay filters or all-pass filters. That constant delay refers to the fact the time difference between input and output remains constant when frequency is changed over a range of operating frequencies.

This is called all-pass because normally a constant gain is maintained for all the frequencies within the operating range. The two types of circuits, for lagging phase angles and leading phase angles.

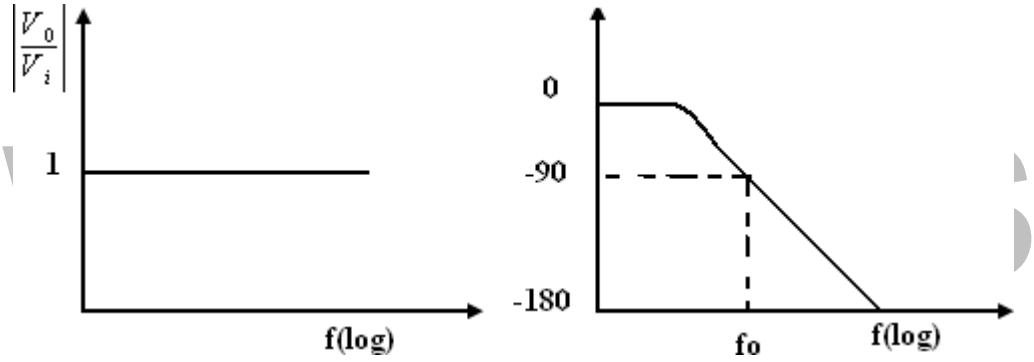
Phase-lag circuit:

Phase log circuit is constructed using an op-amp, connected in both inverting and non inverting modes. To analyze the circuit operation, it is assumed that the input voltage v1 drives a simple inverting amplifier with inverting input applied at(-)terminal of op-amp and a non inverting amplifier with a low-pass filter.

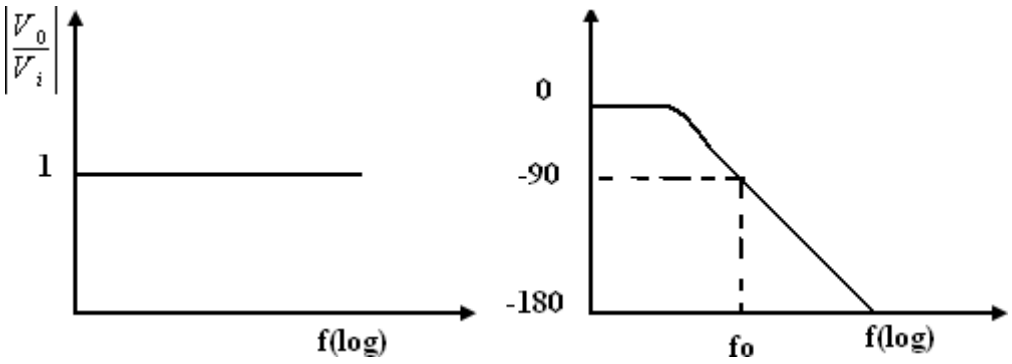
It is also assumed that inverting gain is -1 and non- inverting gain after the low-pass circuit is $1 + \frac{R_f}{R_1} = 1+1=2$, Since $R_f = R_1$



Phase - Lag Circuit



The relationship is complex as defined above equation and it shows that it has both magnitude and phase. Since the numerator and denominator are complex conjugates, their



Voltage follower:

If $R_1=\infty$ and Rf=0 in the non inverting amplifier configuration .

The amplifier act as a unity-gain amplifier or voltage follower.

That is

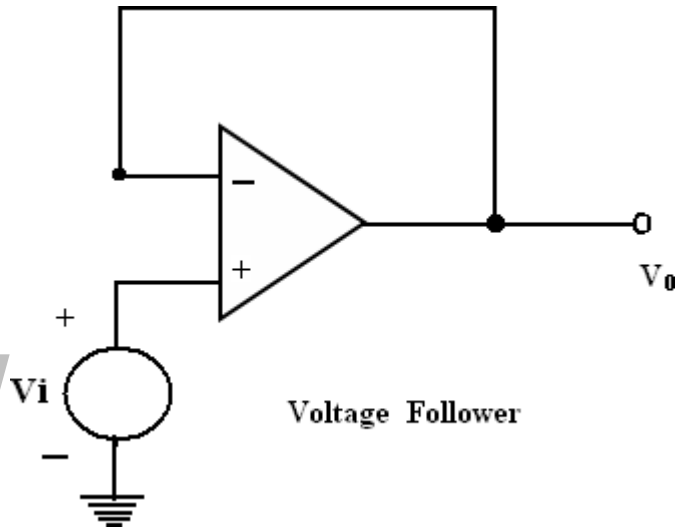
$$A_v = 1 + \frac{R_f}{R_1}$$

Since $\frac{R_f}{R_1} = 0 \Rightarrow A_v = 1$

The circuit consist of an op-amp and a wire connecting the output voltage to the input ,i.e the output voltage is equal to the input voltage, both in magnitude and phase.$V_0=V_i$

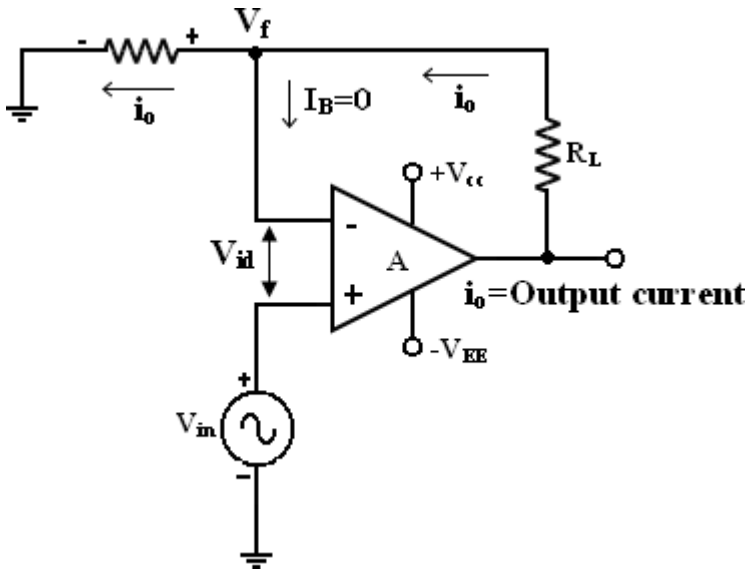
Since the output voltage of the circuit follows the input voltage, the circuit is called voltage follower. It offers very high input impedance of the order of MΩ and very low output impedance.

Therefore, this circuit draws negligible current from the source. Thus, the voltage follower can be used as a buffer between a high impedance source and a low impedance load for impedance matching applications.



Voltage to Current Converter with floating loads (V/I):

1. Voltage to current converter in which load resistor R_L is floating (not connected to ground).
2. Vin is applied to the non inverting input terminal, and the feedback voltage across R_1 devices the inverting input terminal.
3. This circuit is also called as a current – series negative feedback amplifier.
4. Because the feedback voltage across R_1 (applied Non- inverting terminal) depends on the output current i_0 and is in series with the input difference voltage V_{id}.



Writing KVL for the input loop,

$Vin \quad V_{id} \quad V_f$

V_{id} t 0*v , since A is very large* A

$Vin \quad V_f$ ` a

$Vin \quad R_1$ *or*

i_0

From the fig input voltage Vin is converted into output current of Vin/R_1 [Vin -> i_0] . In other words, input volt appears across R_1. If R_1 is a precision resistor, the output current ($i_0 = Vin/R_1$) will be precisely fixed.

Applications:

1. Low voltage ac and dc voltmeters
2. Diode match finders
3. LED
4. Zener diode testers.

SWITCHES FOR DAC

The Switches which connects the digital binary input to the nodes of a D/A converter is an electronic switch. Although switches can be made of using diodes, Bipolar junction Transistors, Field Effect transistors or MOSFETs, there are four main configuratio ns used as switches for DACs. They are

i) Switches using overdriven Emitter Followers.

ii) Switches using MOS Transistor- Totem pole MOSFET Switch and CMOS Inverter Switch.

i) CMOS switch for Multiplying type DACs .iv)

CMOS Transmission gate switches.

These configurations are used to ensure the high speed switching operations for different types of DACs.

Switches using overdriven Emitter Followers:

The bipolar transistors have a negligible resistance when they are operated in saturation. The bipolar transistor operating in saturation region indicates a minimum resistance and thus represents ON condition. When they are operating in cut-off region indicates a maximum resistance and thus represents OFF condition.

The circuit shown here is the arrangement of two transistors connected as emitter followers. A silicon transistor operating in saturation will have a offset voltage of 0.2V dropped across them. To have a zero offset voltage condition, the transistors must be overdriven because the saturation factor becomes negative. The two transistors Q_1(NPN) and Q_2(PNP) acts as a double pole switch. The bases of the transistors are driven by +5.75V and -5.75V.

Case 1:

When $V_{B1} = V_{B2} = +5.75V$, Q_1 is in saturation and Q_2 is OFF. And $V_E \approx 5V$ with

$V_{BE1} = V_{BE2} = 0.75V$

Case 2:

When $V_{B1} = V_{B2} = -5.75V$, Q_2 is in saturation and Q_1 is OFF. And $V_E \approx -5V$ with

$V_{BE1} = V_{BE2} = 0.75V$

Thus the terminal B of the resistor R_e is connected to either -5V or +5V depending on the input bit.

Switches using MOS transistor:

Totem pole MOSFET Switch:

As shown in the figure, the totem pole MOSFET Switch is connected in series with resistors of R-2R network. The MOSFET driver is connected to the inverting terminal of the summing op-amp.The complementary outputs *Q* and *Q* drive the gates of the MOSFET M_1 and M_2 respectively. The SR flipflop holds one bit of digital information of the binary word under conversion. Assuming the negative logic (-5V for logic 1 and +5V for logic 0) the operation is given as two cases.

Case 1:

When the bit line is 1 with S=1 and R=0 makes *Q*=1 and *Q* =0. This makes the transistor M_1 ON,thereby connecting the resistor R to reference voltage $-V_R$. The transistor M_2 remains in OFF condition.

Case 2:

When the bit line is 0 with S=0 and R=1 makes *Q*=0 and *Q* =1. This makes the transistor M_2 ON,thereby connecting the resistor R to Ground. The transistor M_1 remains in OFF condition.

CMOS Inverter Switch:

The figure of CMOS inverter is shown here. It consists of a CMOS inverter connected with an op- amp acting as a buffer. The buffer drives the resistor R with a very low output impedance. Assuming positive logic (+5V for logic 1 and 0V for logic 0), the operation can be explained in two cases.

Case1:

When the complement of the bit line *Q* is low, M_1 becomes ON connecting V_R to the non-inverting input of the op-amp. This drives the resistor R HIGH.

Case2:

When the complement of the bit line *Q* ~~is~~ high, M_2 becomes ON connecting Ground to the non-inverting input of the op-amp. This pulls the resistor R LOW (to ground).

CMOS switch for Multiplying type DACs:

The circuit diagram of CMOS Switch is shown here. The heart of the switching element is formed by transistors M_1 and M_2. The remaining transistors accept TTl or CMOS compatible logic inputs and provides the anti-phase gate drives for the transistors M_1 and M_2. The operation for the two cases is as follows.

Case 1:

When the logic input is 1, M_1 is ON and M_2 is OFF. Thus current I_K is diverted to Io‘ bus.

Case 2:

When the logic input is 0, M_2 is ON and M_1 is OFF. Thus current I_K is diverted to Io bus.

CMOS Transmission gate switches:

The disadvantage of using individual NMOS and PMOS transistors are threshold voltage drop(NMOS transistor passing only minimum voltage of VR - VTH and PMOS transistor passing minimum voltage of VTH). This is eliminated by using transmission gates which uses a parallel connection of both NMOS and PMOS. The arrangement shown here can pass voltages from VR to 0V acting as a ideal switch. The following cases explain the operation.

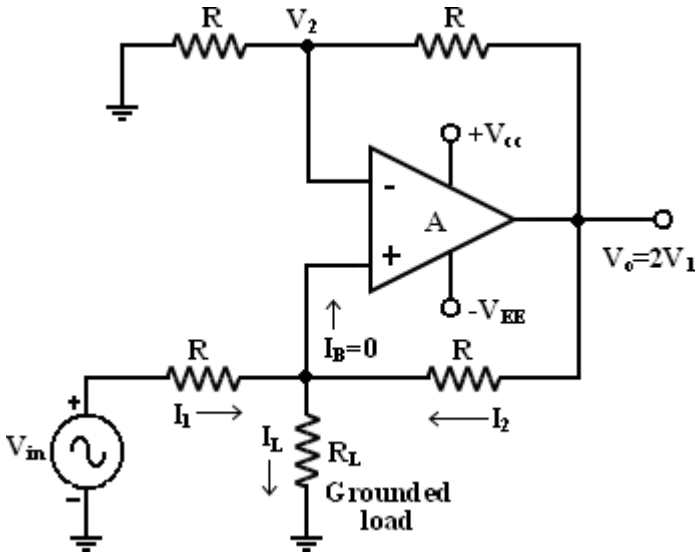
Case 1:

When the bit-line b_k is HIGH, both transistors M_n and M_p are ON, offering low resistance over theentire range of bit voltages.

Case 2: When the bit-line b_k is LOW, both the transistors are OFF, and the signal transmission is inhibited (Withdrawn).Thus the NMOS offers low resistance in the lower portion of the signal and PMOS offers low resistance in the upper portion of the signal. As a combination, they offer a low parallel resistance throughout the operating range of voltage. Wide varieties of these kinds of switches were available. Example: CD4066 and CD4051.

Voltage – to current converter with Grounded load:

This is the other type V – I converter, in which one terminal of the load is connected to ground.



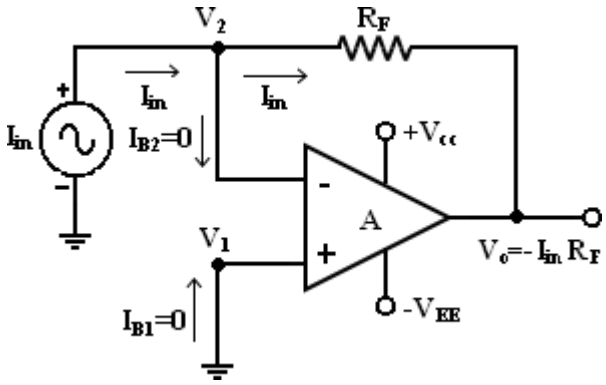
Analysis of the circuit:

The analysis of the circuit can be done by following 2 steps.

1. To determine the voltage V_1 at the non- inverting (+) terminals and
2. To establish relationship between V_1 and the load current I_L .

Applying KCL at node V_1 we can write that,

Current to Voltage Converter (I –V):

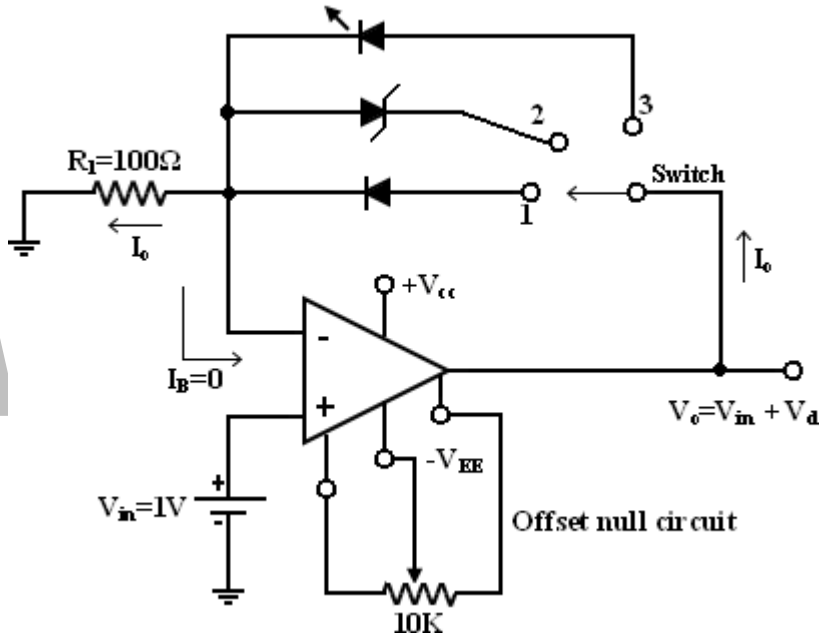


Sensitivity of the I – V converter:

1. The output voltage $V_0 = -R_F I_{in}$.
2. Hence the gain of this converter is equal to $-R_F$. The magnitude of the gain (i.e) is also called as sensitivity of I to V converter.
3. The amount of change in output volt ΔV_0 for a given change in the input current ΔIin is decide by the sensitivity of I-V converter.
4. By keeping R_F variable, it is possible to vary the sensitivity as per the requirements.

Applications of V-I converter with Floating Load:

1. Diode Match finder:



In some applications, it is necessary to have matched diodes with equal voltage drops at a particular value of diode current. The circuit can be used in finding matched diodes and is obtained from fig (V-I converter with floating load) by replacing R_L with a diode. When the switch is in position 1: (Diode Match Finder) Rectifierr diode (IN 4001) is placed in the f/b loop, the current through this loop is set by input voltage Vin and Resistor R_1 . For Vin = 1V and $R_1 = 100\Omega$, the current through this

$I_0 = Vin/R_1 = 1/100 = 10mA.$

As long as V_0 and R_1 constant, I_0 will be constant. The Voltage drop across the diode can be found either by measuring the volt across it or o/p voltage. The output voltage is equal to (Vin + V_D) V_0

= Vin + V_D . To avoid an error in output voltage the op-amp should be initially nulled. Thus the matched diodes can be found by connecting diodes one after another in the feedback path and measuring voltage across them.

2. Ze ner diode Tester:

(When the switch position 2)

when the switch is in position 2, the circuit becomes a zener diode tester. The circuit can be used to find the breakdown voltage of zener diodes. The zener current is set at a constant value by Vin and R_1. If this current is larger than the knee current (I_{ZK}) of the zener, the zenerr blocks (V_z) volts.

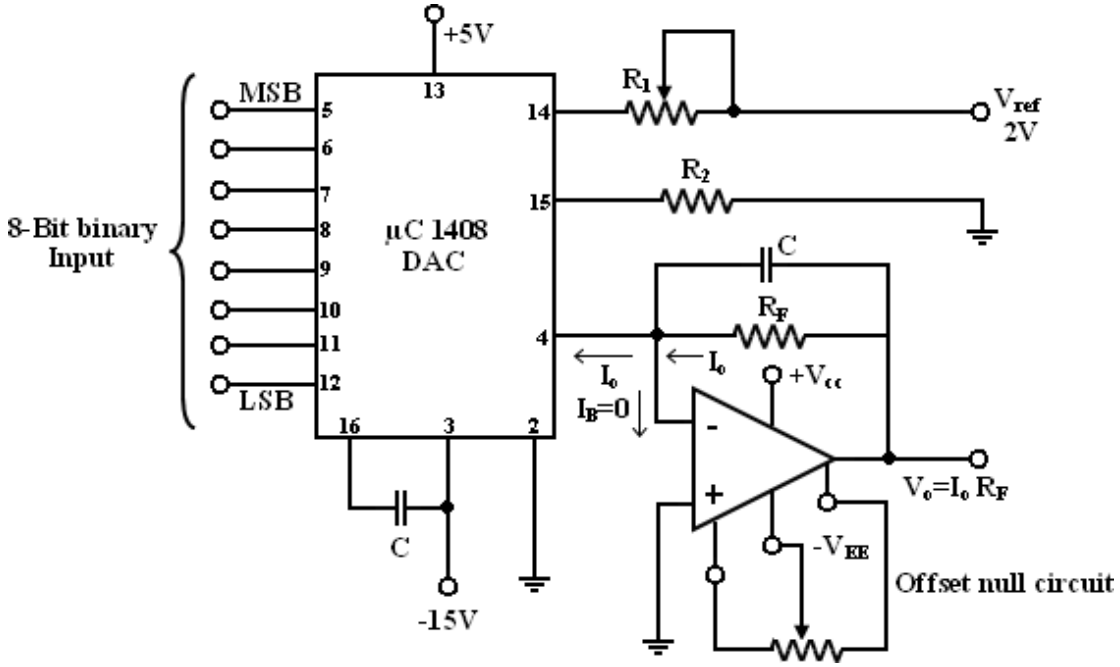
For Ex:

I_{ZK} = 1mA , V_Z = 6.2V, Vin = 1v , R_1 = 100Ω Since the current through the zener is , I_0 = Vin/R_1 = 1/100 =10mA > I_{ZK} the voltage across the zener will be approximately equal to 6.2V.

3. When the switch is in position 3: (LED)

The circuit becomes a LED when the switch is in position 3. LED current is set at a constant value by Vin and R_1. LEDs can be tested for brightness one after another at this current. Matched LEDs with equal brightness at a specific value of current are useful as indicates and display devices in digital applications.

Applications of I – V Converter:



One of the most common use of the current to voltage converter is

1. Digital to analog Converter (DAC)
2. Sensing current through Photodetector. Such as photocell, photodiodes and photovoltaic cells.

Photoconductive devices produce a current that is proportional to an incident energy or light (i.e) It can be used to detect the light.

1. DAC using I – V converter:

It shows a combination of a DAC and current to voltage converter. The 8 digit binary signal is the input to the DAC and V_0 is the corresponding analog output of the current to voltage converter. The outputu of the DAC is current I_0, the value of which depends on the logic state (0 or 1), of the binary inputs as indicated by the following eqn.

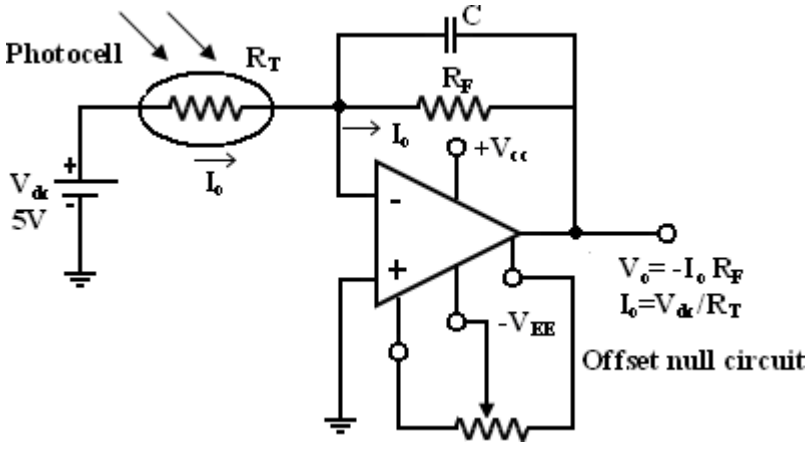
This means I_0 is zero when all inputs are logic 0.

I_0 is max when all inputs are logic 1.

The variations in I_0 can be converted into a desired o/p voltage range by selecting a proper value for R_F. since, $V_0 = I_0 R_F$

Where I_0 is given by eqn (1). It is common to parallel R_F with capacitance C to minimize the overshoot. In the fig the o/p voltage of the current to voltage converter is positive because the direction of input current I_0 is opposite to that in the basic I – V Converter.

2. Detecting current through photosensitive devices:



Photocells, photodiodes, photovoltaic cells give an output curren that depends on the intensity of light and independent of the load. The current through this devices can be converted to voltage by I – V converter and it can be used as a measure of the amount of light. In this fig photocell is connected to the I – V Converter. Photocell is a passive transducer, it requires an external dc voltage(Vdc). The dc voltage can be eliminated if a photovo ltaic cell is used instead of a photocell. The Photovoltaic Cell is a semiconductor device that converts the radiant energy to electrical power. It is a self generating circuit because it doesnot require dc voltage externally. Ex of Photovoltaic Cell : used in space applications and watches.

Summing Amplifier:

Op-amp may be used to design a circuit whose output is the sum of several input signals. Such a circuit is called a summing amplifier or a summer.

An inverting summer or a non- inverting summer may be discussed now.

Inverting Summing Amplifier:

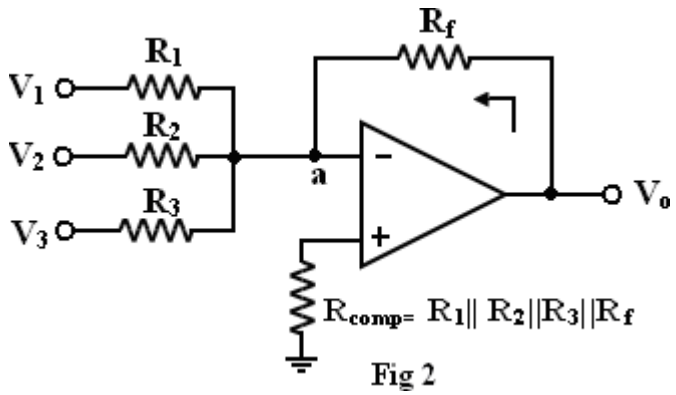


Fig 2

A typical summing amplifier with three input voltages V_1, V_2 and V_3 three input resistors R_1, R_2, R_3 and a feedback resistor R_f is shown in figure 2.

The following analysis is carried out assuming that the op-amp is an ideal one, that is, $A_{OL} = \infty$. Since the input bias current is assumed to be zero, there is no voltage drop across the resistor R_{comp} and hence the non- inverting input terminal is at ground potential.

To find R_{comp}, make all inputs $V_1 = V_2 = V_3 = 0$. So the effective input resistance $R_i = R_1 \| R_2 \| R_3$. Therefore, $R_{comp} = R_i \| R_f = R_1 \| R_2 \| R_3 \| R_{,f}$.

Non-Inverting Summing Amplifier:

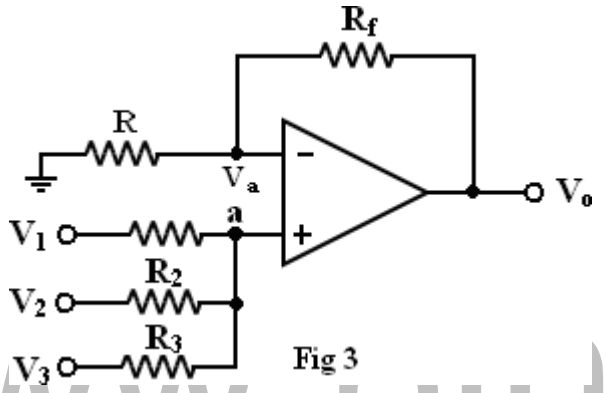


Fig 3

A summer that gives a non- inverted sum is the non- inverting summing amplifier of figure **3.** Let the voltage at the (-) input teriminal be V_a.

which is a non- inverting weighted sumof inputs.

Let $R_1 = R_2 = R_3 = R = R_f/2$, then $V_o = V_1+V_2+V_3$

Subtractor:

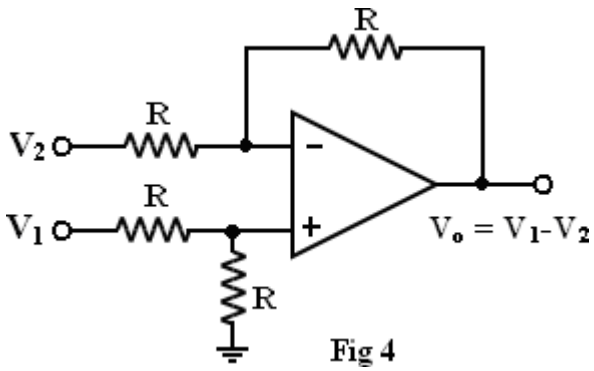


Fig 4

A basic differential amplifier can be used as a subtractor as shown in the above figure. If all resistors are equal in value, then the output voltage can be derived by using superposition principle.

To find the output V_{01} due to V_1 alone, make $V_2 = 0$.

Then the circuit of figure as shown in the above becomes a non- inverting amplifier having input voltage $V_1/2$ at the non- inverting input terminal and the output becomes

$$V_{01} = \frac{V_1}{2}\left(1 + \frac{R_f}{R}\right)$$

Similarly the output V_{02} due to V_2 alone (with V_1 grounded) can be written simply for an inverting amplifier as

$$V_{02} = -V_2$$

Thus the output voltage V_o due to both the inputs can be written as

$$V_o = V_{01} + V_{02} = V_1 - V_2$$

Adder/Subtractor:

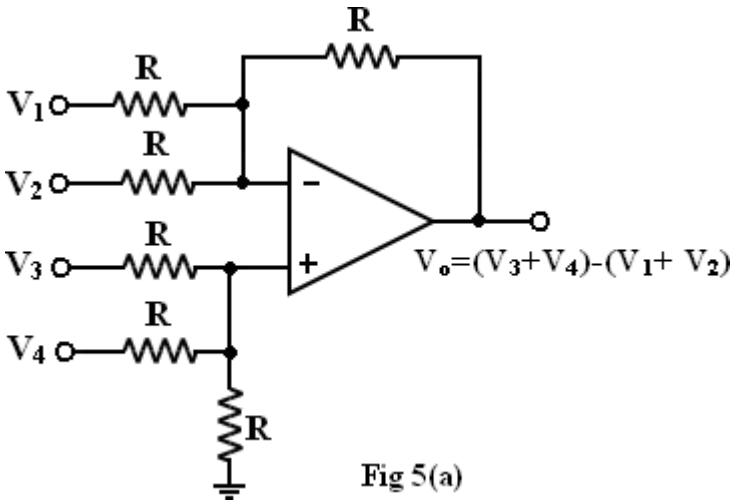


Fig 5(a)

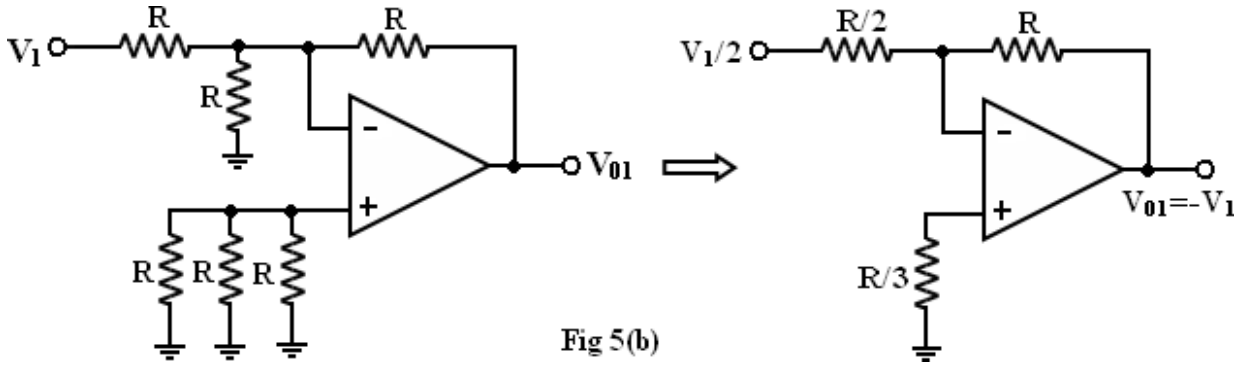


Fig 5(b)

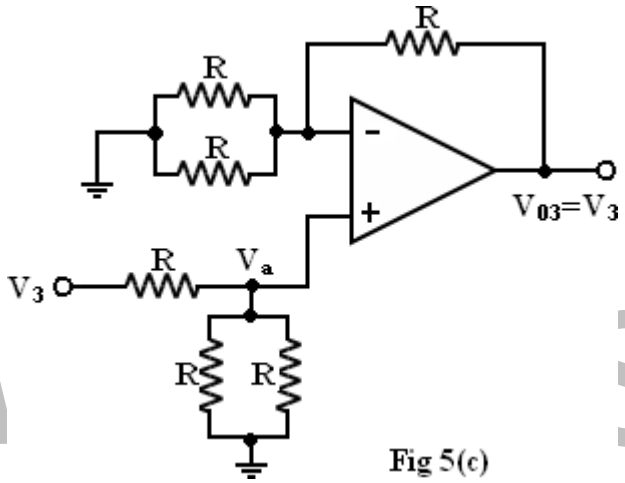


Fig 5(c)

It is possible to perform addition and subtraction simultaneously with a single op-amp using the circuit shown in figure 5(a).

The output voltage V_o can be obtained by using superposition theorem. To find output voltage V_{01} due to V_1 alone, make all other input voltages V_2, V_3 and V_4 equal to zero.

The simplified circuit is shown in figure 5(b). This is the circuit of an inverting amplifier and its output voltage is,

(by Thevenin's equivalent circuit at inverting input terminal).

Similarly, the output voltage V_{02} due to V_2 alone is,

V_{02} – @V v o l tage V_{03} due to the input voltage signal V_3 alone applied at the (+)

2

Now, the output

input terminal can be found by setting V_1, V_2 and V_4 equal to zero.

The circuit now becomes a non-inverting amplifier as shown in figure 5(c). The voltage V_a at the non- inverting terminal is

Similarly, it can be shown that the output voltage V_{04} due to V_4 alone is

$$V_{04} = V_4$$

Thus,

So, the circuit is an adder-subtractor.

Instrumentation Amplifier:

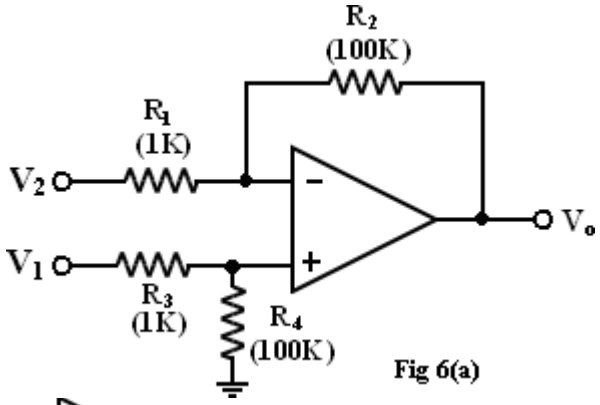


Fig 6(a)

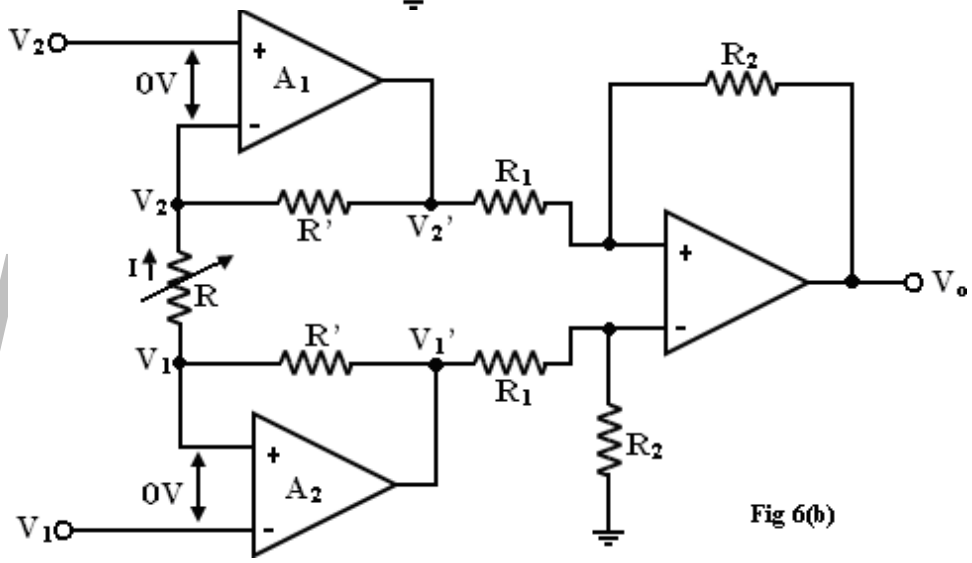


Fig 6(b)

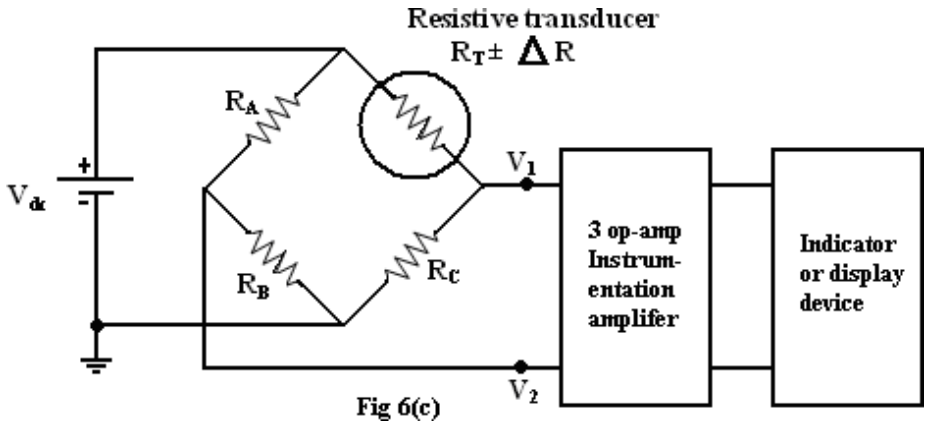


Fig 6(c)

In a number of industrial and consumer applications, one is required to measure and control physical quantities.

Some typical examples are measurement and control of temperature, humidity, light intensity, water flow etc. these physical quantities are usually measured with help of transducers.

The output of transducer has to be amplified so that it can drive the indicator or display system. This function is performed by an instrumentation amplifier. The important features of an instrumentation amplifier are

1. high gain accuracy
2. high CMRR
3. high gain stability with low temperature coefficient
4. low output impedance

There are specially designed op-amps such as µA725 to meet the above stated requirements of a good instrumentation amplifier. Monolithic (single chip) instrumentation amplifier are also available commercially such as AD521, AD524, AD620, AD624 by Analog Devices, LM363.XX (XX -->10,100,500) by National Semiconductor and INA101, 104, 3626, 3629 by Burr Brown.

In the circuit of figure 6(a), source V_1 sees an input impedance = R_3+R_4 (=101K) and the impedance seen by source V_2 is only R_1 (1K). This low impedance may load the signal source heavily.

Therefore, high resistance buffer is used preceding each input to avoid this loading effect as shown in figure 6(b).

The op-amp A_1 and A_2 have differential input voltage as zero. For $V_1=V_2$, that is, under common mode condition, the voltage across R will be zero. As no current flows through R and R‘ the non-inverting amplifier.

A_1 acts as voltage follower, so its output V_2‘=V_2. Similarly op-amp A_2 acts as voltage follower having output V_1‘=V_1. However, if $V_1 \neq V_2$, current flows in R and R‘, and $(V_2‘-V_{1‘})>(V_2-V_1)$. Therefore, this circuit has differential gain and CMRR more compared to the single op-amp circuit of figure 6(a).

The difference gain of this instrumentation amplifier R, however should never be made zero, as this will make the gain infinity. To avoid such a situation, in a practical circuit, a fixed resistance in series with a potentiometer is used in place of R.

Figure 6(c) shows a differential instrumentation amplifier using Transducer Bridge. The circuit uses a resistive transducer whose resistance changes as a function of the physical quantity to be measured.

The bridge is initially balanced by a dc supply voltage V_{dc} so that $V_1=V_2$. As the physical quantity changes, the resistance R_T of the transducer also changes, causing an unbalance in the bridge ($V_1 \neq V_2$). This differential voltage now gets amplified by the three op-amp differential instrumentation amplifier.

There are number differential applications of instrumentation amplifier with the transducer bridge, such as temperature indicator, temperature controller, and light intensity meter to name a few.