## Construction of a Monolithic Bipolar Transistor:

The fabrication of a monolithic transistor includes the following steps.

1. Epitaxial growth
2. Oxidation
3. Photolithography
4. Isolation diffusion
5. Base diffusion
6. Emitter diffusion
7. Contact mask
8. Aluminium metallization
9. Passivation

The letters P and N in the figures refer to type of doping, and a minus (-) or plus (+) with P and N indicates lighter or heavier doping respectively.

**1. Epitaxial growth:**

The first step in transistor fabrication is creation of the collector region. We normally require a low resistivity path for the collector current. This is due to the fact that, the collector contact is normally taken at the top, thus increasing the collector series resistance and the $V_{CE(Sat)}$ of the device.

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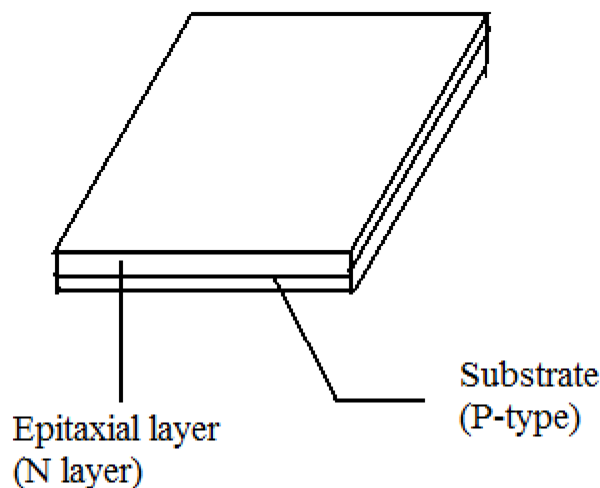


The higher collector resistance is reduced by a process called buried layer as shown in figure. In this arrangement, a heavily doped _N' region is sandwiched between the N-type epitaxial layer and

P – type substrate. This buried $N^+$ layer provides a low resistance path in the active collector

region to the collector contact C. In effect, the buried layer provides a low resistance shunt path for the flow of current.

For fabricating an NPN transistor, we begin with a P-type silicon substrate having a resistivity of typically 1Ω-cm, corresponding to an acceptor ion concentration of $1.4 * 10^{15}$ atoms/$cm^3$ . An oxide mask with the necessary pattern for buried layer diffusion is prepared. This is followed by masking and etching the oxide in the buried layer mask.

The N-type buried layer is now diffused into the substrate. A slow-diffusing material such as arsenic or antimony us used, so that the buried layer will stay-put during subsequent diffusions. The junction depth is typically a few microns, with sheet resistivity of around 20Ω per square.

Then, an epitaxial layer of lightly doped N-silicon is grown on the P-type substrate by placing the wafer in the furnace at $1200^0$ C and introducing a gas containing phosphorus (donor impurity). The resulting structure is shown in figure.

The subsequent diffusions are done in this epitaxial layer. All active and passive components are formed on the thin N- layer epitaxial layer grown over the P-type substrate. Obtaining an epitaxial layer of the proper thickness and doping with high crystal quality is perhaps the most formidable challenge in bipolar device processing.

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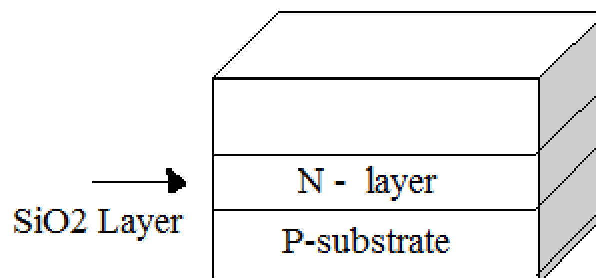
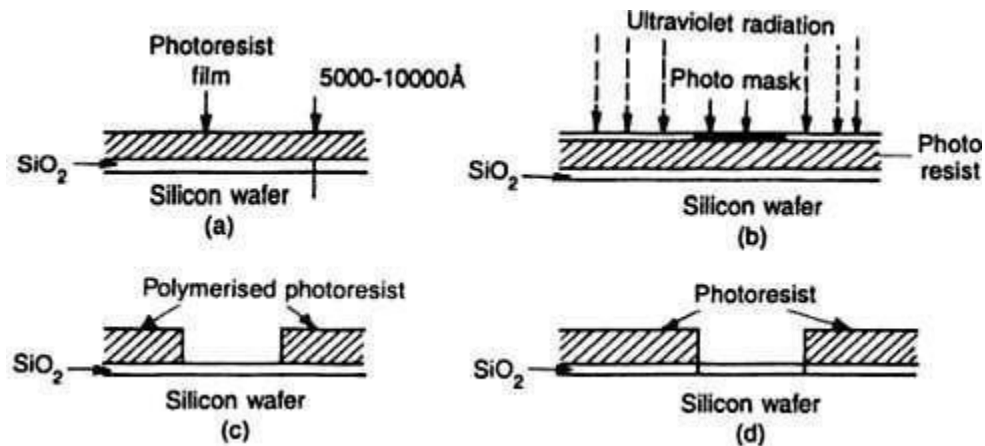
## 2. Oxidation:




As shown in figure, a thin layer of silicon dioxide ($SiO_2$) is grown over the N-type layer by exposing the silicon wafer to an oxygen atmosphere at about $1000^0$ C.

## 3. Photolithography:




The prime use of photolithography in IC manufacturing is to selectively etch or remove the $SiO_2$ layer. As shown in figure, the surface of the oxide is first covered with a thin uniform layer of photosensitive emulsion (Photo resist). The mask, a black and white negative of the requied pattern, is placed over the structure. When exposed to ultraviolet light, the photo resist under the transparent region of the mask becomes poly- merized. The mask is then removed and the wafer is treated chemically that removes the unexposed portions of the photoresist film. The polymerized region is cured so that it becomes resistant to corrosion. Then the chip is dipped in an etching solution of hydrofluoric acid which removes the oxide layer not protected by the polymerized photoresist. This creates openings in the $SiO_2$ layer through which P-type or N-type impurities can be diffused using the isolation diffusion process as shown in figure. After diffusion of impurities, the polymerized photoresist is removed with sulphuric acid and by a mechanical abrasion process.

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## 4. Isolation Diffusion:

The integrated circuit contains many devices. Since a number of devices are to be fabricated on the same IC chip, it becomes necessary to provide good isolation between various components and their interconnections.

The most important techniques for isolation are:

1. PN junction Isolation
2. Dielectric Isolation

In PN junction isolation technique, the $P^+$ type impurities are selectively diffused into the N-type epitaxial layer so that it touches the P-type substrate at the bottom. This method generated N-type isolation regions surrounded by P-type moats. If the P-substrate is held at the most negative potential, the diodes will become reverse-biased, thus providing isolation between these islands.

The individual components are fabricated inside these islands. This method is very economical, and is the most commonly used isolation method for general purpose integrated circuits.

In dielectric isolation method, a layer of solid dielectric such as silicon dioxide or ruby surrounds each component and this dielectric provides isolation. The isolation is both physical and electrical. This method is very expensive due to additional processing steps needed and this is mostly used for fabricating IC's required for special application in military and aerospace.

The PN junction isolation diffusion method is shown in figure. The process take place in a furnace using boron source. The diffusion depth must be atleast equal to the epitaxial thickness in order to obtain complete isolation. Poor isolation results in device failures as all transistors might get shorted together. The N-type island shown in figure forms the collector region of the NPN transistor. The heavily doped P-type regions marked $P^+$ are the isolation regions for the active and passive components that will be formed in the various N-type islands of the epitaxial layer.

## 5 Base diffusion:

Formation of the base is a critical step in the construction of a bipolar transistor. The base must be aligned, so that, during diffusion, it does not come into contact with either the isolation region or the buried layer. Frequently, the base diffusion step is a lso used in parallel to fabricate diffused resistors for the circuit. The value of these resistors depends on the diffusion conditions and the width of the opening made during etching. The base width influences the transistor parameters very strongly. Therefore, the base junction depth and resistivity must be tightly controlled. The base sheet resistivity should be fairly high (200- 500Ω per square) so that the base does not inject carriers into the emitter. For NPN transistor, the base is diffused in a furnace using a boron source. The diffusion process is done in two steps, pre deposition of dopants at $900^0$ C and driving them in at about $1200^0$ C. The drive-in is done in an oxidizing ambience, so that oxide is grown over the base region for subsequent fabrication steps. Figure shows that P-type base region of the transistor diffused in the N-type island (collector region) using photolithography and isolation diffusion processes.

## 6. Emitter Diffusion:

Emitter Diffusion is the final step in the fabrication of the transistor. The emitter opening must lie wholly within the base. Emitter masking not only opens windows for the emitter, but also for the contact point, which provides a low resistivity ohmic contact path for the emitter terminal.

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The emitter diffusion is normally a heavy N-type diffusion, producing low-resistivity layer that can inject charge easily into the base. A Phosphorus source is commonly used so that the diffusion time id shortened and the previous layers do not diffuse further. The emitter is diffused into the base, so that the emitter junction depth very closely approaches the base junction depth. The active base is then a P-region between these two junctions which can be made very narrow by adjusting the emitter diffusion time. Various diffusion and drive in cycles can be used to fabricate the emitter. The Resistivity of the emitter is usually not too critical.

The N-type emitter region of the transistor diffused into the P-type base region is shown below. However, this is not needed to fabricate a resistor where the resistivity of the P-type base region itself will serve the purpose. In this way, an NPN transistor and a resistor are fabricated simultaneously.

## 7. Contact Mask:

After the fabrication of emitter, windows are etched into the N-type regions where contacts are to be made for collector and emitter terminals. Heavily concentrated phosphorus $N^+$ dopant is diffused into these regions simultaneously.

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The reasons for the use of heavy $N^+$ diffusion is explained as follows: Aluminium, being a good conductor used for interconnection, is a P-type of impurity when used with silicon. Therefore, it can produce an unwanted diode or rectifying contact with the lightly doped N-material. Introducing a high concentration of $N^+$ dopant caused the Si lattice at the surface semi-metallic. Thus the $N^+$ layer makes a very good ohmic contact with the Aluminium layer. This is done by the oxidation, photolithography and isolation diffusion processes.

## 8. Metallization:

The IC chip is now complete with the active and passive devices, and the metal leads are to be formed for making connections with the terminals of the devices. Aluminium is deposited over the entire wafer by vacuum deposition. The thickness for single layer metal is 1µ m. Meta llization is carried out by evaporating aluminium over the entire surface and then selectively etching away aluminium to leave behind the desired interconnection and bonding pads as shown in figure.

Metallization is done for making interconnection between the various components fabricated in an IC and providing bonding pads around the circumference of the IC chip for later connection of wires

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## 9. Passivation/ Assembly and Packaging:

Metallization is followed by passivation, in which an insulating and protective layer is deposited over the whole device. This protects it against mechanical and chemical damage during subsequent processing steps. Doped or undoped silicon oxide or silicon nitride, or some combination of them, are usually chosen for passivation of layers. The layer is deposited by chemical vapour deposition (CVD) technique at a temperature low enough not to harm the metallization.

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# UNIT –I IC FABRICATION

## Integrated Circuits:

An integrated circuit (IC) is a miniature, low cost electronic circuit consisting of active and passive components fabricated together on a single crystal of silicon. The active components are transistors and diodes and passive components are resistors and capacitors.

## Advantages of integrated circuits:

Miniaturization and hence increased equipment density.
Cost reduction due to batch processing.
Increased system reliability due to the elimination of soldered joints.
Improved functional performance.
Matched devices.
Increased operating speeds.
Reduction in power consumption

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## Classification:

Integrated circuits can be classified into analog, digital and mixed signal (both analog and digital on the same chip). Based upon above requirement two different IC technology namely Monolithic Technology and Hybrid Technology have been developed. In monolithic IC ,all circuit components ,both active and passive elements and their interconnections are manufactured into or on top of a single chip of silicon. In hybrid circuits, separate component parts are attached to a ceramic substrate and interconnected by means of either metallization pattern or wire bounds.

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Digital integrated circuits can contain anything from one to millions of logic gates, flip- flops, multiplexers, and other circuits in a few square millimeters. The small size of these circuits allows high speed, low power dissipation, and reduced manufacturing cost compared with board- level integration. These digital ICs, typ ically microprocessors, DSPs, and micro controllers work using binary mathematics to process "one" and "zero" signals.

Analog ICs, such as sensors, power management circuits, and operational amplifiers, work by processing continuous signals. They perform functions like amplification, active filtering, demodulation, mixing, etc. Analog ICs ease the burden on circuit designers by having expertly designed analog circuits available instead of designing a difficult analog circuit from scratch.

ICs can also combine analog and digital circuits on a single chip to create functions such as A/D converters and D/A converters. Such circuits offer smaller size and lower cost, but must carefully account for signal interference

## Classification of ICs:

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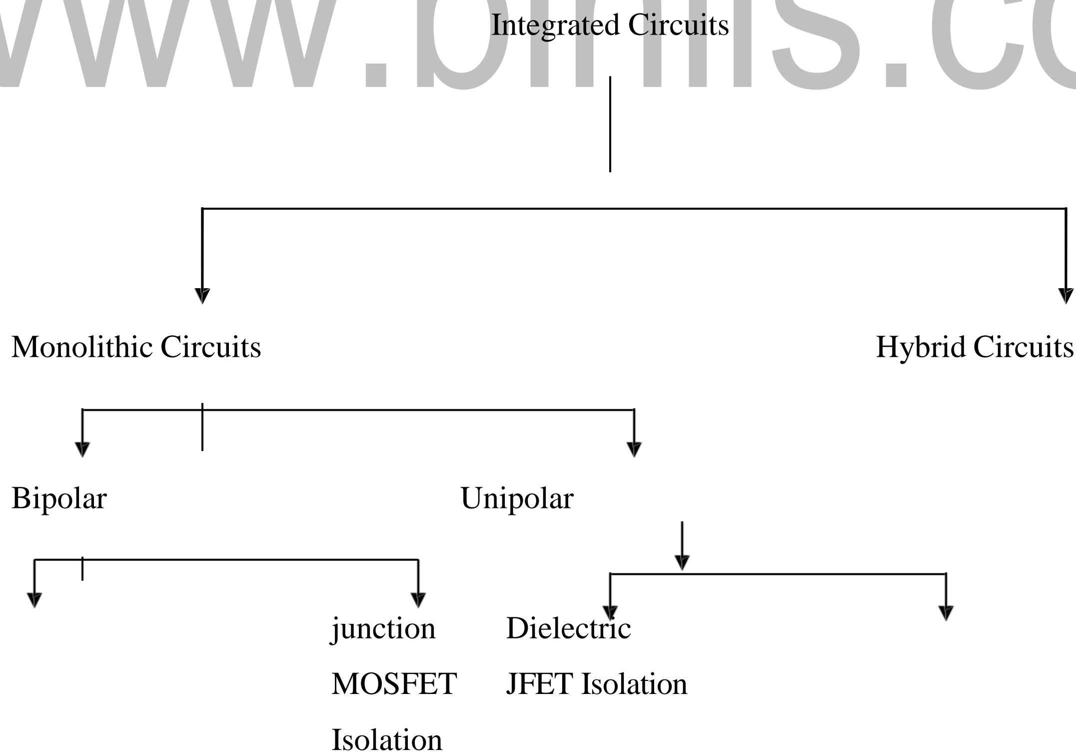

## Generations

## SSI, MSI and LSI

The first integrated circuits contained only a few transistors. Called "Small-Scale Integration" (SSI), digital circuits containing transistors numbering in the tens provided a few logic gates for example, while early linear ICs such as the Plessey SL201 or the Philips TAA320 had as few as two transistors. The term Large Scale Integration was first used by IBM scientist Rolf Landauer when describing the theoretical concept, from there came the terms for SSI, MSI, VLSI, and ULSI. They began to appear in consumer products at the turn of the decade, a typical l application being FM inter-carrier sound processing in television receivers.

The next step in the development of integrated circuits, taken in the late 1960s, introduced devices which contained hundreds of transistors on each chip, called "Medium-Scale Integration" (MSI). They were attractive economically because while they cost little more to produce than SSI devices, they allowed more complex systems to be produced using smaller circuit boards, less assembly work (because of fewer separate components), and a number of other advantages.

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## VLSI

The final step in the development process, starting in the 1980s and continuing through the present, was "very large-scale integration" (VLSI). The development started with hundreds of thousands of transistors in the early 1980s, and continues beyond several billion transistors as of 2007.

In 1986 the first one megabit RAM chips were introduced, which contained more than one million transistors. Microprocessor chips passed the million transistor mark in 1989 and the billion transistor mark in 2005

## ULSI, WSI, SOC and 3D-IC

To reflect further growth of the complexity, the term ULSI that stands for "Ultra-Large Scale Integration" was proposed for chips of complexity of more than 1 million transistors.

Wafer-scale integration (WSI) is a system of building very- large integrated circuits that uses an entire silicon wafer to produce a single "super-chip". Through a combination of large size and reduced packaging, WSI could lead to dramatically reduced costs for some systems, notably

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Massively parallel supercomputers. The name is taken from the term Very-Large-Scale Integration, the current state of the art when WSI was being developed.

System-on-a-Chip (SoC or SOC) is an integrated circuit in which all the components needed for a computer or other system are included on a single chip. The design of such a device can be complex and costly, and building disparate components on a single piece of silicon may compromise the efficiency of some elements.

However, these drawbacks are offset by lower manufacturing and assembly costs and by a greatly reduced power budget: because signals among the components are kept on-die, much less power is require. Three Dimensional Integrated Circuit (3D-IC) has two or more layers of active electronic components that are integrated both vertically and horizontally into a single circuit. Communication between layers uses on-die signaling, so power consumption is much lower than in equivalent separate circuits. Judicious use of short vertical wires can substantially reduce overall wire length for faster operation.

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# Transistor Fabrication:

## PNP Transistor:

The integrated PNP transistors are fabricated in one of the following three structures.

1. Substrate or Vertical PNP
2. Lateral or horizontal PNP and
3. Triple diffused PNP.

## Substrate or Vertical PNP:

The P-substrate of the IC is used as the collector, the N-epitaxial layer is used as the base and the next P-diffusion is used as the emitter region of the PNP transistor. The structure of a vertical monolithic PNP transistor $Q_1$ is shown in figure. The base region of an NPN transistor structure is formed in parallel with the emitter region of the PNP transistor.

The method of fabrication has the disadvantage of having its collector held at a fixed negative potential. This is due to the fact that the P-substrate of the IC is always held at a negative potential normally for providing good isolation between the circuit components and the substrate.

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## Triple diffused PNP:

This type of PNP transistor is formed by including an additional diffusion process over the standard NPN transistor processing steps. This is called a triple diffusion process, because it involves an additional diffusion of P-region in the second N-diffusion region of a NPN transistor. The structure of the triple diffused monolithic PNP transistor $Q_2$ is also shown in the below figure.

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This has the limitations of requiring additional fabrication steps and sophisticated fabrication assemblies.

## Lateral or Horizontal PNP:

This is the most commonly used form of integrated PNP transistor fabrication method. This has the advantage that it can be fabricated simultaneously with the processing steps of an NPN transistor and therefore it requires as the base of the PNP transistor. During the P-type base diffusion process of NPN transistor, two parallel P-regions are formed which make the emitter and collector regions of the horizontal PNP transistor.

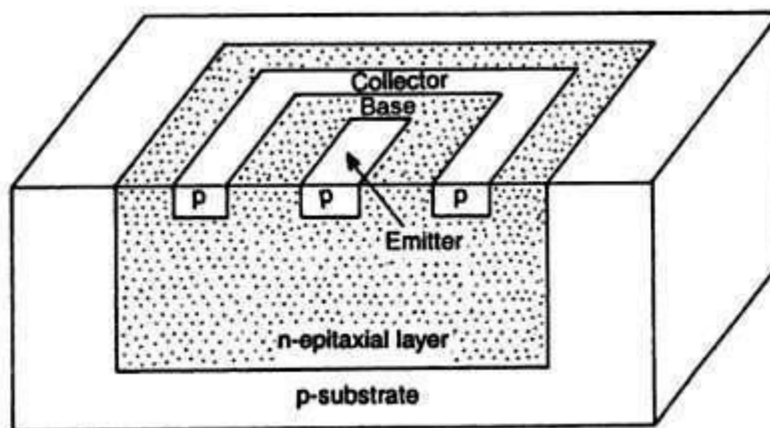


Fig. 1.17 A *pnp* lateral transistor

Comparison of monolithic NPN and PNP transistor:

Normally, the NPN transistor is preferred in monolithic circuits due to the following reasons:

1. The vertical PNP transistor must have his collector held at a fixed negative voltage.

2. The lateral PNP transistor has very wide base region and has the limitation due to the lateral diffusion of P-type impurities into the N-type base region. This makes the photographic mask making, alignment and etching processes very difficult. This reduces the current gain of lateral PNP transistors as low as 1.5 to 30 as against 50 to 300 for a monolithic NPN transistor.

3. The collector region is formed prior to the formation of base and emitter diffusion. During the later diffusion steps, the collector impurities diffuse on either side of the defined collector junction. Since the N-type impurities have smaller diffusion constant compared to P-type impurities the N-

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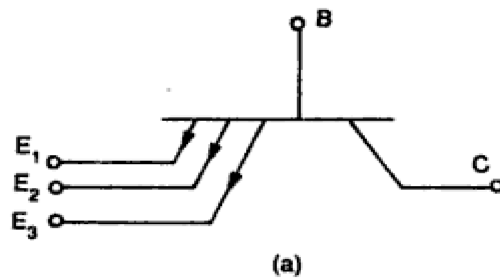
type collector performs better than the P-type collector. This makes the NPN transistor preferable for monolithic fabrication due to the easier process control.

Transistor with multiple emitters: The applications such as transistor- transistor logic (TTL) require multiple emitters. The below figure shows the circuit sectional view of three N-emitter regions diffused in three places inside the P-type base. This arrangement saves the chip area and enhances the component density of the IC.



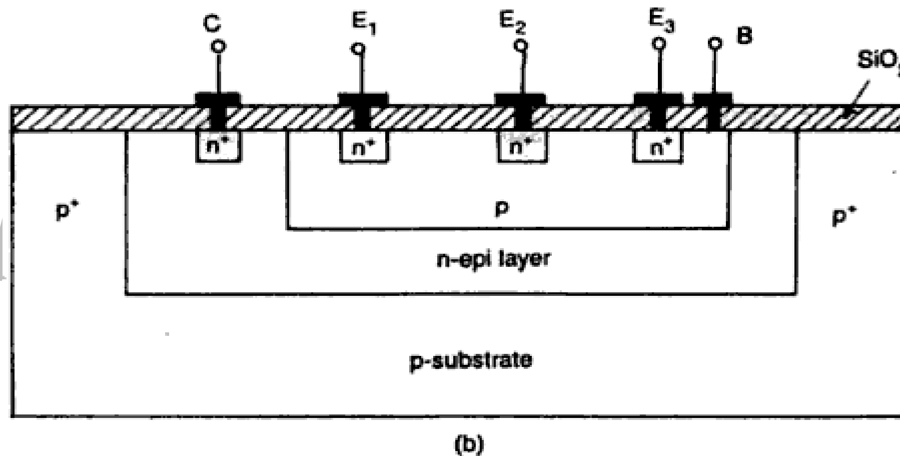




Fig. 1.18 (a) Multi-emitter transistor, (b) Cross-sectional view of a multi-emitter transistor

## Schottky Barrier Diode:

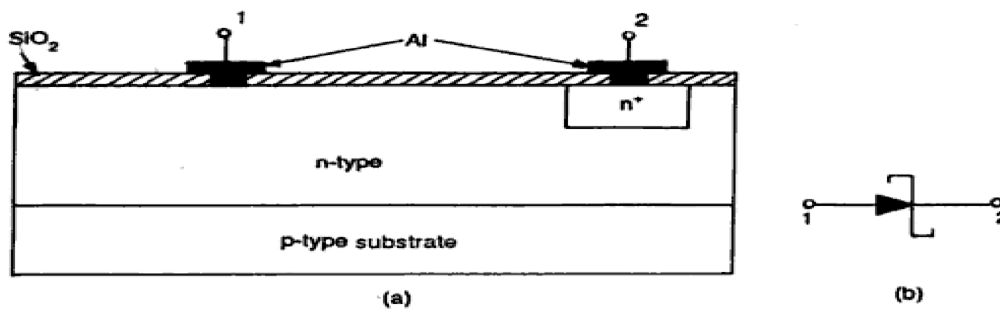



Fig. 1.21 (a) A Schottky diode, (b) Symbol for metal semiconductor diode

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The metal contacts are required to be ohmic and no PN junctions to be formed between the metal and silicon layers. The $N^+$ diffusion region serves the purpose of generating ohmic contacts. On the other hand, if aluminum is deposited directly on the N-type silicon, then a metal semiconductor diode can be said to be formed. Such a metal semiconductor diode junction exhibits the same type of V-I Characteristics as that of an ordinary PN junction.

The cross sectional view and symbol of a Schottky barrier diode as shown in figure. Contact 1 shown in figure is a Schottky barrier and the contact 2 is an ohmic contact. The contact potential between the semiconductor and the metal generated a barrier for the flow of conducting electrons from semiconductor to metal. When the junction is forward biased this barrier is lowered and the electron flow is allowed from semiconductor to metal, where the electrons are in large quantities.

The minority carriers carry the conduction current in the Schottky diode whereas in the PN junction diode, minority carriers carry the conduction current and it incurs an appreciable time delay from ON state to OFF state. This is due to the fact that the minority carriers stored in the junction have to be totally removed. This characteristic puts the Schottky barrier diode at an advantage since it exhibits negligible time to flow the electron from N-type silicon into aluminum almost right at the contact surface, where they mix with the free electrons. The other advantage of this diode is that it has less forward voltage (approximately 0.4V). Thus it can be used for clamping and detection in high frequency applications and microwave integrated circuits.

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## Schottky transistor:

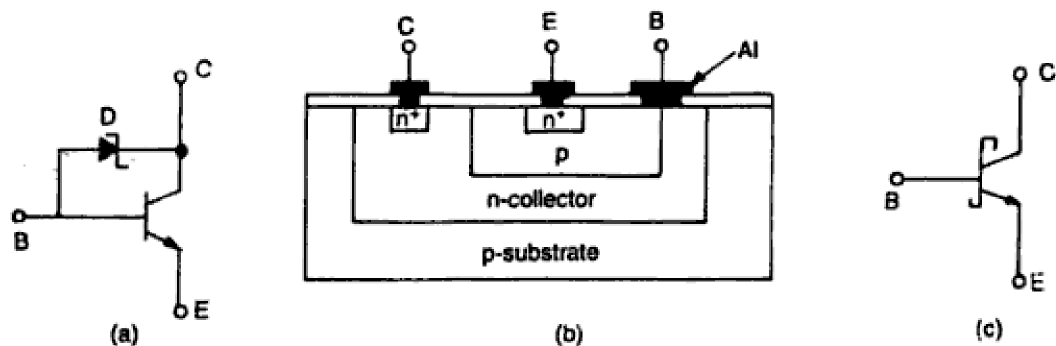


**Fig. 1.19** (a) A transistor with a Schottky-barrier diode clamped between base and collector to prevent saturation, (b) Cross-section of a Schottky-barrier transistor, (c) Symbolic representation

The cross-sectional view of a transistor employing a Schottky barrier diode clamped between its base and collector regions is shown in figure. The equivalent circuit and the symbolic representation of the Schottky transistor are shown in figure. The Schottky diode is formed by allowing aluminium metallization for the base lead which makes contact with the N-type collector region also as shown in figure.

When the base current is increased to saturate the transistor, the voltage at the collector C reduces and this makes the diode Ds conduct. The base to collector voltage reduces to 0.4V, which is less the cut- in-voltage of a silicon base-collector junction. Therefore, the transistor does not get saturated.

## Monolithic diodes:

The diode used in integrated circuits are made using transistor structures in one of the five possible connections. The three most popular structures are shown in figure. The diode is obtained from a transistor structure using one of the following structures.

1. The emitter-base diode, with collector short circuited to the base.
2. The emitter-base diode with the collector open and
3. The collector –base diode, with the emitter open-circuited.

The choice of the diode structure depends on the performance and application desired. Collector-base diodes have higher collector-base arrays breaking rating, and they are suitable for common-cathode diode arrays diffused within a single isolation island. The emitter-base diffusion is very popular for the fabrication of diodes, provided the reverse-voltage requirement of the circuit does not exceed the lower base-emitter breakdown voltage.

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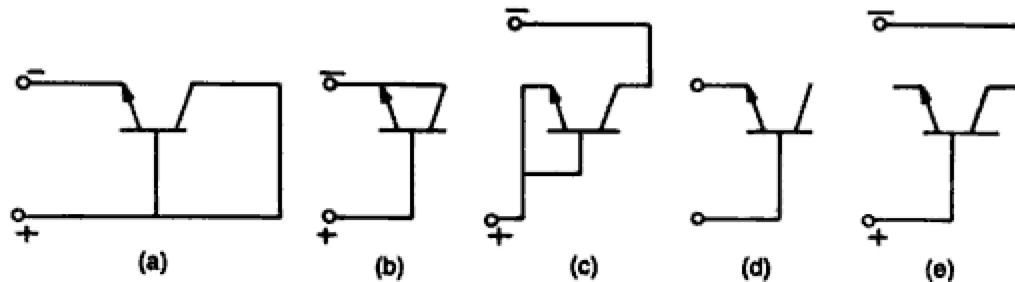
| Characteristic | (a) $V_{CB} = 0$ | (b) $V_{CE} = 0$ | (c) $V_{EB} = 0$ | (d) $I_C = 0$ | (e) $I_E = 0$ |
|---|---|---|---|---|---|
| Breakdown voltage in volts | 7 | 7 | 55 | 7 | 55 |
| Storage time, n sec | 9 | 100 | 53 | 56 | 85 |
| Forward voltage in volts | .85 | .92 | .94 | .96 | .95 |




## Integrated Resistors:

A resistor in a monolithic integrated circuit is obtained by utilizing the bulk resistivity of the diffused volume of semiconductor region. The commonly used methods for fabricating integrated resistors are 1. Diffused 2. epitaxial 3. Pinched and 4. Thin film techniques.

## Diffused Resistor:

The diffused resistor is formed in any one of the isolated regions of epitaxial layer during base or emitter diffusion processes. This type of resistor fabrication is very economical as it runs in parallel to the bipolar transistor fabrication. The N-type emitter diffusion and P-type base diffusion are commonly used to realize the monolithic resistor.

The diffused resistor has a severe limitation in that, only small valued resistors can be fabricated. The surface geometry such as the length, width and the diffused impurity profile determine the resistance value. The commonly used parameter for defining this resistance is called the sheet resistance. It is defined as the resistance in ohms/square offered by the diffused area.

In the monolithic resistor, the resistance value is expressed by

$R = R_s\, 1/w$ where R= resistance offered (in ohms)

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$R_s$ = sheet resistance of the particular fabrication process involved (in ohms/square)
l = length of the diffused area and
w = width of the diffused area.

The sheet resistance of the base and emitter diffusion in 200Ω/Square and 2.2Ω/square respectively. For example, an emitter-diffused strip of 2mil wide and 20 mil long will offer a resistance of 22Ω. For higher values of resistance, the diffusion region can be formed in a zig-zag fashion resulting in larger effective length. The poly silicon layer can also be used for resistor realization.

## Epitaxial Resistor:

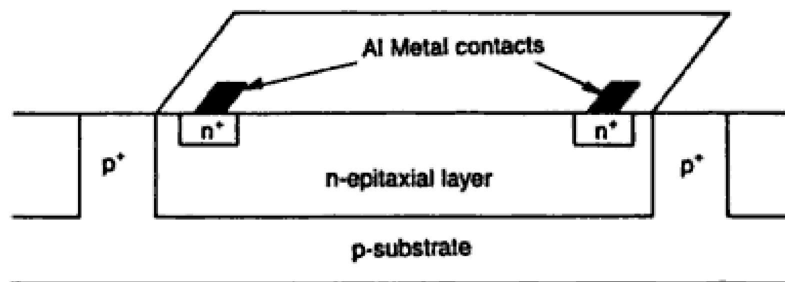


Fig. 1.23 (a) Epitaxial resistor

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The N-epitaxial layer can be used for realizing large resistance values. The figure shows the cross-sectional view of the epitaxial resistor formed in the epitaxial layer between the two $N^+$ aluminium metal contacts.

## Pinched resistor:

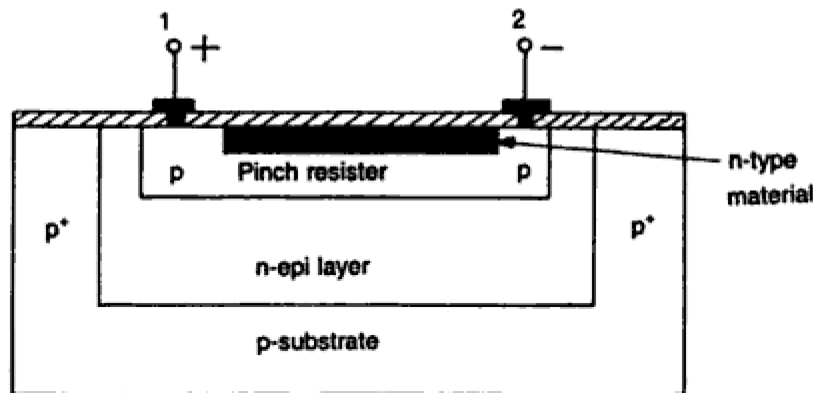


Fig. 1.23 (b) Cross-sectional view of a pinch resistor

The sheet resistance offered by the diffusion regions can be increased by narrowing down its cross-sectional area. This type of resistance is normally achieved in the base region. Figure shows a pinched base diffused resistor. It can offer resistance of the order of mega ohms in a

comparatively smaller area. In the structure shown, no current can flow in the N-type material since the diode realized at contact 2 is biased in reversed direction. Only very small reverse saturation current can flow in conduction path for the current has been reduced or pinched. Therefore, the resistance between the contact 1 and 2 increases as the wid th narrows down and hence it acts as a pinched resistor.

## Thin film resistor:

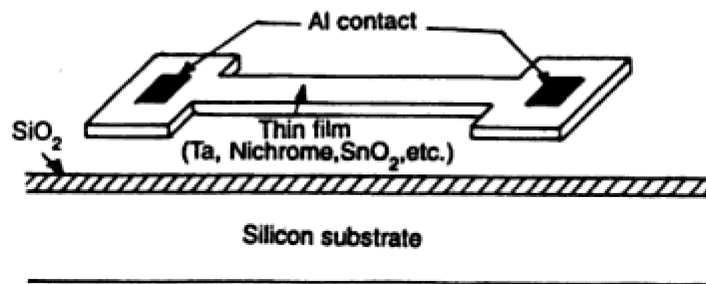


**Fig. 1.23** (c) Cross-section of a thin film resistor

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The thin film deposition technique can also be used for the fabrication of monolithic resistors. A very thin metallic film of thickness less than 1µm is deposited on the silicon dioxide layer by vapour deposition techniques. Normally, Nichrome (NiCr) is used for this process. Desired geometry is achieved using masked etching processes to obtain suitable value of resistors. Ohmic contacts are made using aluminium metallization as discussed in earlier sections.

The cross-sectional view of a thin film resistor as shown in figure. Sheet resistances of 40 to 400Ω/ square can be easily obtained in this method and thus 20kΩ to 50kΩ values are very practical.

The advantages of thin film resistors are as follows:

1. They have smaller parasitic components which makes their high frequency behavior good.
2. The thin film resistor values can be very minutely controlled using laser trimming.
3. They have low temperature coefficient of resistance and this makes them more stable.

The thin film resistor can be obtained by the use of tantalum deposited over silicon dioxide layer. The main disadvantage of thin film resistor is that its fabrication requires additional processing steps.

**Monolithic Capacitors:**

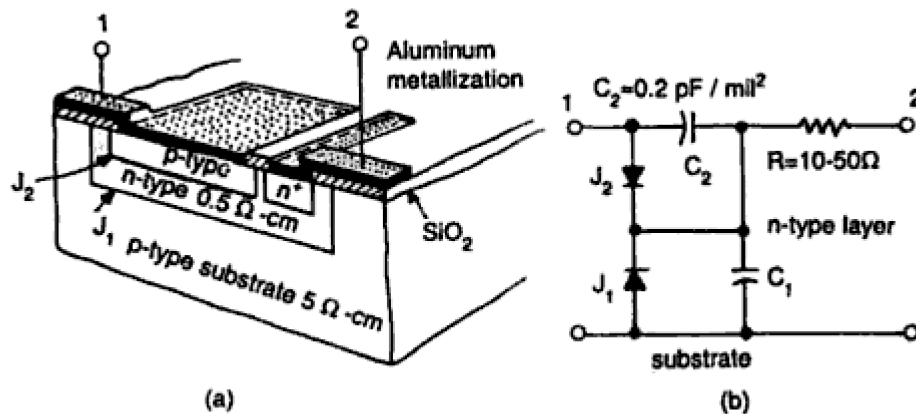


Fig. 1.24 (a) Junction-type IC capacitor, (b) Equivalent circuit

Monolithic capacitors are not frequently used in integrated circuits since they are limited in the range of values obtained and their performance. There are, however, two types available, the junction capacitor is a reverse biased PN junction formed by the collector-base or emitter-base diffusion of the transistor. The capacitance is proportional to the area of the junction and inversely proportional to the depletion thickness.

C α A, where a is the area of the junction and

C α T , where t is the thickness of the depletion layer.

The capacitance value thus obtainable can be around $1.2nF/mm^2$ .

The thin film or metal oxide silicon capacitor uses a thin layer of silicon dioxide as the dielectric. One plate is the connecting metal and the other is a heavily doped layer of silicon, which is formed during the emitter diffusion. This capacitor has a lower leakage current and is non-directional, since emitter plate can be biased positively. The capacitance value of this method can be varied between 0.3 and $0.8nF/mm^2$ .

**Inductors:**

No satisfactory integrated inductors exist. If high Q inductors with inductance of values larger than 5μH are required, they are usually supplied by a wound inductor which is connected externally to the chip. Therefore, the use of inductors is normally avoided when integrated circuits are used.

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