5.11 POWER AUDIO AMPLIFIER IC LM 380

Introduction:

Small signal amplifiers are essentially voltage amplifier that supplies their loads with larger amplifier signal voltage. On the other hand, large signal or power amplifier supply a large signal current to current operated loads such as speakers & motors. Figure 5.11.1 Shown below is the Functional block diagram of Audio power Amplifier.

In audio applications, however, the amplifier called upon to deliver much higher current than that supplied by general purpose op-amps. This means that loads such as speakers & motors requiring substantial currents cannot be driven directly by the output of general purpose op-amps. Pin diagram of power ampilfierLM380 and block diagram of LM380 is shown in figure 5.11.2 and figure 5.11.3. To handle it following is done

- To use discrete or monolithic power transistors called power boosters at the output of the op-amp
- To use specialized ICs designed as power amplifiers like LM 380.

Features of LM380:

1. Internally fixed gain of 50 (34dB)
2. Output is automatically self centering to one half of the supply voltage.
3. Output is short circuit proof with internal thermal limiting.
4. Input stage allows the input to be ground referenced or ac
5. Wide supply voltage range (5 to 22V).
6. High peak current capability.
7. High impedance.

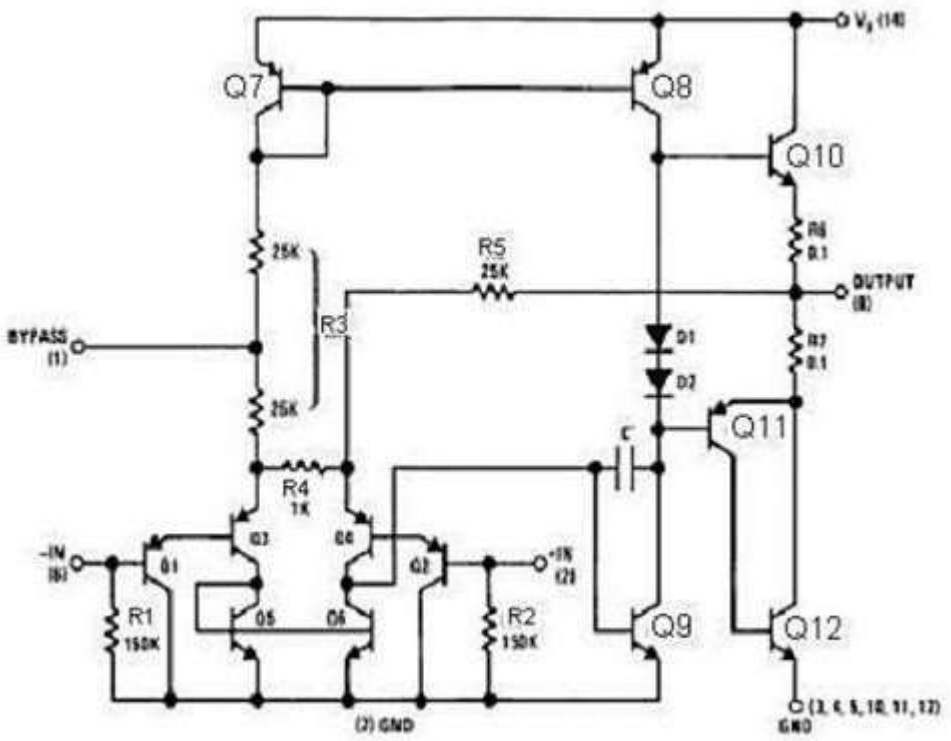


Figure 5.11.1 Functional block diagram of Audio power Amplifier

[source: https://www.brainkart.com/subject/Linear-Integrated-Circuits_220/]

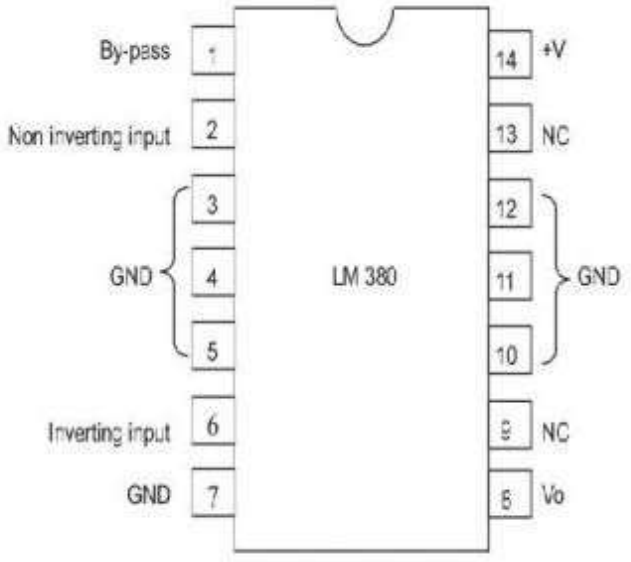


Figure 5.11.2 Pin diagram of power ampilfierLM380

[source: https://www.brainkart.com/subject/Linear-Integrated-Circuits_220/]

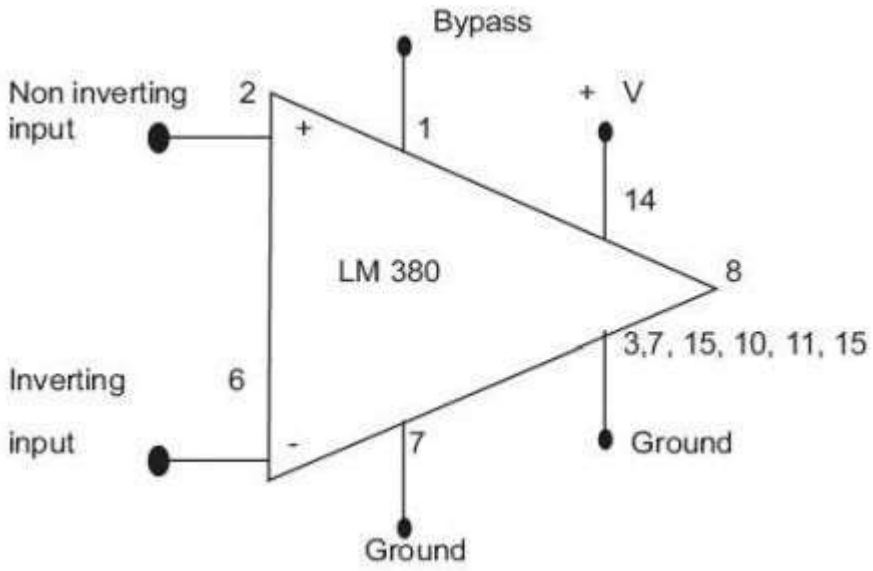


Figure 5.11.3.Block diagram of LM380

[source: https://www.brainkart.com/subject/Linear-Integrated-Circuits_220/]

LM380 circuit description:

It is connected of 4 stages,

i. PNP emitter follower
ii. Different amplifier
iii. Common emitter
iv. Emitter follower

(i) PNP Emitter follower:

- The input stage is emitter follower composed of PNP transistors Q1 & Q2 which drives the PNP Q3-Q4 differential pair.
- The choice of PNP input transistors Q1 & Q2 allows the input to be referenced to ground i.e., the input can be direct coupled to either the inverting & non-inverting terminals of the amplifier.

(ii) Differential Amplifier:

- The current in the PNP differential pair Q3-Q4 is established by Q7, R3 & +V.
- The current mirror formed by transistor Q7, Q8 & associated resistors then establishes the collector current of Q9.
- Transistor Q5 & Q6 constitute of collector loads for the PNP differential pair.

- The output of the differential amplifier is taken at the junction of Q4 & Q6 transistors & is applied as an input to the common emitter voltage gain.

(iii) Common Emitter amplifier stage:

- Common Emitter amplifier stage is formed by transistor Q9 with D1, D2 & Q8 as a current source load.
- The capacitor C between the base & collector of Q9 provides internal compensation & helps to establish the upper cutoff frequency of 100 KHz.
- Since Q7 & Q8 form a current mirror, the current through D1 & D2 is approximately the same as the current through R3.
- D1 & D2 are temperature compensating diodes for transistors Q10 & Q11 in that D1 & D2 have the same characteristics as the base-emitter junctions of Q11. Therefore the current through Q10 & (Q11-Q12) is approximately equal to the current through diodes D1 & D2.

(iv) (Output stage) - Emitter follower:

- Emitter follower formed by NPN transistor Q10 & Q11. The combination of PNP transistor Q11 & NPN transistor Q12 has the power capability of NPN transistors but the characteristics of a PNP transistor.
- The negative dc feedback applied through R5 balances the differential amplifier so that the dc output voltage is stabilized at +V/2;
- To decouple the input stage from the supply voltage +V, by pass capacitor in order of micro farad should be connected between the bypass terminal (pin 1) & ground (pin 7).
- The overall internal gain of the amplifier is fixed at 50. However gain can be increased by using positive feedback.

Applications:

(i) Audio Power Amplifier:

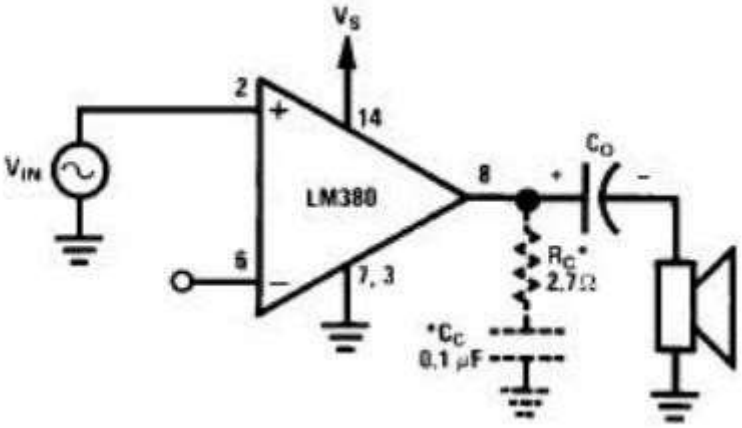


Figure 5.11.4.Connections of Audio power amplifier

[source: https://www.brainkart.com/subject/Linear-Integrated-Circuits_220/]

- Figure 5.11.4 shown above is the connection of Audio power Amplifier.Amplifier requires very few external components because of the internal biasing, compensation & fixed gain.
- When the power amplifier is used in the non inverting configuration, the inverting terminal may be either shorted to ground, connected to ground through resistors & capacitors.
- Similarly when the power amplifier is used in the inverting mode, the non inverting terminal may be either shorted to ground or returned to ground through resistor or capacitor.
- Usually a capacitor is connected between the inverting terminal & ground if the input has a high internal impedance.
- As a precautionary measure, an RC combination should be used at the output terminal (pin 8) to eliminate 5-to-10 MHz oscillation.
- C1 is coupling capacitor which couples the output of the amplifier to the 8 ohms loud speaker which acts as a load. The amplifier will amplify the Vin applied at the non-inverting terminal.

(ii) LM 380 as a High gain amplifier:

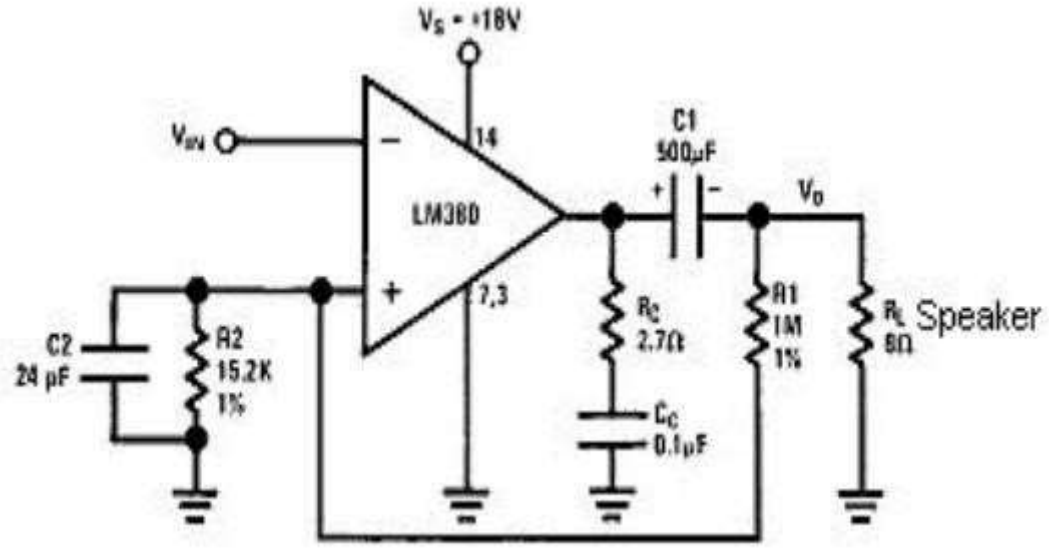


Figure 5.11.5.Circuit connections of LM380 as a High gain Amplifier

[source: https://www.brainkart.com/subject/Linear-Integrated-Circuits_220/]

- Figure 5.11.5 shown above is the circuit connections of LM380 as a High gain Amplifier.The gain of LM380 is internally fixed at 50. But it can be increased by using the external components.
- The increase in gain is possible due to the use of positive feedback, this setup to obtain a gain 200.

(iii) LM 380 as a variable Gain:

- Figure 5.11.6. shown below is the circuit connections of LM380 as a Variable gain Amplifier.Instead of getting a fixed gain of 50, it is possible to obtain a variable gain up to 50 by connecting a potentiometer between the input terminals.

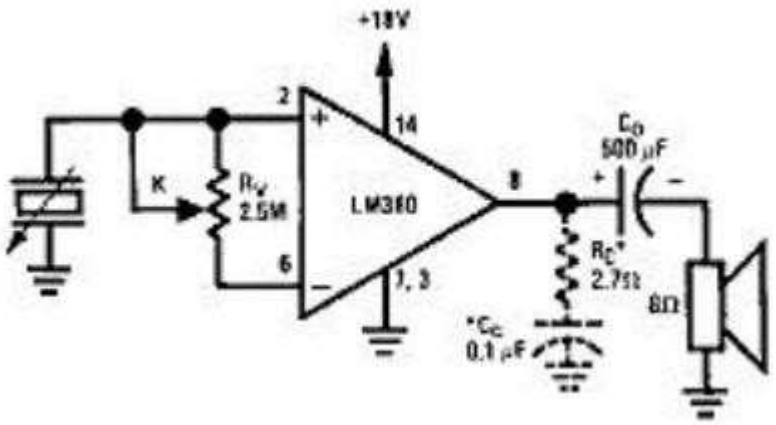


Figure 5.11.6. Circuit connections of LM380 as a Variable gain Amplifier

[source: https://www.brainkart.com/subject/Linear-Integrated-Circuits_220/]

(iv) LM 380 as a Bridge Audio Power Amplifier:

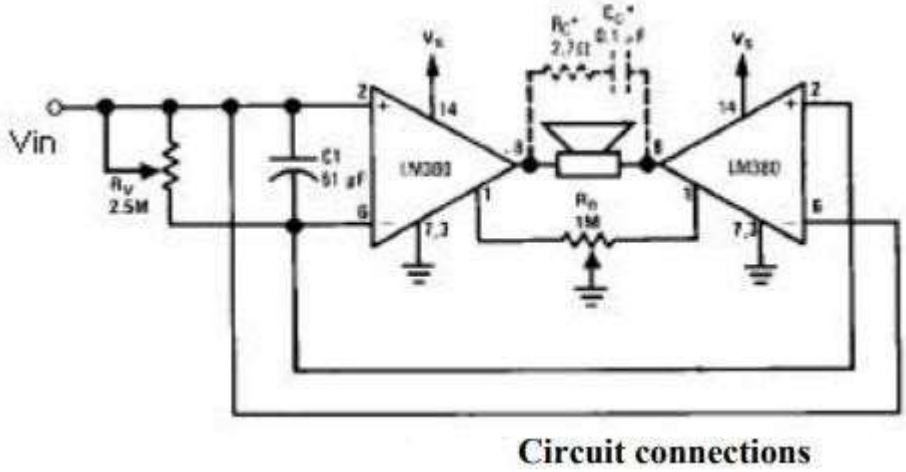


Figure 5.11.7 Circuit connections of LM380 as a Bridge Audio power Amplifier

[source: https://www.brainkart.com/subject/Linear-Integrated-Circuits_220/]

- Figure 5.11.6. shown above is the circuit connections of LM380 as a Bridge Audio power Amplifier.If a certain application requires more power than what is provided by a single LM380 amplifier, then two LM380 chips can be used in the bridge configuration.
- With this arrangement we get an output voltage swing which is twice that of a single LM380 amplifier.

- As the voltage is doubled, power output will increase by four times that of a single LM380 amplifier. The pot R4 is used to balance the output offset voltages of the two chips.

(v) Intercom system using LM 380:

- Figure 5.11.8. shown below is the Intercom system using LM380 as Talk mode.When the switch is in Talk mode position, the master speaker acts as a microphone.
- Figure 5.11.9. shown below is the Intercom system using LM380 as Listen mode.When the switch is in Listen position, the remote speaker acts as a microphone.
- In either phone the overall gain of the circuit is the same depends on the turns of transformer T.

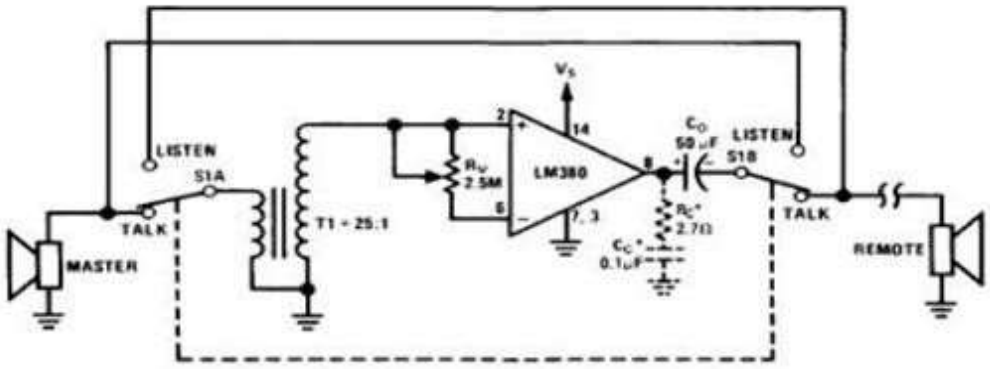


Figure 5.11.8.Intercom system using LM380 as Talk mode

[source: https://www.brainkart.com/subject/Linear-Integrated-Circuits_220/]

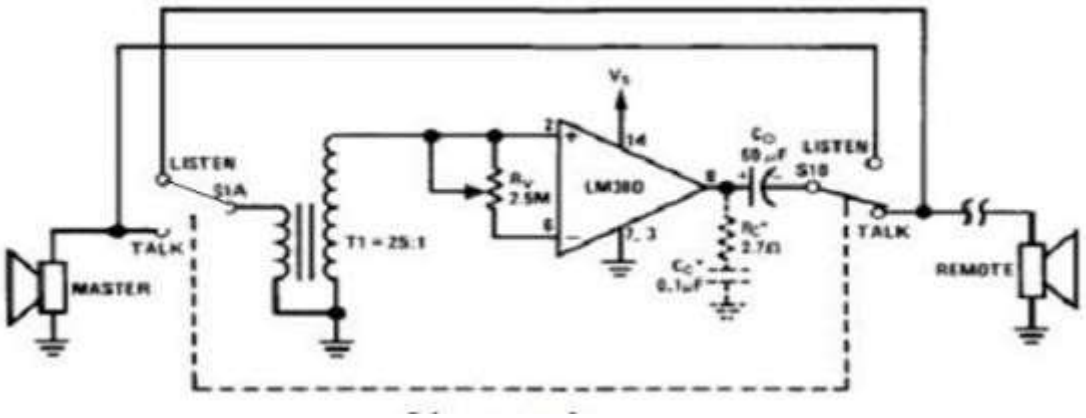


Figure 5.11.9 Intercom system using LM380 as Listen mode

[source: https://www.brainkart.com/subject/Linear-Integrated-Circuits_220/]

5.12 VIDEO AMPLIFIER

DESCRIPTION

The 733 is a monolithic differential input, differential output, wideband video amplifier. It offers fixed gains of 10,100 or 400 without external components, and adjustable gains from 10 to 400 by the use of an external resistor. No external frequency compensation components are required for any gain option. Gain stability, wide bandwidth and low phase distortion are obtained through use of the classic series-shunt feedback from the emitter follower outputs to the inputs of the second stage. The emitter follower outputs provide low output impedance, and enable the device to drive capacitive loads. The 733 is intended for use as a high performance video and pulse amplifier in communications, magnetic memories, display and video recorder systems. Fig 1.shown below is the Pin configuration and IC package of Video Amplifier.

FEATURES

• 120 MHz Bandwidth

• 250k£2 Input Resistance

• Selectable Gains of 10,100 and 400

• No Frequency Compensation Required

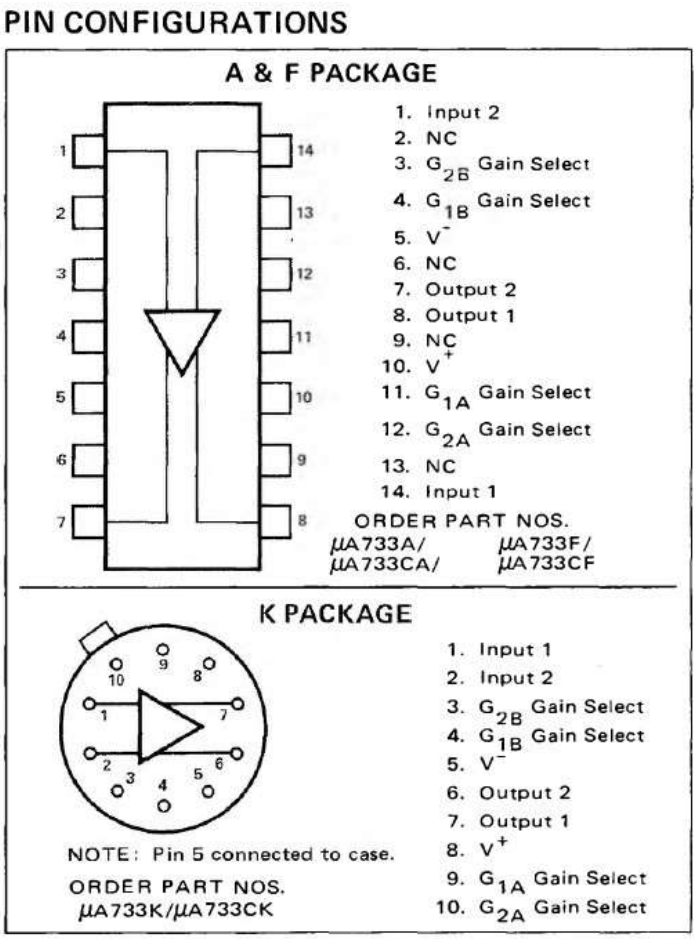


Figure 5.12.1.Pin configuration and IC package of Video Amplifier

[source:http://www.elektronikjk.pl/elementy_czynne/IC/UA733-2.pdf]

MONOLITHIC VIDEO AMPLIFIER

Video amplifiers are a special type of wide band amplifier that also preserve the DC level of the signal and are used specifically for signals that are to be applied to CRTs or other video equipment. The video signal carries all the picture information in TV, video and radar systems. The bandwidth of video amplifiers depends on use. In TV receivers it extends from 0Hz (DC) to 6MHz and is wider still in radar. Monolithic video amplifier is shown in figure 5.12.2.

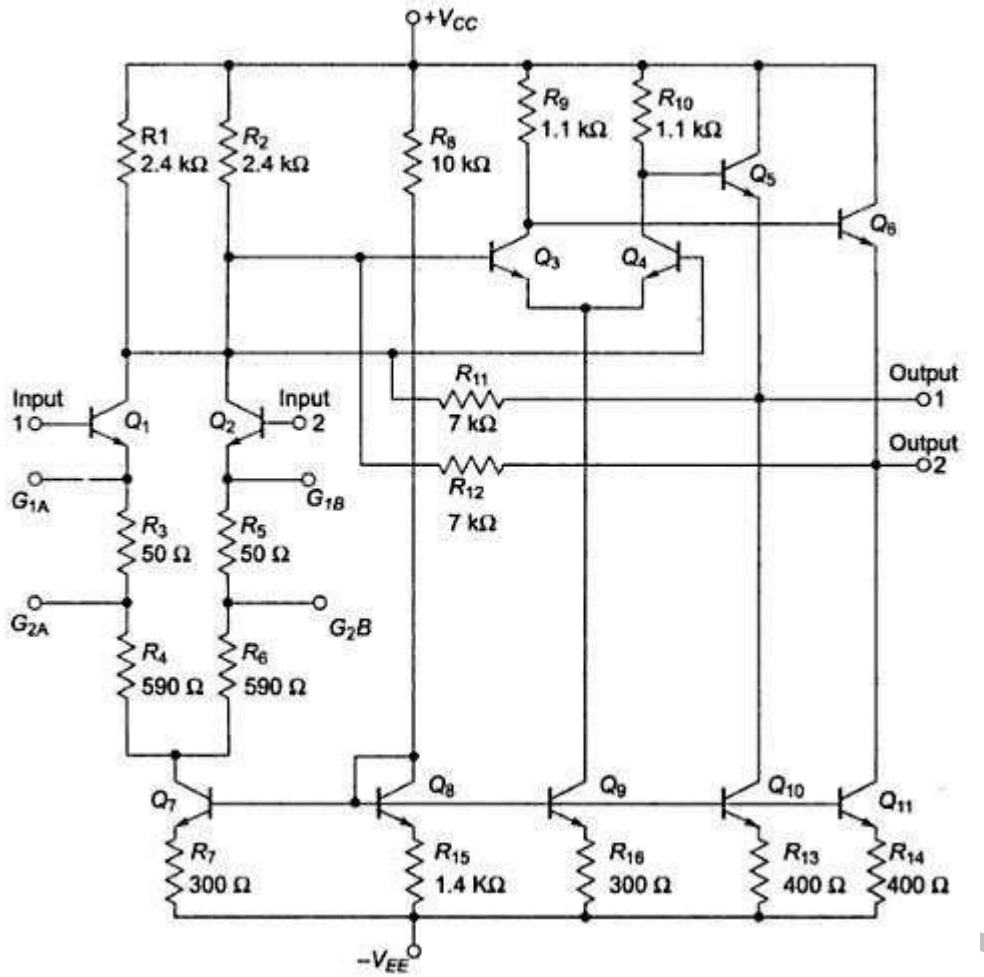


Figure 5.12.2. Monolithic video amplifier

[source: http://www.elektronikjk.pl/elementy_czynne/IC/UA733-2.pdf]

5.13 ISOLATION AMPLIFIER

An isolation amplifier or a unity gain amplifier provides isolation from one fraction of the circuit to another fraction. So, the power cannot be drawn, used and wasted within the circuit. The main function of this amplifier is to increase the signal. The same input signal of the op-amp is passed out exactly from the op-amp as an output signal. These amplifiers are used to give an electrical safety battier as well as isolation. These amplifiers protect the patients from the outflow of current. They crack electrical signal's ohmic continuity among input & output and isolated power supply can be provided for both the input and output. So, the low-level signals can be amplified.

An isolation amplifier can be defined as, an amplifier which doesn't have any conductive contact among input as well as output sections. Consequently, this amplifier gives ohmic isolation among the i/p & o/p terminals of the amplifier. This isolation must have less leakage as well as a high amount of dielectric breakdown voltage. The typical resistor and capacitor values of amplifier among the input & output terminals are resistor should have 10 Tera Ohms and capacitor should have 10 picofarads.

These amplifiers are frequently used when there is extremely huge common-mode voltage disparity among input & output side. In this amplifier, the ohmic circuitry is not there from input ground to output ground.

ISOLATION AMPLIFIER DESIGN METHODS

There are three kinds of design methods are used in isolation amplifiers which include the following.

- Transformer Isolation
- Optical Isolation
- Capacitive Isolation

1). TRANSFORMER ISOLATION

This type of isolation uses two signals like PWM or frequency modulated. Internally, this amplifier includes 20 KHz oscillator, rectifier, filter, and transformer to give supply to every isolated stage.

- The rectifier is used as an input to the main op-amp.
- Transformer links the supply.
- The oscillator is used as an input to the secondary op-amp.
- An LPF is used for removing the components of other frequency.
- The advantages of transformer isolation mainly include high CMRR, linearity, and accuracy.
- The applications of transformer isolation mainly include medical, nuclear and industrial.

2). OPTICAL ISOLATION

In this isolation, the l signal can be changed from biological to light signal with LED for further process. In this, the patient circuit is input circuit whereas the output circuit can be formed by a phototransistor. These circuits are operated with a battery. The i/p circuit changes the signal into the light as well as the o/p circuit changes the light back to the signal.

- The advantages of optical isolation mainly include;
- By using this we can obtain amplitude and original frequency.
- It connects optically without the need of modulator otherwise demodulator.
- It improves the safety of the patient.

The applications of transformer isolation mainly include process control in industries, data acquisition, measurements of biomedical, monitoring of the patient, interface element, test equipment, controlling of SCR, etc.

3). CAPACITIVE ISOLATION

- It uses frequency modulation and the input voltage’s digital encoding.
- The input voltage can be changed to relative charge over the switched capacitor.
- It includes circuits like modulator as well as a demodulator.

- The signals are sent across a differential capacitive barrier.
- For both sides, separate supplied are given.
- The advantages of capacitive isolation mainly include;
- This isolation can be used to remove ripple noises
- These are used for analog systems
- It includes linearity and high-gain stability.
- It gives high immunity to magnetic noises
- By using this, noise can be avoided.
- The applications of capacitive isolation mainly include data acquisition, interface element, monitoring of the patient, EEG, and ECG.

IC ISO 100 ISOLATION AMPLIFIER

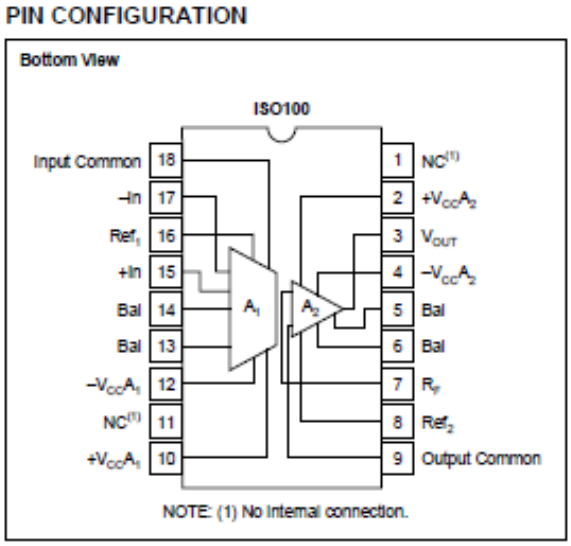


Figure 5.13.1 Pin configuration of ISO100

[source:"Linear Integrated Circuits"by S.Salivahanan& V.S. Kanchana Bhaskaran, Page-539]

FEATURES

- Easy to use, similar to an OP AMP
- VOUT/IIN = RF, Current Input
- VOUT/VIN = RF/RIN, Voltage Input
- 100% tested for breakdown:

- 750V Continuous Isolation Voltage
- Ultra-low leakage: 0.3mA, max, at
- 240V/60Hz
- Wide bandwidth: 60kHz
- 18-PIN DIP PACKAGE

OPERATION OF ISO100

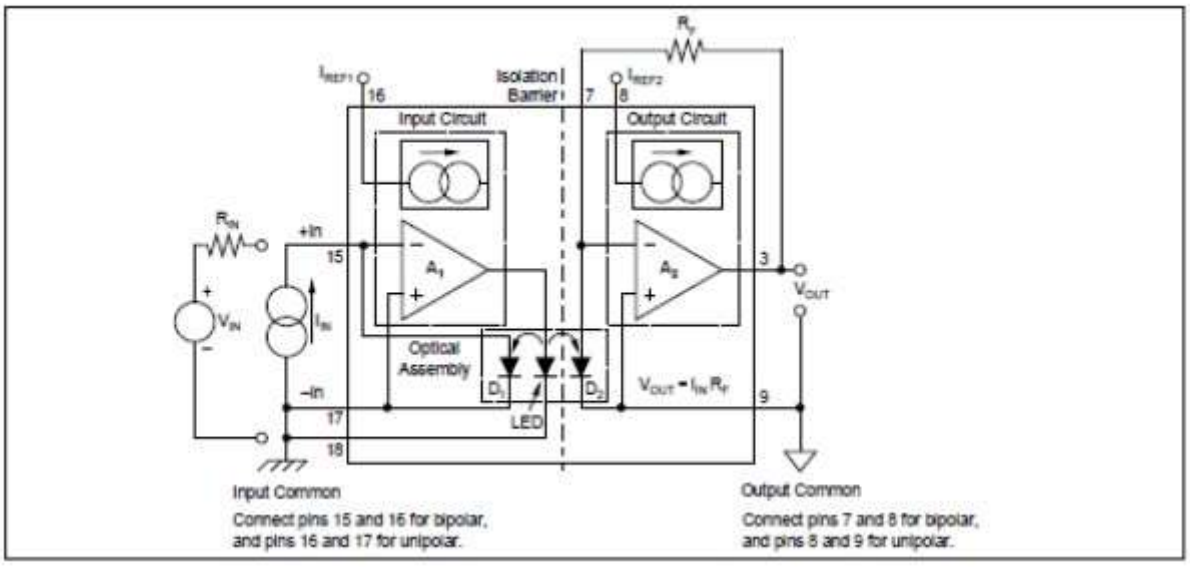


Figure 5.13.2 simplified block diagram of ISO100

[source:"Linear Integrated Circuits"by S.Salivahanan& V.S. Kanchana Bhaskaran, Page-70]

Pin configuration is shown in figure 5.13.1.And Figure 5.13.2 is the simplified block diagram of ISO100.In figure 5.13.2, assume a current, IIN, flows out of the ISO100 (IIN must be negative in unipolar operation). This causes the voltage at pin 15 to decrease. Because the amplifier is inverting, the output of A1 increases, driving current through the LED. As the LED light output increases, D_1 responds by generating an increasing current. The current increases until the sum of the currents in and out of the input node (–Input to A1) is zero. At that point, the negative feedback through D_1 has stabilized the loop, and the current I_{D1} equals the input current plus the bias current. As a result, no bias current flows in the source. Since D_1 and D_2 are matched ($I_{D1} = I_{D2}$), I_{IN} is replicated at the output via D_2. Thus, A_1 functions as

a unity-gain current amplifier, and A_2 is an current-to-voltage converter, as described below. Current produced by D_2 must either flow into A_2 or R_F. Since A_2 is designed for low bias current (»10nA), almost all of the current flows through R_F to the output. The output voltage then becomes:

$$V_O = (I_{D2})R_F = (I_{D1} \pm I_{OS})R_F = -(-I_{IN})R_F = I_{IN}R_F \quad (1)$$

where, I_{OS} is the difference between A_1 and A_2 bias currents.

For input voltage operation I_{IN} can be replaced by a voltage source (V_{IN}) and series resistor (R_{IN}), since the summing node of the op amp is essentially at ground. Thus,

$$I_{IN} = V_{IN}/R_{IN}.$$

Unipolar operation does have some constraints, however. In this mode the input current must be negative so as to produce a positive output voltage from A_1 to turn the LED on. A current more negative than 20nA is necessary to keep the LED turned on and the loop stabilized. When this condition is not met, the output may be in determinant. Many sensors generate unidirectional signals, e.g., photoconductive and photodiode devices, as well as some applications of thermocouples. However, other applications do require bipolar operation of the ISO100.

BIPOLAR OPERATION

To activate the bipolar mode, reference currents as shown in Figure 1 are attached to the input nodes of the op amps. The input stage stabilizes just as it did in unipolar operation. Assuming $I_{IN} = 0$, the photodiode has to supply all the I_{REF1} current. Again, due to symmetry, $I_{D1} = I_{D2}$. Since the two references are matched, the current generated by D_2 will equal I_{REF2}. This results in no current flow in RF, and the output voltage will be zero. When IIN either adds or subtracts current from the input node, the current D_1 will adjust to satisfy $I_{D1} = I_{IN} + I_{REF1}$. Because I_{REF1} equals I_{REF2} and I_{D1} equals I_{D2}, a current equal to I_{IN} will flow in R_F. The output voltage is then VO = $I_{IN}R_F$. The range of allowable I_{IN} is limited. Positive I_{IN} can be as large as IREF1 (10.5mA, min). At this point, D_1 supplies no current and the loop opens. Negative I_{IN} can be as large as that generated by D_1 with maximum LED output (recommended 10mA, max).

DC ERRORS

Errors in the ISO100 take the form of offset currents and voltages plus their drifts with temperature. These are shown in Figure 5.13.3. *A_1 and A_2*— assumed to be ideal amplifiers. *V_{OSO} and V_{OSI}*—the input offset voltages of the output and input stage, respectively. V_{OSO} appears directly at the output, but, VOSI appears at the output as $V_{OSI}\frac{RF}{R_{IN}}$, see equation (2).

I_{OS}—the offset current. This is the current at the input necessary to make the output zero. It is equal to the combined effect of the difference between the bias currents of A_1 and A_2 and the matching errors in the optical components in the unipolar mode. *I_{REF1} and I_{REF2}*—reference currents that, when connected to the inputs, enable bipolar operation. The two currents are trimmed, in the bipolar mode, to minimize the $I_{OS\ BIPOLAR}$ error. *I_{D1} and I_{D2}*—currents generated by each photodiode in response to the light from the LED.

Ae—gain error.

$$Ae = |\ \text{Ideal gain/Actual gain}\ | - 1$$

The output then becomes:

$$V_{OUT} = R_F[(\frac{VIN \pm VOS}{R_{IN}} - I_{REF1} \pm I_{OS})(1 + Ae) + I_{REF2}] \pm V_{OSO}\ (2)$$

The total input referred offset voltage of the ISO100 can be simplified in the unipolar case in fig4 by assuming that Ae = 0 and

$$V_{IN} = 0:$$

$$V_{OUT} = R_F\left[\frac{\pm V_{OSI}}{R_{IN}} \pm I_{OS\ UNIPOLAR}\right] \pm V_{OSO}\ (3)$$

Circuit Techniques for Reducing Noise from the current sources in the Bipolar Mode is in figure 5.13.5 This voltage is then referred back to the input by dividing by R_F/R_{IN}.

$$V_{OS}\,(R_{TI}) = (\pm V_{OSI}) \pm R_{IN}\,(I_{OS\ UNIPOLAR}) + V_{OSO}/(R_F/R_{IN})$$

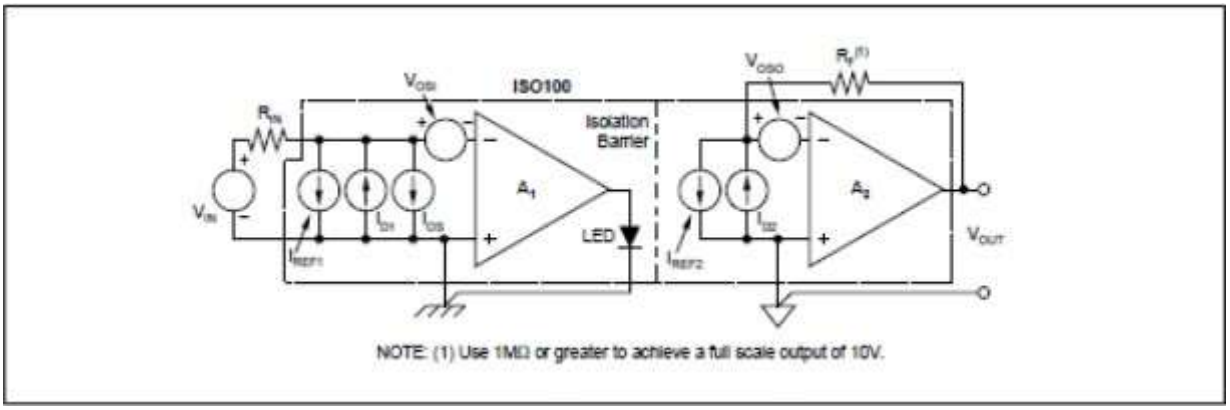


Figure 5.13.3 Circuit model for Dc errors in ISO100

[source:"Linear Integrated Circuits"by S.Salivahanan& V.S. Kanchana Bhaskaran, Page-539]

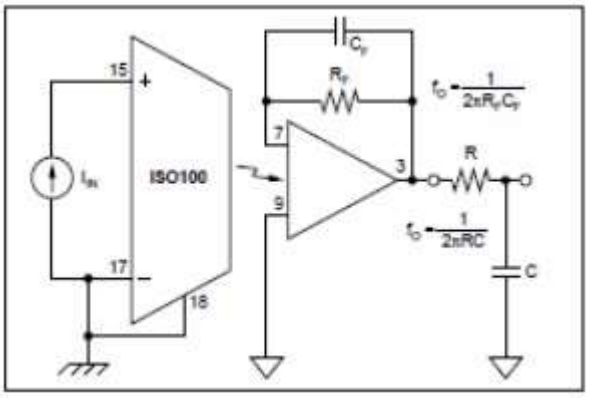


Figure 5.13.4 Two circuit Techniques for Reducing Noise in unipolar Mode

[source:"Linear Integrated Circuits"by S.Salivahanan& V.S. Kanchana Bhaskaran, Page-540]

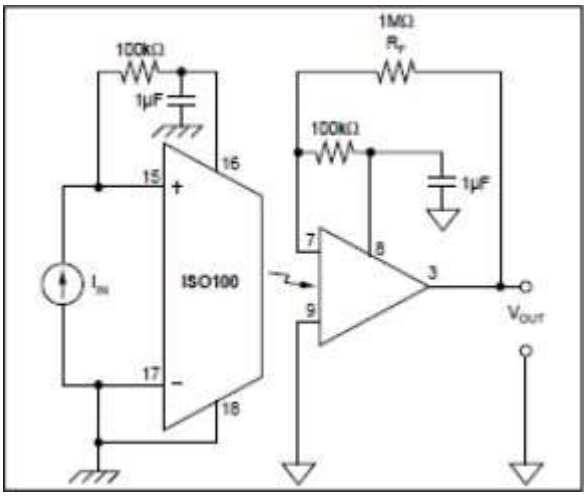


Figure 5.13.5 circuit Techniques for Reducing Noise from the current sources in the Bipolar Mode

[source:"Linear Integrated Circuits"by S.Salivahanan& V.S. Kanchana Bhaskaran, Page-539]

5.10 FREQUENCY TO VOLTAGE CONVERTORS (F-V)

- F-V convertors applications: Tachometer in motor speed control Rotational speed measurement.
- Ideal characteristics of V-F converter and F-V converter is shown in figure 5.10.1.
- Two types of it: Pulse integrating Phase locked loop

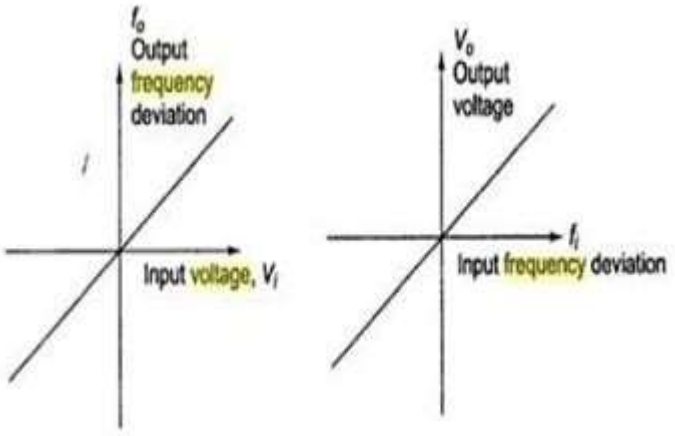


Figure 5.10.1 Ideal characteristics of V-F converter and F-V converter

[source: https://www.brainkart.com/subject/Linear-Integrated-Circuits_220/]

- F-V convertor produces an output voltage whose amplitude is a function of input signal frequency.
- $V_0=k_f f_i$ k_f is sensitivity of F-V convertor
- Frequency to voltage converter using VFC32 is shown in figure 5.10.2.
- It is basically a FM discriminator.

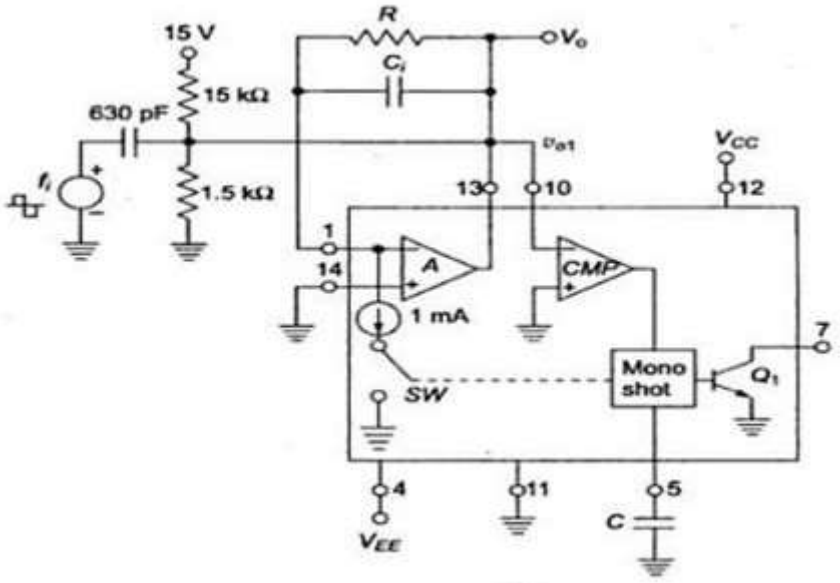


Figure 5.10.2 Frequency to voltage converter using VFC32

[source: https://www.brainkart.com/subject/Linear-Integrated-Circuits_220/]

- Input frequency is applied to comparator A.
- Resistor R acts as feedback element.
- Capacitor Ci enables charge-balancing,
- High pass network conditions input signal

For negative spike of V 01, comparator COMP triggers one shot multivibrator with threshold 7.5V The output of multivibrator closes the switch SW, for a time TH, this causes voltage Vo to build up and inject thru R and this continues until current out of summing input of opamp is equal to that injected by Vo through R continuously. Input –output characteristics of Frequency to voltage converter using VFC32 is shown in figure 5.10.3

$$Vo=10^{-3} *T_H *R*fi \qquad \text{as } T_H = 7.5\ C\ /1X10^{-3}$$

Ripple Voltage, Vr(max) =7.5 C /Ci

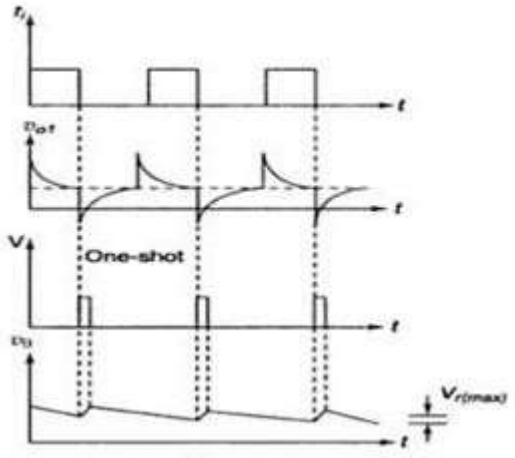


Figure 5.10.3 input –output characteristics

[source: https://www.brainkart.com/subject/Linear-Integrated-Circuits_220/]

VOLTAGE TO FREQUENCY CONVERTOR

Principle: Charge balancing technique-the process of charging and discharging results in frequency proportional to input signal F0= k Vi

Operation: Op-amp A converts input V_i to current $I_i = V_i/R$ into summing junction.When switch SW is open the current flows into capacitor Ci and charges it, and node voltage V_{o1} produce ramp down.When V_{01} =0 CMP triggers and sends a triggering signal to one shot multivibrator that closes the switch SW and turns transistor Q ON for time T_H. Voltage – Frequency using VF32 and its input –output characteristics is shown in figure 5.10.4.

The threshold of mono shot = 7.5 V and $T_H = 7.5\ C/10^{-3}$

During T_H , V_{01} ramps upward by amount $\Delta V_{01}=(1mA-I_i)\ T_H\ /C_i$

Time duration TL for vo1 to return to 0 is $TL = C\Delta V_{01}/I_i$

$$T_L+T_H = 1mA\ T_H\ /I_i \quad = T$$

$$F_0=V_i/7.5\ RC$$

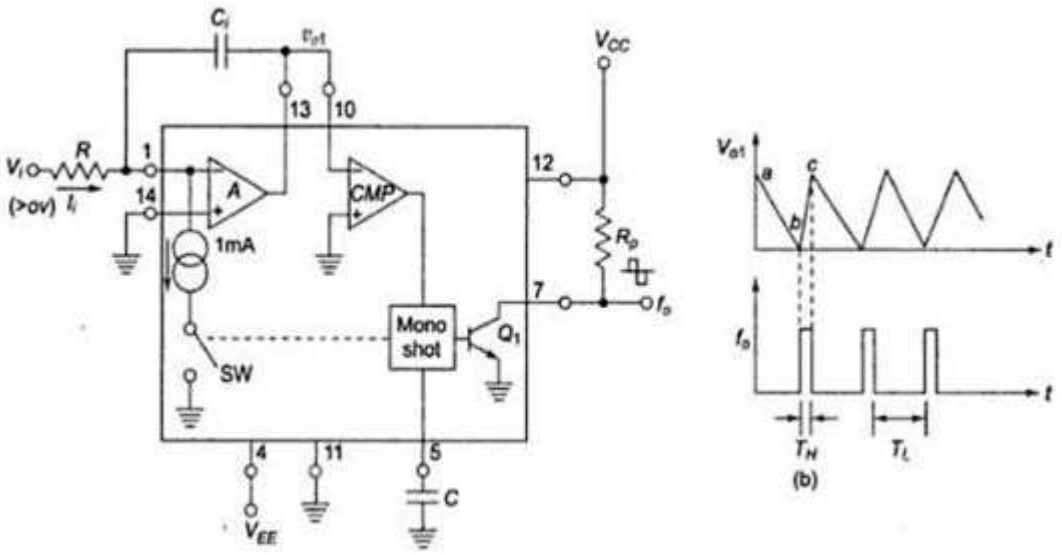


Figure 5.10.4 Voltage –Frequency using VF32 and its input –output characteristics

[source: https://www.brainkart.com/subject/Linear-Integrated-Circuits_220/]

5.6 IC 723 – GENERAL PURPOSE REGULATOR

Disadvantages of fixed voltage regulator:

1. Do not have the shot circuit
2. Output voltage is not adjustable

These limitations can be overcomes in IC723.

Features of IC723:

1. Unregulated dc supply voltage at the input between 9.5V & 40V
2. Adjustable regulated output voltage between 2 to 3V.
3. Maximum load current of 150 mA (ILmax = 150mA).
4. With the additional transistor used, ILmax upto 10A is obtainable.
5. Positive or Negative supply operation
6. Internal Power dissipation of 800mW.
7. Built in short circuit protection.
8. Very low temperature drift.
9. High ripple rejection.

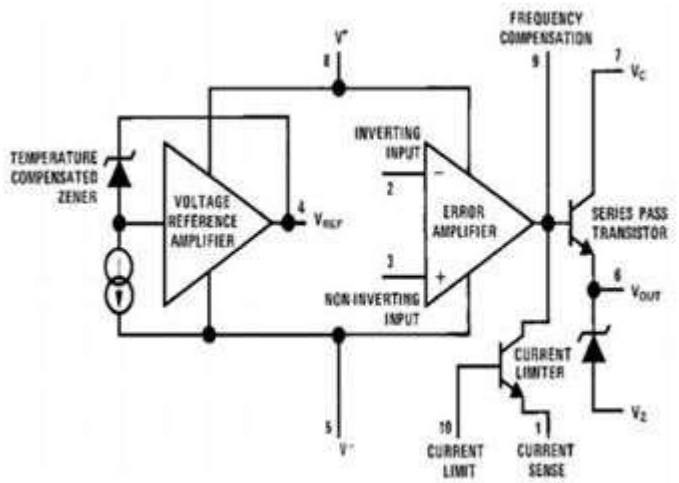


Figure 5.6.1 Functional block diagram of IC723

[source: https://www.brainkart.com/subject/Linear-Integrated-Circuits_220/]

Functional block diagram of IC723 is shown in figure 5.6.1.The simplified functional block diagram can be divided in to 4 blocks.

1. Reference Generating block:

The temperature compensated Zener diode, constant current source & voltage reference amplifier together from the reference generating block. The Zener diode is used to generate a fixed reference voltage internally. Constant current source will make the Zener diode to operate at affixed point & it is applied to the Non – inverting terminal of error amplifier. The Unregulated input voltage ±Vcc is applied to the voltage reference amplifier as well as error amplifier.

2. Error Amplifier:

Error amplifier is a high gain differential amplifier with 2 input (inverting & Non-inverting). The Non-inverting terminal is connected to the internally generated reference voltage. The Inverting terminal is connected to the full regulated output voltage.

3. Series Pass Transistor:

Q1 is the internal series pass transistor which is driven by the error amplifier. This transistor actually acts as a variable resistor & regulates the output voltage. The collector of transistor Q1 is connected to the Un-regulated power supply. The maximum collector voltage of Q1 is limited to 36Volts. The maximum current which can be supplied by Q1 is 150mA.

4. Circuitry to limit the current:

The internal transistor Q2 is used for current sensing & limiting. Q2 is normally OFF transistor. It turns ON when the IL exceeds a predetermined limit.Low voltage, Low current is capable of supplying load voltage which is equal to or between 2 to 7Volts.Pin diagram of IC723 in figure 5.6.2.

$$V_{load} = 2 \text{ to } 7V \text{ and } I_{load} = 50mA$$

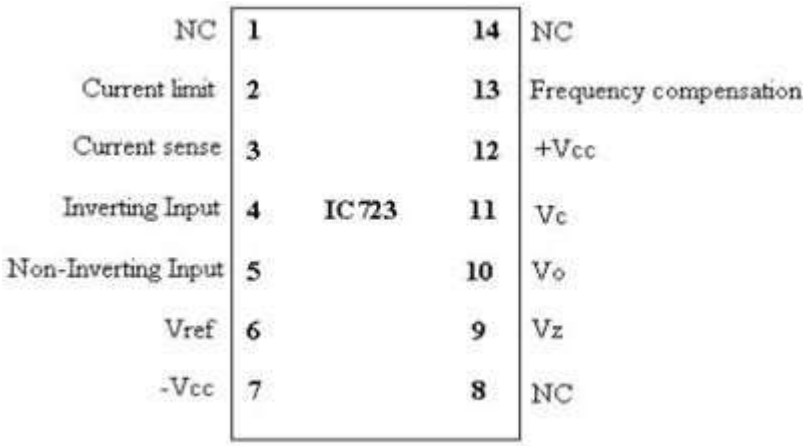


Figure 5.6.2.Pin diagram of IC723

[source: https://www.brainkart.com/subject/Linear-Integrated-Circuits_220/]

IC723 as a LOW voltage LOW current:

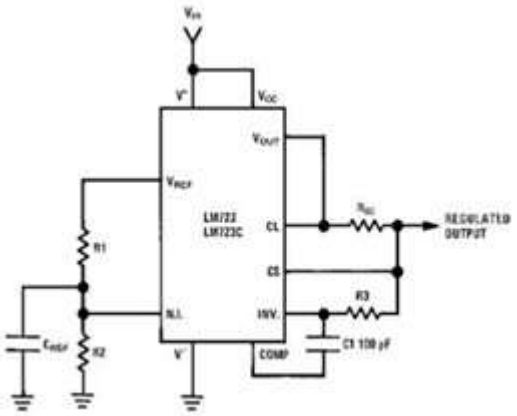


Figure 5.6.3.Typical circuit connection diagram

[source: https://www.brainkart.com/subject/Linear-Integrated-Circuits_220/]

- Circuit connection is shown in fig 3.R_1 & R_2 from a potential divider between V_{ref} & Gnd.
- The Voltage across R_2 is connected to the Non – inverting terminal of the regulator

$$I_C\ V_{non\text{-}inv} = R_2/(R_1+R_2)\ Vref$$

- Gain of the internal error amplifier is large

$$V_{non\text{-}inv} = V_{in}$$

- Therefore the Vo is connected to the Inverting terminal through R_3 & R_{SC} must also

be equal to $V_{non-inv}$

$$V_o = V_{non-inv} = R_2/(R_1+R_2)\ V_{ref}$$

R_1 & R_2 can be in the range of 1 KΩ to 10KΩ & value of R3 is given by

$$R_3 = R_1 ll\ R_2 = R_1R_2/(R_1+R_2)$$

Rsc (current sensing resistor) is connected between Cs & CL. The voltage drop across Rsc is proportional to the IL.

- This resistor supplies the output voltage in the range of 2 to 7 volts, but the load current can be higher than 150mA.
- The current sourcing capacity is increased by including a transistor Q in the circuit.
- The output voltage , Vo $= R_2/(R_1+R_2)\ V_{ref}$

IC723 as a HIGH voltage LOW Current:

- This circuit is capable of supplying a regulated output voltage between the ranges of 7 to 37 volts with a maximum load current of 150 mA.

- The Non – inverting terminal is now connected to V_{ref} through resistance R_3.
- The value of R_1 & R_2 is adjusted in order to get a voltage of Vref at the inverting terminal at the desired output.

$$V_{in} = V_{ref} = R_2/(R_1+R_2)V_0$$

$$V_o = [1+R_1/R_2]\ V_{in}$$

- Rsc is connected between CL & Cs terminals as before & it provides the shortCircuit current limiting Rsc =0.6/Ilimit
- The value of resistors R3 is given by ,

$$R_3 = R_1 ll\ R_2 = R_1R_2/(R_1+R_2)$$

IC723 as a HIGH voltage HIGH Current:

- An external transistor Q is added in the circuit for high voltage low current regulator to improve its current sourcing capacity. Circuit connection of IC 723 as a High voltage High current regulator is shown in figure 5.6.4. below

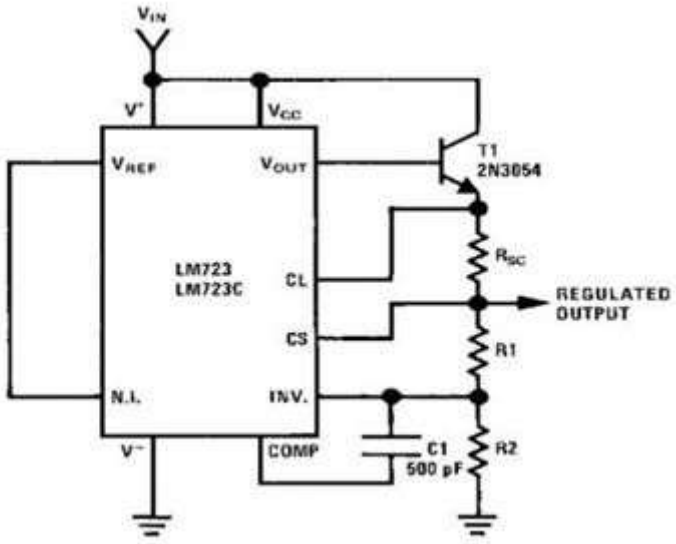


Figure 5.6.4.Circuit connection of IC 723 as a High voltage High current regulator

[source: https://www.brainkart.com/subject/Linear-Integrated-Circuits_220/]

- For this circuit the output voltage varies between 7 & 37V.
- Transistor Q increase the current sourcing capacity thus IL (MAX) is greater than 150mA.
- The output voltage Vo is given by ,

$$V_0 = Vo = [1+R_1/R_2]\ V_{in}$$

$$Rsc = 0.6/I\ limit$$

5.5 LINEAR REGULATORS

- All electronic circuits need a dc power supply for their operation. To obtain this dc voltage from 230 V ac mains supply, we need to use rectifier.
- Therefore the filters are used to obtain a "steady" dc voltage from the pulsating one.
- The filtered dc voltage is then applied to a regulator which will try to keep the dc output voltage constant in the event of voltage fluctuations or load variation.

The combination of rectifier & filter can produce a dc voltage. But the problem with this type of dc power supply is that its output voltage will not remain constant in the event of fluctuations in an AC input or changes in the load current(IL).

- The output of unregulated power supply is connected at the input of voltage regulator circuit.
- The voltage regulator is a specially designed circuit to keep the output voltage constant. It does not remain exactly constant. It changes slightly due to changes in certain parameters.

Factors affecting the output voltage:

i) I_L (Load Current)

ii) V_{IN} (Input Voltage)

iii) T (Temperature)

IC VOLTAGE REGULATORS

They are basically series regulators.

Important features of IC Regulators:

1. Programmable output
2. Facility to boost the voltage/current
3. Internally provided short circuit current limiting
4. Thermal shutdown

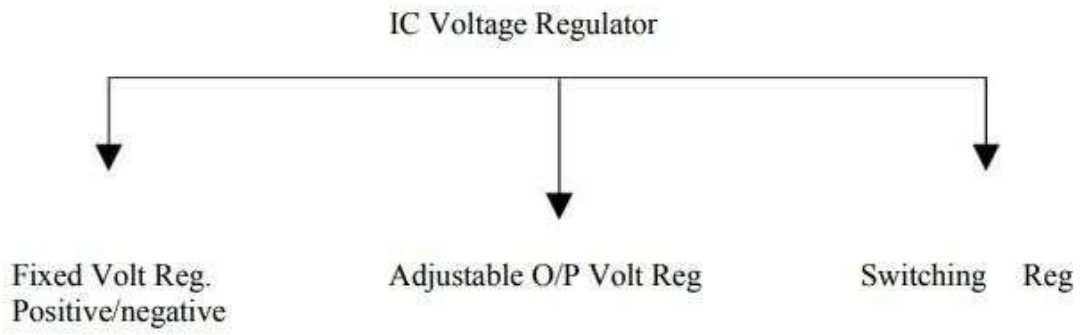
5. Floating operation to facilitate higher voltage output

Classifications of IC voltage regulators:

a. Fixed Volt Reg. Positive/negative

b. Adjustable O/P Volt Reg

c. Switching Reg



- Fixed & Adjustable output Voltage Regulators are known as Linear Regulator.
- A series pass transistor is used and it operates always in its active region.

SWITCHING REGULATOR

1. Series Pass Transistor acts as a switch.
2. The amount of power dissipation in it decreases considerably.
3. Power saving result is higher efficiency compared to that of linear.

ADJUSTABLE VOLTAGE REGULATOR

Advantages of Adjustable Voltage Regulator over fixed voltage regulator are,

1. Adjustable output voltage from 1.2v to 57 v
2. Output current 0.10 to 1.5 A
3. Better load & line regulation
4. Improved overload protection
5. Improved reliability under the 100% thermal overloading

ADJUSTABLE POSITIVE VOLTAGE REGULATOR (LM317)

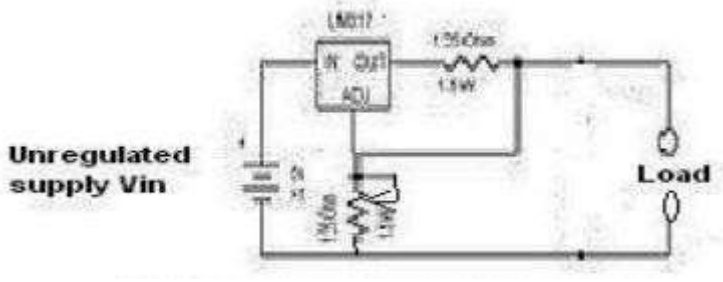


Figure 5.5.1 LM317 Regulator circuit Diagram

[source: https://www.brainkart.com/subject/Linear-Integrated-Circuits_220/]

1. LM317 series adjustable 3 terminal positive voltage regulator, the three terminals are Vin, V_{out} & adjustment (ADJ).Figure 5.5.1.shows the LM317 Regulator circuit.
2. LM317 requires only 2 external resistors to set the output voltage.
3. LM317 produces a voltage of 1.25v between its output & adjustment terminals. This voltage is called as V_{ref}.
4. V_{ref} (Reference Voltage) is a constant, hence current I1 flows through R1 will also be constant. Because resistor R1 sets current I1. It is called "current set" or "program resistor".
5. Resistor R2 is called as "Output set" resistors, hence current through this resistor is the sum of I1 & I_{adj}
6. LM317 is designed in such as that I_{adj} is very small & constant with changes in line voltage & load current.
7. The output voltage Vo is, $V_o=R_1I_1+(I_1+I_{adj})R_2$ ---------- (1)

Where $I_1= V_{ref}/R_1$

$$V_o = (V_{ref}/R_1)\, R_1 + V_{ref}/R_1 + I_{adj}\, /R_2$$

$$= V_{ref} + (V_{ref}/R_1)\, R_2 + I_{adj}\, R_2$$

$$V_o = V_{ref}\, [1 + R_2/R_1] + I_{adj}\, R_2 \text{ ----------} (2)$$

R_1 = Current (I1) set resistor

R_2 = output (Vo) set resistor.

V_{ref} = 1.25v which is a constant voltage between output and ADJ terminals.

- Current I_{adj} is very small. Therefore the second term in (2) can be neglected.
- Thus the final expression for the output voltage is given by

$$Vo = 1.25v[1 + R_2/R_1] \text{----------} (3)$$

Eqn (3) indicates that we can vary the output voltage by varying the resistance R_2. The value of R_1 is normally kept constant at 240 ohms for all practical applications.

PRACTICAL REGULATOR USING LM317

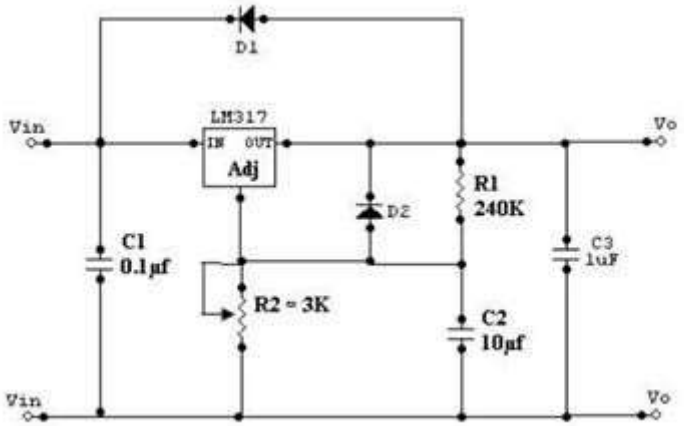


Figure 5.5.2 Practical Regulator

[source: https://www.brainkart.com/subject/Linear-Integrated-Circuits_220/]

- Practical Regulator is shown in figure 5.5.2.If LM317 is far away from the input power supply, then 0.1µf disc type or 1µf tantalum capacitor should be used at the input of LM317.
- The output capacitor Co is optional. Co should be in the range of 1 to 1000µf.
- The adjustment terminal is bypassed with a capacitor C2 this will improve the ripple
- rejection ratio as high as 80 dB is obtainable at any output level.
- When the filter capacitor is used, it is necessary to use the protective diodes.
- These diodes do not allow the capacitor C2 to discharge through the low current point of the regulator.
- These diodes are required only for high output voltages (above 25v) & for higher values of output capacitance 25µf and above.

5.3 FUNCTION GENERATOR IC 8038:

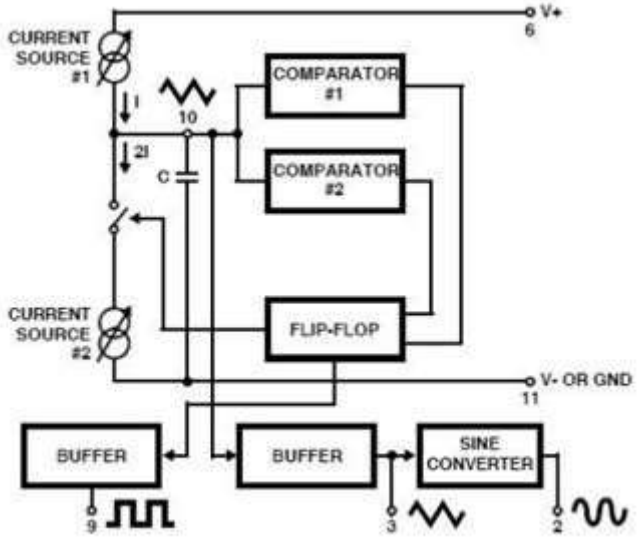


Figure 5.3.1 Functional block diagram of Function Generator IC 8038

[source: https://www.brainkart.com/subject/Linear-Integrated-Circuits_220/]

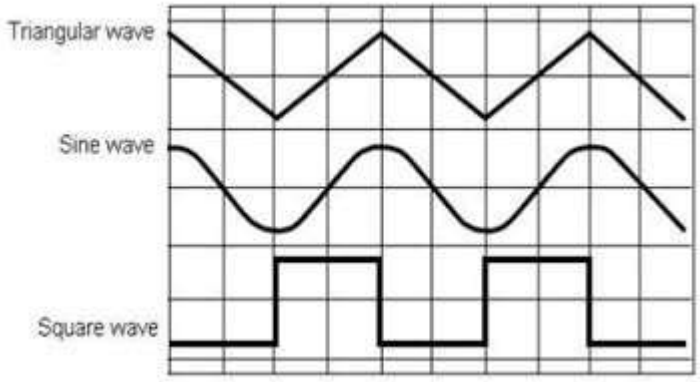


Figure 5.3.2 Output waveforms of IC 8038

[source: https://www.brainkart.com/subject/Linear-Integrated-Circuits_220/]

It consists of two current sources, two comparators, two buffers, one FF and a sine wave converter. .Functional block diagram of Function Generator IC 8038 is shown in figure 5.3.1.and the Output waveforms of IC 8038 is shown in figure 5.3.2.

Pin description:

- Pin 1 & Pin 12: Sine wave adjusts:

The distortion in the sine wave output can be reduced by adjusting the 100KΩ pots connected between pin12 & pin11 and between pin 1 & 6.

- Pin 2 Sine Wave Output:

Sine wave output is available at this pin. The amplitude of this sine wave is 0.22 Vcc. Where ± 5V ≤ Vcc ≤ ± 15 V.

- Pin 3 Triangular Wave output:

Triangular wave is available at this pin. The amplitude of the triangular wave is 0.33Vcc.Where ± 5V ≤ Vcc ≤ ± 15 V.

- Pin 4 & Pin 5 Duty cycle / Frequency adjust:

The symmetry of all the output wave forms & 50% duty cycle for the square wave output is adjusted by the external resistors connected from Vcc to pin 4. These external resistors & capacitors at pin 10 will decide the frequency of the output wave forms.

- Pin 6 + Vcc:

Positive supply voltage the value of which is between 10 & 30V is applied to this pin.

- Pin 7 : FM Bias:

This pin along with pin no8 is used to TEST the IC 8038.

- Pin 9 : Square Wave Output:

A square wave output is available at this pin. It is an open collector output so that this pin can be connected through the load to different power supply voltages. This arrangement is very useful in making the square wave output.

- Pin 10 : Timing Capacitors:

The external capacitor C connected to this pin will decide the output frequency along with the resistors connected to pin 4 & 5.

- Pin 11 : -VEE or Ground:

If a single polarity supply is to be used then this pin is connected to supply ground & if (±) supply voltages are to be used then (-) supply is connected to this pin.

- Pin 13 & Pin 14: NC (No Connection)

Important features of IC 8038:

1. All the outputs are simultaneously available.
2. Frequency range : 0.001Hz to 500kHz
3. Low distortion in the output wave forms.
4. Low frequency drifts due to change in temperature.
5. Easy to use.

Parameters:

(i) Frequency of the output wave form:

The output frequency dependent on the values of resistors R_1 & R_2 along with the external capacitor C connected at pin 10.If $R_A = R_B = R$ & if RC is adjusted for 50% duty cycle then $f_0 = 0.3/RC$; $R_A = R_1$, $R_B = R_3$, $RC = R_2$.

(ii) Duty cycle / Frequency Adjust : (Pin 4 & 5):

Duty cycle as well as the frequency of the output wave form can be adjusted by external resistors at pin 4 & 5.The values of resistors RA & RB connected between Vcc pin 4 & 5 respectively along with the capacitor connected at pin 10 decide the frequency of the wave form. The values of RA & RB should be in the range of 1kΩ to 1MΩ.

(iii)FM Bias:

- The FM Bias input (pin7) corresponds to the junction of resistors R1 & R2.
- The voltage Vin is the voltage between Vcc & pin8 and it decides the output frequency.
- The output frequency is proportional to Vin as given by the following expression.

For $R_A = R_B$ (50% duty cycle).

$f_0 = 5\ V_{in}/CR_AVcc$; where C is the timing capacitor.

- With pin 7 & 8 connected to each other the output frequency is given by f0= 0.3/RC where R = RA = RB for 50% duty cycle.
- This is because M Sweep input (pin 8):

$$Vin=R1Vcc/R1+R2$$

- This input should be connected to pin 7, if we want a constant output frequency.But if the output frequency is supposed to vary, then a variable dc voltage should be applied to this pin.
- The voltage between Vcc & pin 8 is called Vin and it decides the output frequency as,

$$f_0=1.5\ V_{in}/CR_AV_{CC}$$

A potentiometer can be connected to this pin to obtain the required variable voltage required to change the output frequency.

5.8 LOW DROP-OUT (LDO) REGULATOR

The disadvantage of the typical 78XXseries and LM317 type of regulators is that the devices require a minimum voltage $V_{DO,}$ called the drop-out voltage. This is the minimum voltage difference between input and output terminals needed to regulate the supply voltage within the specifications. To cite an example. the IC µA7805 with I_o=1A needs V_{DO} =2.5V maximum. This indicates that the minimum unregulated input voltage V_i must never be less than

$$V_{i,min} = V_{ref} + V_{DO} = 5V + 2.5V$$

Similarly, the LM317 type of regulator needs at least 3 V between the input and output leads to produce power to the internal circuits. Hence, in typical applications, involving batteries whose voltage can easily drop from 12V to as low as 6V such as in the case of car battery, the dropout voltage is a detrimental factor.

The LDO regulator shown in figure 5.8.1 is ideal for such applications. This is a simple modification of the LM317 circuit. It employs a PNP BJT as the series element to drive the output. The second PNP transistor Q_2 buffers the error amplifier output.

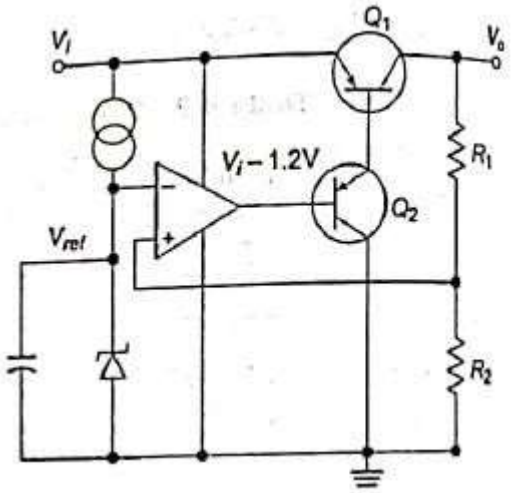


Figure 5.8.1.Low drop –out positive voltage regulator

[source:"Linear Integrated Circuits"by S.Salivahanan& V.S. Kanchana Bhaskaran, Page374]

The op-amp output is maintained at $V_i - 1.2V$. The voltage at the junction of resistors R_1 and R_2 is fed to the non-inverting input of the error amplifier. When this voltage is more than the reference voltage set by the zener diode, the output of the op-amp goes positive.

This reduces the base current of transistor Q_2,which in turn reduces the base current drive to series element Q_1.Thus the circuit realizes a minimum voltage of about 0.2 V, being the $V_{EC(sat)}$ voltage between V_i and V_o terminals. It is noted that the transistor base drive from the op-amp is relative to the input voltage V_i.

The IC LM2941 is a typical low drop-out positive voltage regulator. It can source an output current of 1A with a typical drop out voltage of 0.5V and a maximum of 1V over the entire temperature range. This IC has a quiescent current reduction circuit which reduces the ground terminal current if the differential voltage across the input and output terminals exceeds approximately 3V.The quiescent current is only 30mA while providing with 1A of output current and an input to output differential voltage of 5V.Higher quiescent currents exist only when the regulator is in the drop-out mode ($V_i - V_o \leq 3V$).These types of regulators are mainly used for vehicular applications.

The LM2941 is protected from reverse battery installations or two-battery jumps.During accidental line transients or when the input voltage momentarily exceed the specified maximum operating voltage, the regulator will automatically switch to shut-dowm mode.This protects both the internal circuits and the load.Futhermore ,the short circuit and termal overload protection features are also provided. Figure 5.8.2 shows the TO-220 Plastic,TO-263 and 8-Lead LLP surface mount packages.Figure 5.8.3 shows a typical regulator circuit using LM2941 to provide a regulated output voltage of 5V to 20V.

$$V_o = V_{ref}\left[1+\frac{R_2}{R_1}\right], where\ V_{ref} = 1.275V\ (Typically)$$

$$R_2 = R_1\left(\frac{V_o}{V_{ref}}\right) - 1$$

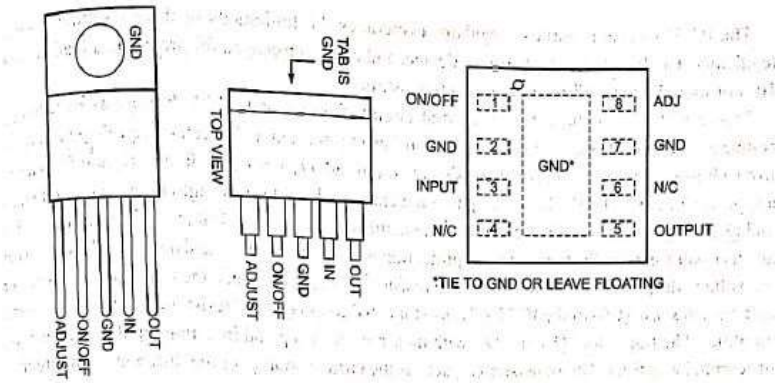


Figure 5.8.2 TO-220 Plastic,TO-263 and 8-Lead LLP surface mount packages

[source:"Linear Integrated Circuits"by S.Salivahanan& V.S. Kanchana Bhaskaran, Page-375]

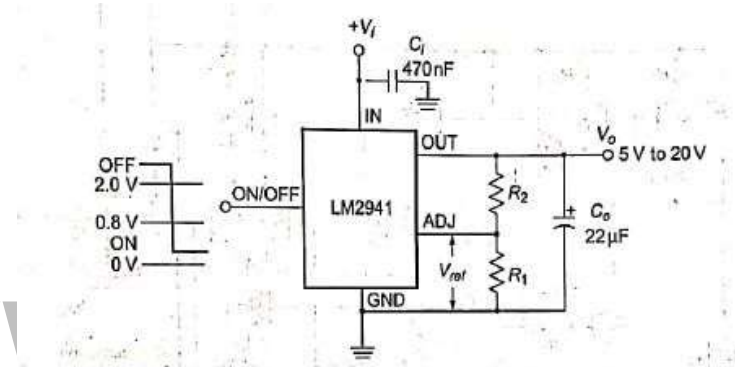


Figure 5.8 3 5V to 2V regulator circuit using LM2941

[source:"Linear Integrated Circuits"by S.Salivahanan& V.S. Kanchana Bhaskaran, Page-375]

5.7 MONOLITHIC SWITCHING REGULATOR [µA78S40]

The µA78S40 consists of a temperature compensated voltage reference, duty cycle controllable oscillator with an active current limit circuit, a high gain comparator, a high-current, high voltage output switch, a power switching diode & an uncommitted op-amp. Figure 5.7.1 shown below is the Functional block diagram of µA78S40.Important features of the µA78S40 switching regulators are:

- Step up, down & Inverting operation
- Operation from 2.5 to 40V input
- 80dB line & load regulations
- Output adjustable from 1.3 to 40V
- Peak current to 1.5A without external resistors
- Variable frequency, variable duty cycle device

The internal switching frequency is set by the timing capacitor CT, connected between pin12 & ground pin 11. The initial duty cycle is 6:1. The switching frequency & duty cycle can be modified by the current limit circuitry, IPK sense, pin14, 7 the comparator, pin9 & 10. Pin diagram of monolithic swithching regulator is shown in figure 5.7.2.

Comparator:

The comparator modifies the OFF time of the output switch transistor Q1 & Q2. In the step – up & step down modes, the non-inverting input(pin9) of the comparator is connected to the voltage reference of 1.3V (pin8) & the inverting input (pin10) is connected to the output terminal via the voltage divider network.

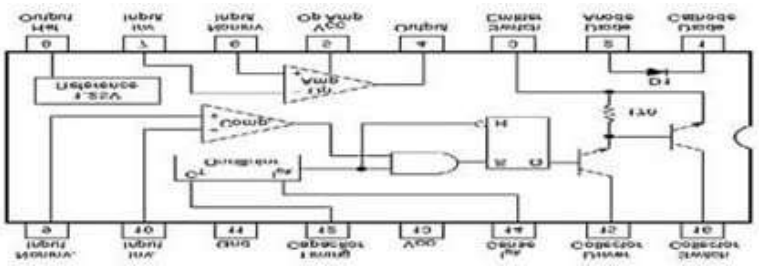


Figure 5.7.1 Functional block diagram of µA78S40

[source: https://www.brainkart.com/subject/Linear-Integrated-Circuits_220/]

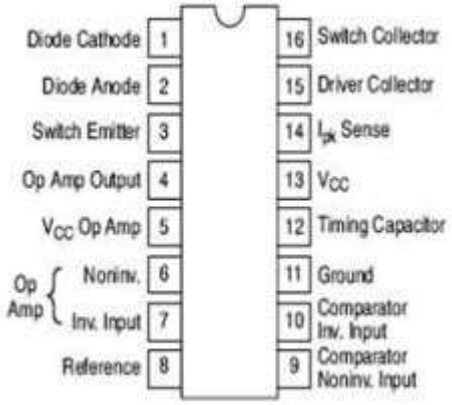


Figure 5.7.2 Pin diagram of monolithic swithching regulator

[source: https://www.brainkart.com/subject/Linear-Integrated-Circuits_220/]

- In the Inverting mode the non – inverting input is connected to both the voltage reference & the output terminal through 2 resistors & the inverting terminal is connected to ground.
- When the output voltage is correct, the comparator output is in high state & has no effect on the circuit operation.
- However, if the output is too high & the voltage at the inverting terminal is higher than that at the non-inverting terminal, then the comparator output goes low.
- In the LOW state the comparator inhibits the turn on of the output switching transistors. This means that, as long as the comparator output is low, the system is in off time.
- As the output current rises or the output voltage falls, the off time of the system decreases.
- Consequently, as the output current nears its maximum IoMAX, the off time approaches its minimum value.

In all 3 modes (Step down, step up, Inverting), the current limit circuit is completed by connecting a sense resistor Rsc, between IPK sense & Vcc.

- The current limit circuit is activated when a 330mV potential appears across Rsc.
- Rsc is selected such that 330mV appears across it when the desired peak current IPK, flows through it.

- When the peak current is reached, the current limit circuit is turned on.

The forward voltage drop, VD, across the internal power diode is used to determine the value of inductor L off time & efficiency of the switching regulator.Another important quantity used in the design of a switching regulator is the saturation voltage Vs:In the step down mode an "output saturation volt" is 1.1V typical, 1.3VMAX.In the step up mode an "Output saturation volt" is 0.45V typical, 0.7 maximum.The desired peak current value is reached; the current limiting circuit turns ON & immediately terminates the ON time & starts OFF time.

- As we increase IL (load current), Vout will decrease, to compensate for this, the ON time of the output is increased automatically.

If the IL decreased then Vout increased, to compensate for this, the OFF time of the output is increased automatically.

(i) Step – Down Switching Regulator:

- Figure 5.7. 3. Shown below is the Step down converter. C_T is the timing capacitor which decides the switching frequency. Rsc is the current sensing resistance. Its value is given by
- The Non-inverting terminal of the internal op-amp (pin 9) is connected to the 1.3V reference (pin 8).
- Resistances R_1 & R_2 from a potential divider, across the output voltage Vo. Their value should be such that the potential at the inverting input of the op-amp should be equal to 1.3V ref when Vo is at its desired level.
- The output capacitance Co is used for reducing the ripple contents in the output voltage. It acts as a filter along with the inductor L.
- The inductor L is a part of filter connected on the output side, to reduce the ripple percentage.
- The 0.1μF capacitor connected between pin8 & ground bypasses any noise voltage coupled to the reference (pin8).

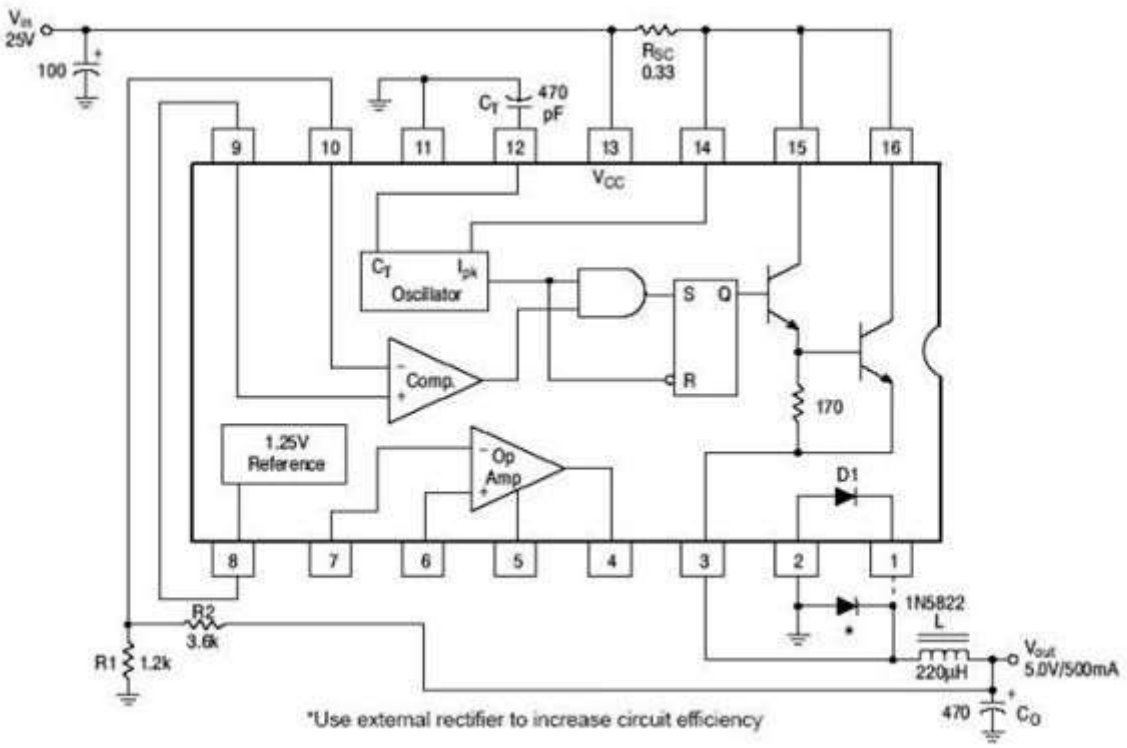


Figure 5.7.3 Step down converter

[source: https://www.brainkart.com/subject/Linear-Integrated-Circuits_220/]

(ii) Step – Up Switching Regulator:

- Step up converter is shown in fig 4.Inductor is connected between the collectors of Q1 & Q2.
- When Q1 is ON, the output is shorted & the collector current of Q1 flows through L.
- The diode D1 is reverse biased & Co supplies the load current.
- The inductor stores the energy. When the Q1 is turned OFF, there is a self induced emf that appears across the inductor with polarities. Operation with Q1 ON and Q1 OFF is shown in Figure 5.7.4.
- The output voltage is given by,

$$V_o = V_{in} + V_L$$

Hence it will be always higher than Vin & step up operation is achieved.

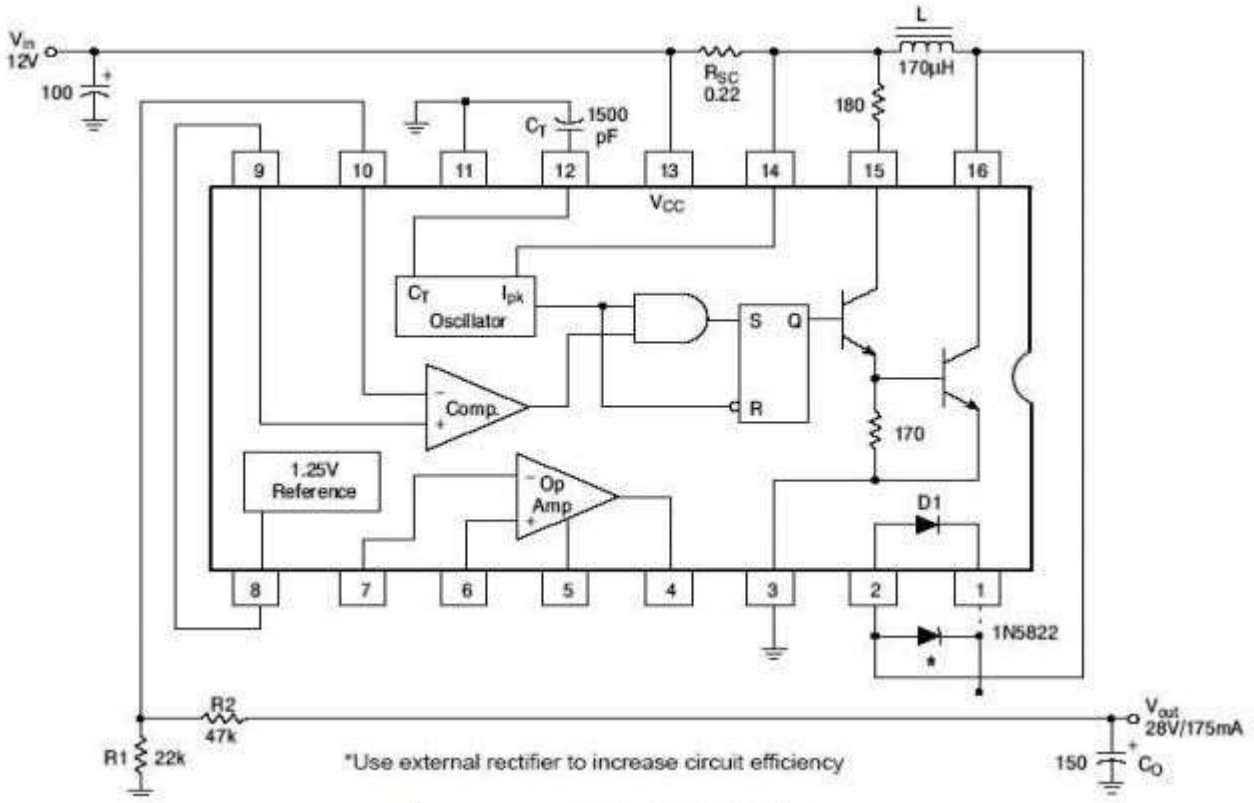


Figure 5.7.4.Step up converter

[source: https://www.brainkart.com/subject/Linear-Integrated-Circuits_220/]

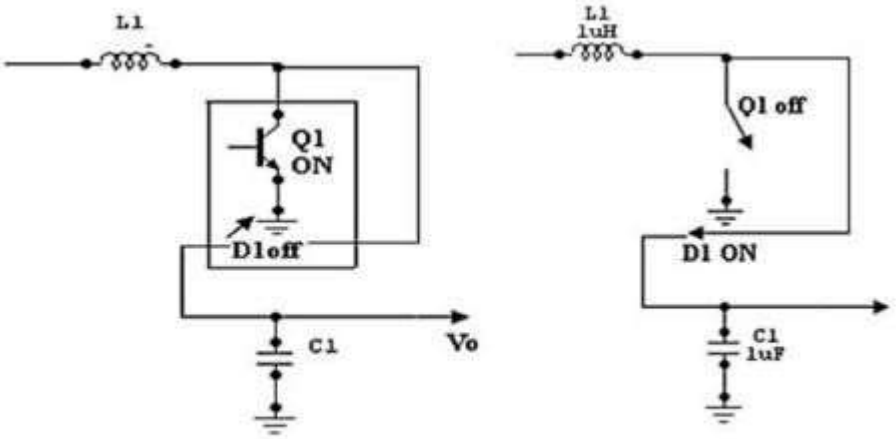


Figure 5.7.5.with Q1 ON and Q1 OFF

[source: https://www.brainkart.com/subject/Linear-Integrated-Circuits_220/]

(iii) Inverting Switching Regulator:

Figure 5.7.6.shown below is the Circuit diagram of inverting switching regulator .Inverting switching regulator converts a positive input voltage into a negative output voltage which is higher in magnitude.

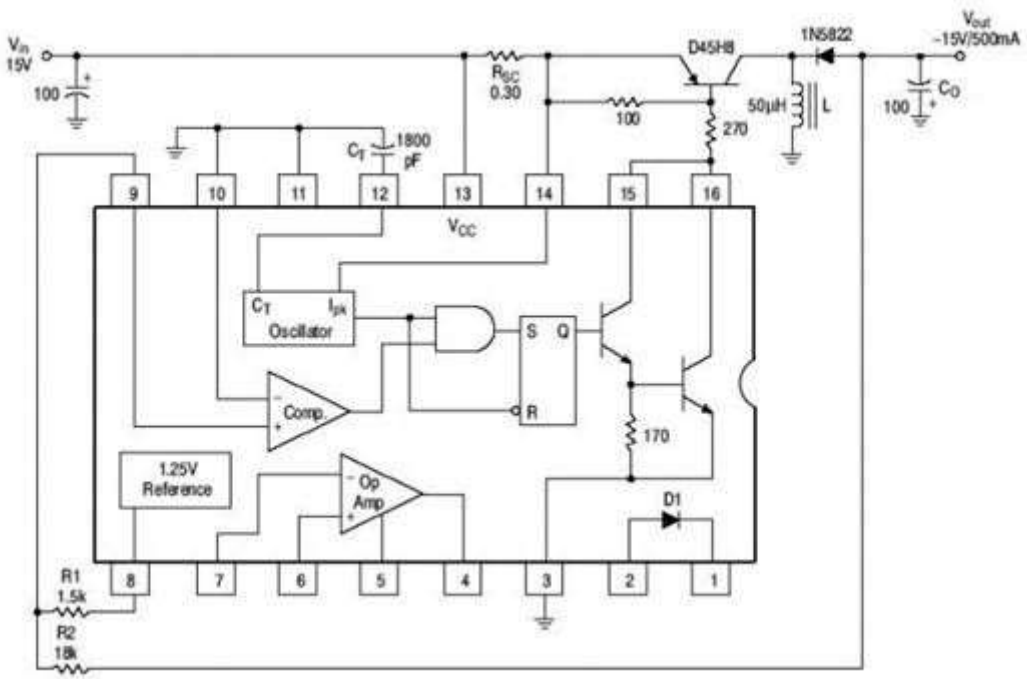


Figure 5.7.6.Circuit diagram of inverting switching regulator

[source: https://www.brainkart.com/subject/Linear-Integrated-Circuits_220/]

5.2 MULTIVIBRATORS

ASTABLE MULTIVIBRATOR

The two states of circuit are only stable for a limited time and the circuit switches between them with the output alternating between positive and negative saturation values. Figure 5.2.1 Shown is the circuit diagram for Astable Multivibrator.

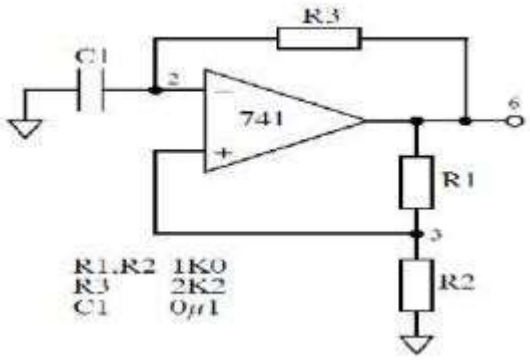


Figure 5.2.1 Astable Multivibrator circuit diagram

[source: https://www.brainkart.com/subject/Linear-Integrated-Circuits_220/]

Analysis of this circuit starts with the assumption that at time t=0 the output has just switched to state 1, and the transition would have occurred.An op-amp Astable multivibrator is also called as free running oscillator. The basic principle of generation of square wave is to force an op-amp to operate in the saturation region ($\pm V_{sat}$).A fraction $\beta = R_2/(R_1+R_2)$ of the output is feedback to the positive input terminal of op-amp. The charge in the capacitor increases & decreases up to a threshold value called $\pm\beta V_{sat}$. The charge in the capacitor triggers the op-amp to stay either at $+V_{sat}$ or $-V_{sat}$.

Asymmetrical square wave can also be generated with the help of Zener diodes. Astable multi vibrator do not require a external trigger pulse for its operation & output toggles from one state to another and does not contain a stable state.Astable multi vibrator is mainly used in timing applications & waveforms generators.

Design

1. The expression of f_o is obtained from the charging period t1 & t2 of capacitor as $T=2RC\ln (R_1+2R_2)/R_1$

2. To simplify the above expression, the value of R_1 & R_2 should be taken as $R_2 = 1.16R$ Such that f_o simplifies to $f_o = 1/2RC$.
3. Assume the value of R_1 and find R_2.
4. Assume the value of C & Determine R from $f_o = 1/2R\ C$
5. Calculate the threshold point from $\beta V_{SAT} = R_1 V_T / R1\text{-}R_2\ l/\beta V_{SAT}$ where β is the feedback ratio.

MONOSTABLE MULTIVIBRATOR USING OP-AMP

circuit diagram:

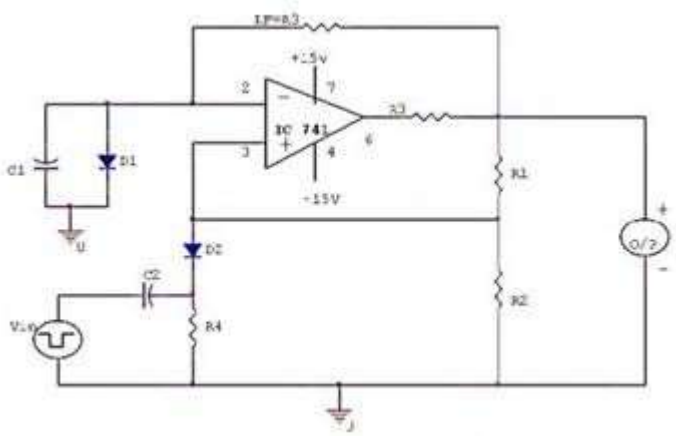


Figure 5.2.2.Monostable multivibrator using op-amp

[source: https://www.brainkart.com/subject/Linear-Integrated-Circuits_220/]

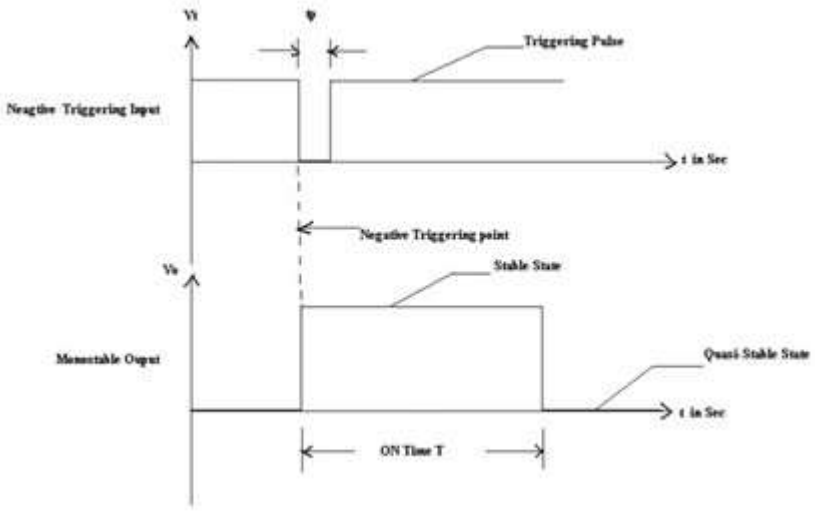


Figure 5.2.3 Input-output waveforms

[source: https://www.brainkart.com/subject/Linear-Integrated-Circuits_220/]

Monostable multivibrator using op-amp is shown in figure 5.2.2.A multivibrator which has only one stable and the other is quasi stable state is called as Monostable multivibrator or one-short multivibrator. This circuit is useful for generating signal output pulse of adjustable time duration in response to a triggering signal. The width of the output pulse depends only on the external components connected to the op-amp. Usually a negative trigger pulse is given to make the output switch to other state. But, it then return to its stable state after a time interval determining by circuit components. The pulse width T can be given as T = 0.69RC. For Monostable operation the triggering pulse width Tp should be less then T, the pulse width of Monostable multivibrator. This circuit is also called as time delay circuit or gating circuit. Input-output waveforms is shown in figure 5.2.3.

Design:

1. Calculating β from expression

$$\beta = \frac{R1}{R1 + R2}$$

2. The value of R and C from the pulse width time expression.

$$T = RC \ln \frac{(1 + V_D / V_{sat})}{1 - \beta}$$

$$T = RC \ln \frac{(1 + V_D / V_{sat})}{0.5}$$

$$T = 0.69RC.$$

3. Triggering pulse width T_p must be much smaller than T. Tp < T.

TRIANGULAR WAVE GENERATOR

A Triangular Wave Generator Using Op amp can be formed by simply connecting an integrator to the square wave generator.

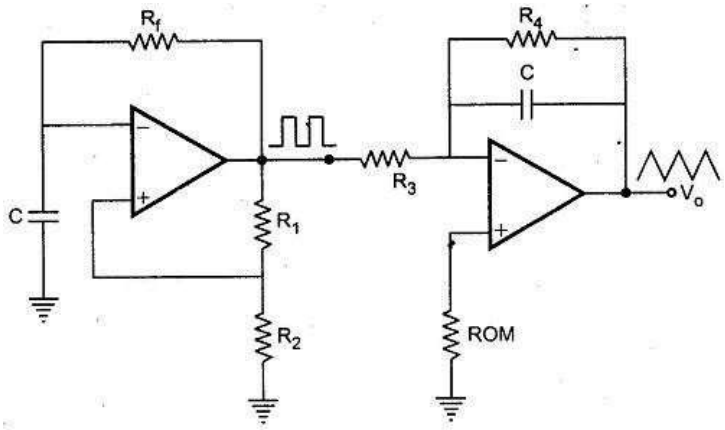


Figure 5.2.4.Circuit Diagram of Triangular wave Generator

[source: https://www.brainkart.com/subject/Linear-Integrated-Circuits_220/]

Triangular wave is generated by alternatively charging and discharging a capacitor with a constant current. This is achieved by connecting integrator circuit at the output of square wave generator as shown in the figure 5.2.4 above.

Assume that V' is high at $+V_{sat.}$ This forces a constant current ($+V_{sat}/R_3$) through C (left to right) to drive Vo negative linearly. When V' is low at —V_{sat}, it forces a constant current (— V_{sat} /R_3) through C (right to left) to drive Vo positive, linearly. The frequency of the triangular wave is same as that of square wave. This is illustrated in Figure 5.2.5 below.

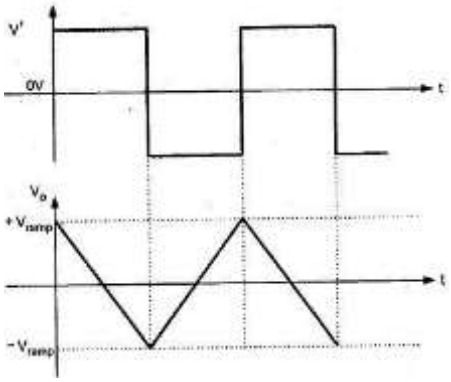


Figure 5.2.5 Input-output waveforms

[source: https://www.brainkart.com/subject/Linear-Integrated-Circuits_220/]

Although the amplitude of the square wave is constant (± V_{sat}), the amplitude of the triangular wave decreases with an increase in its frequency, and vice versa. This is because the reactance of capacitor decreases at high frequencies and increases at low frequencies. In practical circuits, resistance R_4 is connected across C to avoid the saturation problem at low frequencies as in the case of practical integrator as shown in the Figure 5.2.4 above.

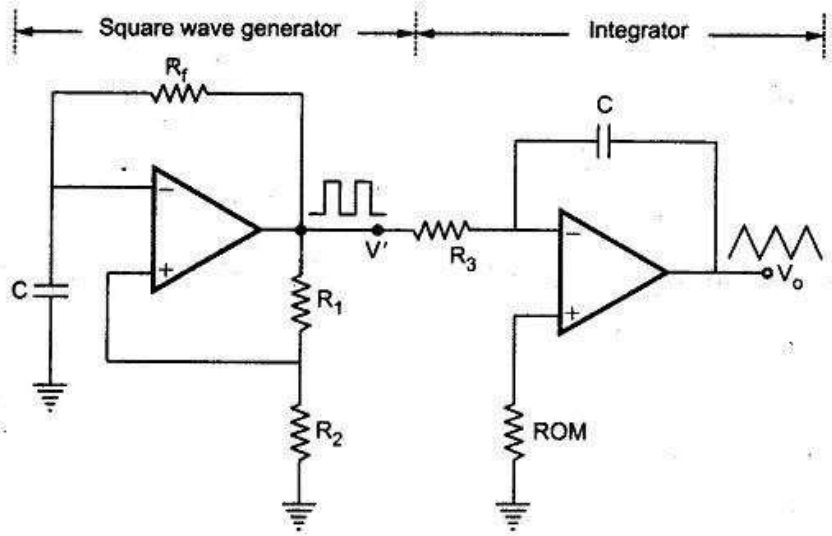


Figure 5.2.6 Triangular wave Generator using lessor components

[source: https://www.brainkart.com/subject/Linear-Integrated-Circuits_220/]

To obtain stable triangular wave at the output, it is necessary to have $5R_3 C_2 > T/2$, where T is the period of the square wave input. Triangular wave Generator using lessor components is shown in figure 5.2.6.

The time period of the output of the square wave generator is $T = 2 \times 2.303 R_f C \times \log((2R_2+R_1)/R_1)$ which is the same for triangular wave generator.

Frequency of the output $f = 1/T$

SAW-TOOTH WAVE GENERATOR

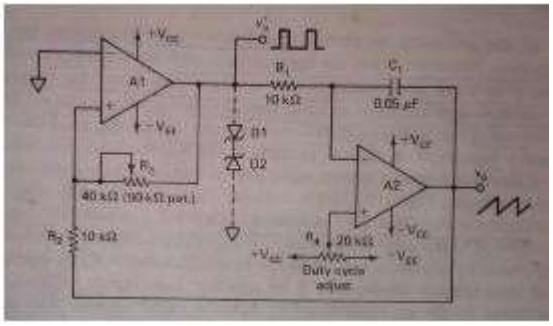


Figure 5.2.7.Schamatic of Sawtooth Generator.

[source:"Linear Integrated Circuits"by D.Roy Choudhry, Shail Bala Jain, Page-246]

Sawtooth wave generator Figure 5.2.7. Schematic of Sawtooth wave generator Sawtooth waveform can be also generated by an asymmetrical astable multivibrator followed by an integrator as shown in figure .The sawtooth wave generators have wide application in time-base generators and pulse width modulation circuits. The difference between the triangular wave and sawtooth waveform is that the rise time of triangular wave is always equal to its fall of time while in saw tooth generator, rise time may be much higher than its fall of time , vice versa. The triangular wave generator can be converted in to a sawtooth wave

generator by injecting a variable dc voltage into the non-inverting terminal of the integrator. In this circuit a potentiometer is used. Now the output of integrator is a triangular wave riding on some dc level that is a function of R4 setting. The duty cycle of square wave will be determined by the polarity and amplitude of dc level. A duty cycle less than 50% will cause output of integrator be a sawtooth. With the wiper at the centre of R_4, the output of integrator is square wave. Use of the potentiometer is when the wiper moves towards $-V_{EE}$,the rise time of the sawtooth become longer than the fall time (see fig. If the wiper moves towards +VCC, the fall time becomes more than the rise time.

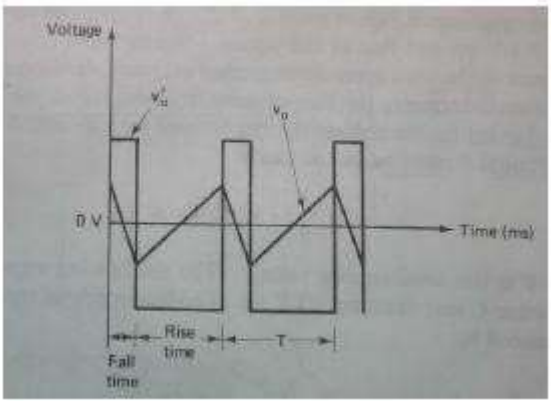


Figure 5.2.8. Output waveform of sawtooth wave generator

[source:"Linear Integrated Circuits"by D.Roy Choudhry, Shail Bala Jain, Page-247]

Figure 5.2.8 shows the Output of sawtooth wave generator when noninverting of integrator is at some negative dc level.

5.14 OPTO COUPLERS/OPTO ISOLATORS AND FIBRE OPTIC IC

- Opto couplers or Opto isolators is a combination of light source & light detector in the same package.
- They are used to couple signal from one point to other optically, by providing a complete electric isolation between them. This kind of isolation is provided between a low power control circuit & high power output circuit, to protect the control circuit.

Characteristics of opto coupler:

(i) Current Transfer Ratio:

It is defined as the ratio of output collector current (Ic) to the input forward current (I_f) CTR = Ic/If * 100%. Its value depends on the devices used as source & detector.

(ii) Isolation voltage between input & output:

It is the maximum voltage which can exist differentially between the input & output without affecting the electrical isolation voltage is specified in K Vrms with a relative humidity of 40 to 60%.

(iii) Response Time:

Response time indicates how fast an opto coupler can change its output state. Response time largely depends on the detector transistor, input current & load resistance.

(iv) Common mode Rejection:

Even though the opto couplers are electrically isolated for dc & low frequency signals, an impulsive input signal (the signal which changes suddenly) can give rise to a displacement current Ic= Cf*dv/dt. This current can flow between input & output due to the capacitance Cf existing between input & output. This allows the noise to appear in the output. Depending on the type of light source & detector used we can get a variety of opto couplers.

They are as follows,

(I) LED – PHOTODIODE OPTO COUPLER

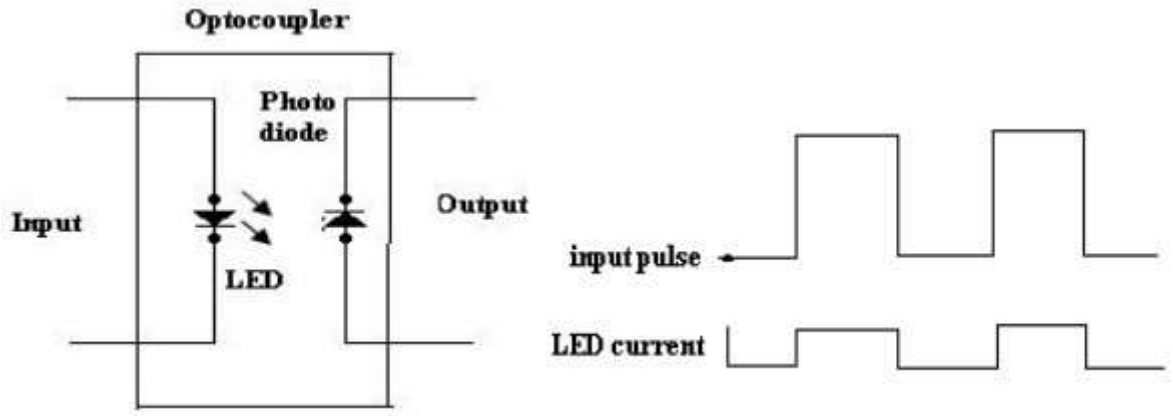


Figure 5.14.1.Schematic of LED-photodiode opto coupler and its waveforms

[source: https://www.brainkart.com/subject/Linear-Integrated-Circuits_220/]

- LED photodiode and its waveforms are shown in figure 5.14.1, here the infrared LED acts as a light source & photodiode is used as a detector.
- The advantage of using the photodiode is its high linearity. When the pulse at the input goes high, the LED turns ON. It emits light. This light is focused on the photodiode.
- In response to this light the photocurrent will start flowing though the photodiode. As soon as the input pulse reduces to zero, the LED turns OFF & the photocurrent through the photodiode reduces to zero. Thus the pulse at the input is coupled to the output side.

(II) LED – PHOTOTRANSISTOR OPTO COUPLER

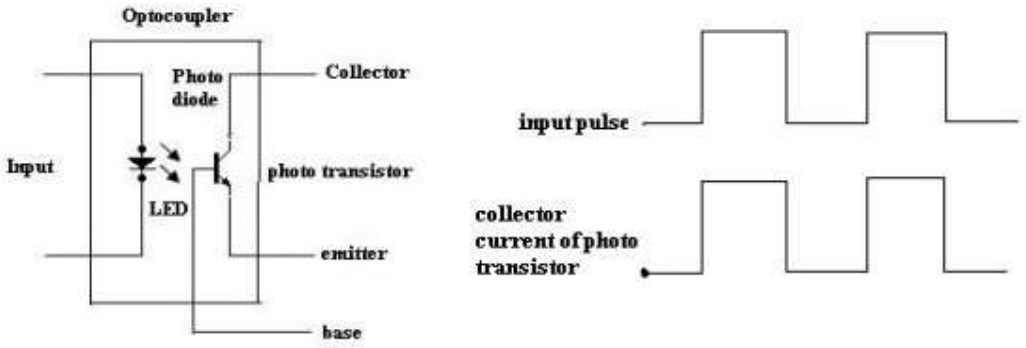


Figure 5.14.2.Schematic of LED- Phototransistor opto coupler and its waveforms

[source: https://www.brainkart.com/subject/Linear-Integrated-Circuits_220/]

- The LED phototransistor opto coupler and its waveforms shown in figure 5.14.2. An infrared LED acts as a light source and the phototransistor acts as a photo detector.
- This is the most popularly used opto coupler, because it does not need any additional amplification.
- When the pulse at the input goes high, the LED turns ON. The light emitted by the LED is focused on the CB junction of the phototransistor.
- In response to this light photocurrent starts flowing which acts as a base current for the phototransistor.
- The collector current of phototransistor starts flowing. As soon as the input pulse reduces to zero, the LED turns OFF & the collector current of phototransistor reduces to zero. Thus the pulse at the input is optically coupled to the output side.
- The input & output waveforms are 180^o out of phase as the output is taken at the collector of the phototransistor

Advantages of Opto coupler:

- Control circuits are well protected due to electrical isolation.
- Wideband signal transmission is possible.
- Due to unidirectional signal transfer, noise from the output side does not get coupled to the input side.
- Interfacing with logic circuits is easily possible.
- It is small size & light weight device.

Disadvantages:

- Slow speed.
- Possibility of signal coupling for high power signals.

Applications:

Opto couplers are used basically to isolate low power circuits from high power circuits.

- At the same time the control signals are coupled from the control circuits to the high power circuits.
- Some of such applications are,

i. AC to DC converters used for DC motor speed control
ii. High power choppers
iii. High power inverters

- One of the most important applications of an opto coupler is to couple the base driving signals to a power transistor connected in a DC-DC chopper.

FIBRE OPTIC IC:

Opto-electronics and opto-electronic devices have undergone tremendous progress in recent years.Optices provides the advantage of large bandwidth,parallelism and reconfigurable characteristics.Electronic devices provide active components in information handling systems.Thus opto-electronic integrated circuits involve the integration of electronic and optical components,and optical interconnects. The fibre forms an optical interconnect medium.such an interconnect medium provides a large bandwidth, high speed data transmission,and immunity against mutual interference and cross-talk. They are unaffected by capacitive loading effects also.It results in size reduction ,reduced power of system and increased fan-out capability.

Figure 5.14.3 a) shows the Block diagram of opto-electronic –integrated circuit .It combines the functions of optical detection, electronic function such as switching and amplification and light transmission.

Figure 5.14.3b) shows the essential elements and Major components of a two-link fibre-optic communication facility.The transmitting end consists of an optical transmitter such as LED or a laser diode source with driver, coupled to the fibre. The LED or laser diode turn ON and OFF according to the bit stream to be sent.The repeaters receive the signal from first link.The signal is amplified,reshaped,retimed and then retransmitted to the next link.The repeater consists of an avananche photo-diode or PIN diode,which senses the attenuated and dispersed train of light pulses.Then the pulses are processed before being sent to the second

link.The receiver at the receiving end converts the incoming light pulses to electrical pulses.The electrical pulses are regenerated and distributed.

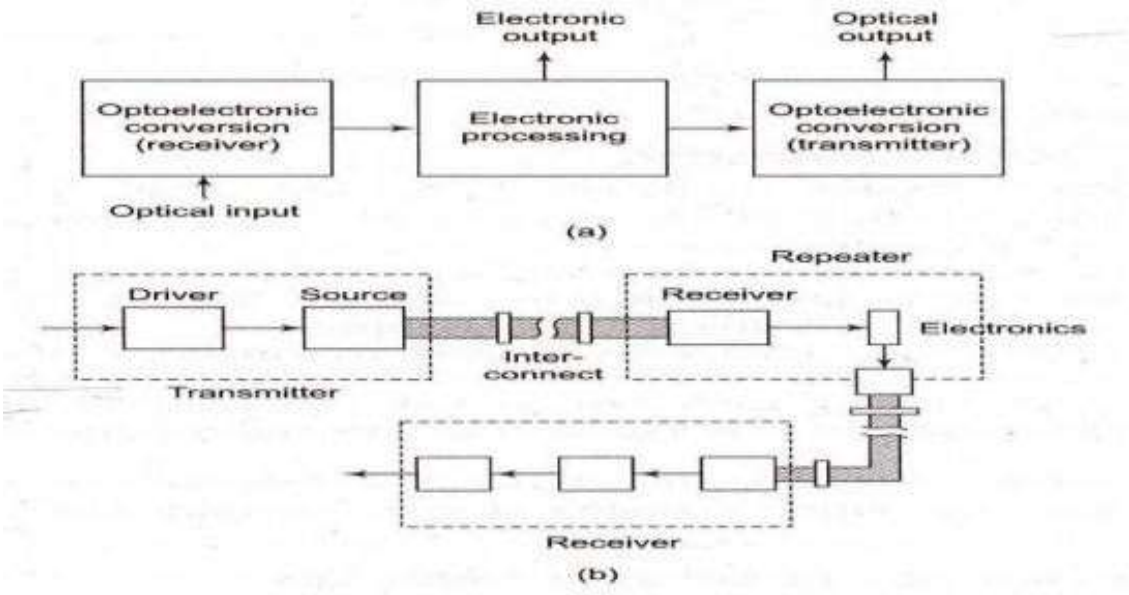


Figure 5.14.3 a)Block diagram of opto-electronic –integrated circuit b) Major components of a fibre-optic communication facility

[source:"Linear Integrated Circuits"by S.Salivahanan& V.S. Kanchana Bhaskaran, Page-542]

In a fibre-optic link,the total loss suffered by the fibre and all the connectors and splices along the length of the fibre optic communication path must not exceed a certain minimum value.The minimum acceptable received optical power P_r is dependent on the type of detector and allowable error rate.Assume a total light flux of power P_t is emitted from the optical source as shown in figure 5.14.4.Only part of the light is sent through the fibre , due to the inefficiency of coupling the diode to fibre end.This results in a part loss of L_{pt}.

Similarly, the connector on the other end of the fibre introduces an insertion loss of L_c.The light passing through the fibre encounters losses due to absorption and leakage,which can be considered as ZL_f where L_f is the rate of loss and Z is the length of the fibre.The splice loss of L_s for each of N_s splices is also introduced.

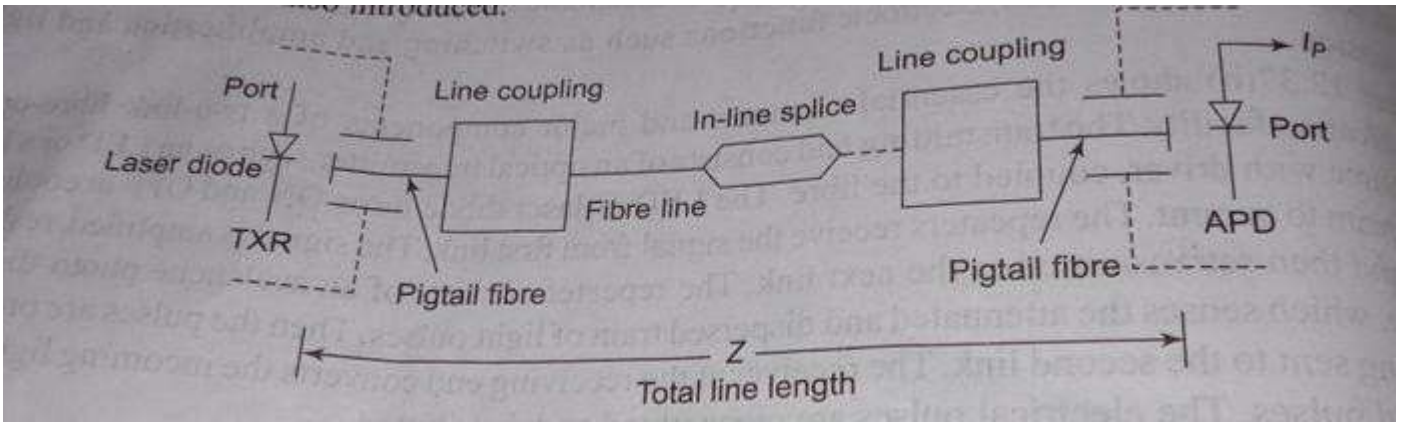


Figure 5.14.4 Elements in the fibre-optic link

[source:"Linear Integrated Circuits"by S.Salivahanan& V.S. Kanchana Bhaskaran, Page-542]

At the receiving end,the digital line connector shown feeds the light from the fibre in to the avalanche photo diode.This introduces a second part loss L_{pr} and a second connector loss L_c.The loss budget for the communication link is then,

$$P_t - P_r = M + L_{pt} + L_{pr} + N_c L_c + N_s L_s + Z L_f$$

Therfore,the maximum length of link Z is determined and limited by the losses.

5.1 BASICS OF OSCILLATORS

CRITERIA FOR OSCILLATION

The canonical form of a feedback system is shown in Figure 5.1.1, and Equation 1 describes the performance of any feedback system (an amplifier with passive feedback Components constitute a feedback system).

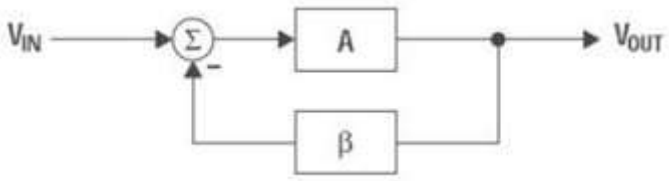


Figure 5.1.1 Canonical form of feedback circuit

[source: https://www.brainkart.com/subject/Linear-Integrated-Circuits_220/]

$$\frac{V_{OUT}}{V_{IN}} = \frac{A}{1+A\beta} \qquad (1)$$

Oscillation results from an unstable state; i.e., the feedback system can't find a stable state because its transfer function can't be satisfied. Equation 1 becomes unstable when $(1+A\beta) = 0$ because A/0 is an undefined state. Thus, the key to designing an oscillator is to insure that $A\beta = -1$ (called the Barkhausen criterion), or using complex math the equivalent expression is $A\beta = 1\ -180°$. The 180° phase shift criterion applies to negative feedback systems, and 0° phase shift applies to positive feedback systems.

The output voltage of a feedback system heads for infinite voltage when $A\beta = -1$. When the output voltage approaches either power rail, the active devices in the amplifiers change gain, causing the value of A to change so the value of $A\beta \neq 1$; thus, the charge to infinite voltage slows down and eventually halts. At this point one of three things can occur.

First, nonlinearity in saturation or cutoff can cause the system to become stable and lock up.Second, the initial charge can cause the system to saturate (or cut off) and stay that way for a long time before it becomes linear and heads for the opposite power rail.
Third, the system stays linear and reverses direction, heading for the opposite power rail. Alternative two produces highly distorted oscillations (usually quasi square waves), and the

resulting oscillators are called relaxation oscillators. Alternative three produces sine wave oscillators.

PHASE SHIFT IN OSCILLATORS

The 180° phase shift in the equation Aβ = 1–180° is introduced by active and passive components. The phase shift contributed by active components is minimized because it varies with temperature, has a wide initial tolerance, and is device dependent. Figure 5.1.2 Shown below is the Phase plot of RC sections.

Amplifiers are selected such that they contribute little or no phase shift at the oscillation frequency. A single pole RL or RC circuit contributes up to 90° phase shift per pole, and because 180° is required for oscillation, at least two poles must be used in oscillator design.

An LC circuit has two poles; thus, it contributes up to 180° phase shift per pole pair, but LC and LR oscillators are not considered here because low frequency inductors are expensive, heavy, bulky, and non-ideal. LC oscillators are designed in high frequency applications beyond the frequency range of voltage feedback op amps, where the inductor size, weight, and cost are less significant.

Multiple RC sections are used in low-frequency oscillator design in lieu of inductors. Phase shift determines the oscillation frequency because the circuit oscillates at the frequency that accumulates –180° phase shift. The rate of change of phase with frequency, dS/dt, determines frequency stability.

When buffered RC sections (an op amp buffer provides high input and low output impedance) are cascaded, the phase shift multiplies by the number of sections, n (see Figure 2).Although two cascaded RC sections provide 180° phase shift, dS/dt at the oscillator frequency is low, thus oscillators made with two cascaded RC sections have poor frequency stability. Three equal cascaded RC filter sections have a higher dS/dt, and the resulting oscillator has improved frequency stability.

Adding a fourth RC section produces an oscillator with an excellent dS/dt, thus this is the most stable oscillator configuration. Four sections are the maximum number used

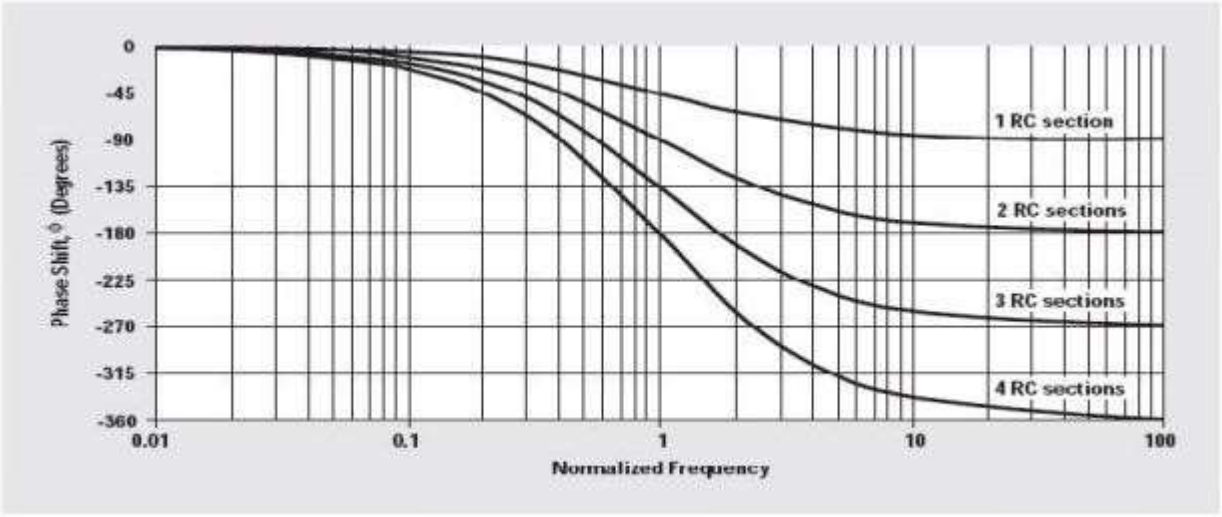


Figure 5.1.2 Phase plot of RC sections

[source: https://www.brainkart.com/subject/Linear-Integrated-Circuits_220/]

because op amps come in quad packages, and the four-section oscillator yields four sine waves that are 45° phase shifted relative to each other, so this oscillator can be used to obtain sine/cosine or quadrature sine waves.

APPLICATIONS

Crystal or ceramic resonators make the most stable oscillators because resonators have an extremely high dS/dt resulting from their non-linear properties. Resonators are used for high- frequency oscillators, but low-frequency oscillators do not use resonators because of size, weight, and cost restrictions.Op-amps are not used with crystal or ceramic resonator oscillators because op amps have low bandwidth. It is more cost-effective to build a high-frequency crystal oscillator and count down the output to obtain a low frequency than it is to use a low-frequency resonator.

GAIN IN OSCILLATORS

The oscillator gain must equal one ($A\beta = 1\text{–}180°$) at the oscillation frequency. The circuit becomes stable when the gain exceeds one and oscillations cease. When the gain exceeds one with a phase shift of –180°, the active device non-linearity reduces the gain to one.

The non-linearity happens when the amplifier swings close to either power rail because cutoff or saturation reduces the active device (transistor) gain. The paradox is that worst-case

design practice requires nominal gains exceeding one for manufacturability, but excess gain causes more distortion of the output sine wave.

When the gain is too low, oscillations cease under worst-case conditions, and when the gain is too high, the output wave form looks more like a square wave than a sine wave.Distortion is a direct result of excess gain overdriving the amplifier; thus, gain must be carefully controlled in low distortion oscillators.Phase-shift oscillators have distortion, but they achieve low-distortion output voltages because cascaded RC sections act as distortion filters. Also, buffered phase-shift oscillators have low distortion because the gain is controlled and distributed among the buffers.

SINE WAVE GENERATORS (OSCILLATORS)

Sine wave oscillator circuits use phase shifting techniques that usually employ

- Two RC tuning networks, and
- Complex amplitude limiting circuitry

RC PHASE SHIFT OSCILLATOR

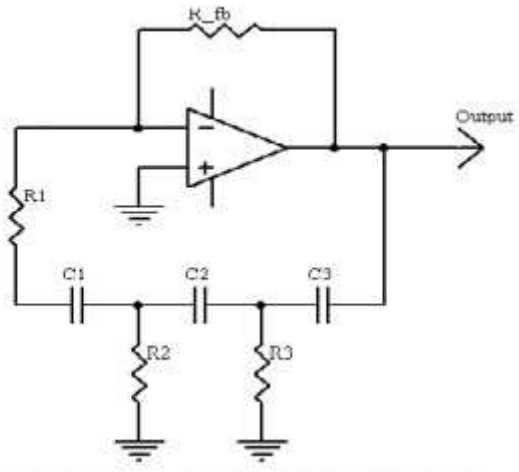


Figure 5.1.3 RC phase shift oscillator

[source: https://www.brainkart.com/subject/Linear-Integrated-Circuits_220/]

RC phase shift oscillator using op-amp in inverting amplifier introduces the phase shift of 180º between input and output. The feedback network consists of 3 RC sections each producing 60º phase shift. Such a RC phase shift oscillator using op-amp is shown in the figure 5.1.3.

The output of amplifier is given to feedback network. The output of feedback network drives the amplifier. The total phase shift around a loop is 180 of amplifier and 180 due to 3 RC sections, thus 360 º. This satisfies the required condition for positive feedback and circuit works as an oscillator.

$$f_{oscillation} = \frac{1}{2\pi\sqrt{R_2R_3(C_1C_2 + C_1C_3 + C_2C_3) + R_1R_3(C_1C_2 + C_1C_3) + R_1R_2C_1C_2}}$$

Oscillation criterion:

$$R_{feedback} = 2(R_1 + R_2 + R_3) + \frac{2R_1R_3}{R_2} + \frac{C_2R_2 + C_2R_3 + C_3R_3}{C_1}$$

$$+\frac{2C_1R_1 + C_1R_2 + C_3R_3}{C_2} + \frac{2C_1R_1 + 2C_2R_1 + C_1R_2 + C_2R_2 + C_2R_3}{C_3}$$

$$+\frac{C_1R_1^2 + C_3R_1R_3}{C_2R_2} + \frac{C_2R_1R_3 + C_1R_1^2}{C_3R_2} + \frac{C_1R_1^2 + C_1R_1R_2 + C_2R_1R_2}{C_3R_3}$$

$$A\beta - A\left(\frac{1}{RCs + 1}\right)^3 \qquad (3)$$

The loop phase shift is –180° when the phase shift of each section is –60°, and this occurs when ω = 2πf = 1.732/RC because the tangent 60° = 1.73. The magnitude of β at this point is $(1/2)^3$, so the gain, A, must be equal to 8 for the system gain to be equal to 1.

WIEN BRIDGE OSCILLATOR

Figure 5.1.4 give the Wien-bridge circuit configuration. The loop is broken at the positive input, and the return signal is calculated in Equation 2 below.

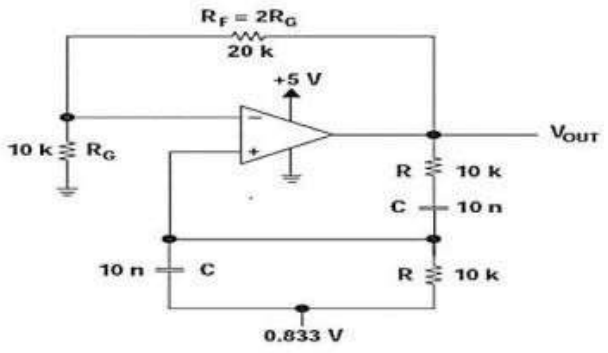


Figure 5.1.4 Wein Bridge oscillator

[source: https://www.brainkart.com/subject/Linear-Integrated-Circuits_220/]

$$\frac{V_{RETURN}}{V_{OUT}} = \frac{\frac{R}{RCs+1}}{\frac{R}{RCs+1} + R + \frac{1}{Cs}} = \frac{1}{3 + RCs + \frac{1}{RCs}} = \frac{1}{3 + j\left(RC\omega - \frac{1}{RC\omega}\right)} \quad (2)$$

where $s = j\omega$ and $j = \sqrt{-1}$.

When $\omega = 2\pi f = 1/RC$, the feedback is in phase (this is positive feedback), and the gain is 1/3, so oscillation requires an amplifier with a gain of 3. When $R_F = 2RG$, the amplifier gain is 3 and oscillation occurs at $f = 1/2\pi RC$. The circuit oscillated at 1.65 kHz rather than 1.59 kHz with the component values shown in Figure 5.1.4 but the distortion is noticeable.

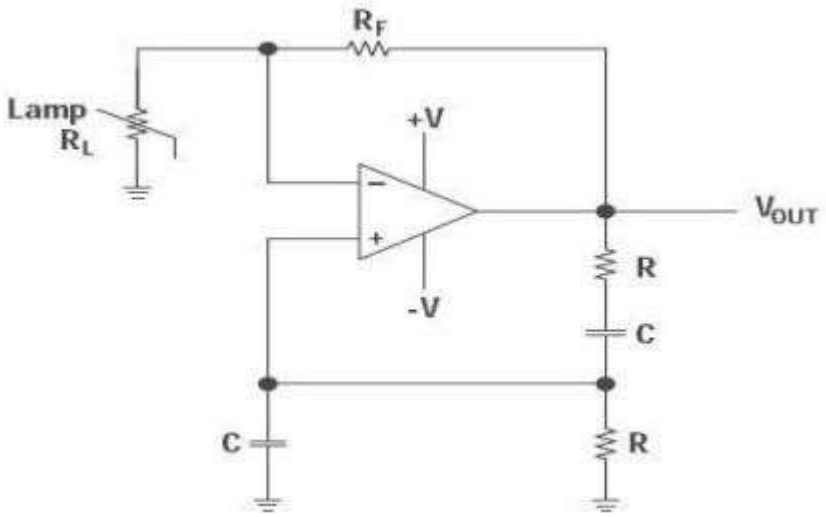


Figure 5.1.5 Wien-bridge circuit with non-linear feedback.

[source: https://www.brainkart.com/subject/Linear-Integrated-Circuits_220/]

Figure 5.1.5 shows a Wien-bridge circuit with non-linear feedback. The lamp resistance, R_L, is nominally selected as half the feedback resistance, R_F, at the lamp current established by R_F and R_L. The non-linear relationship between the lamp current and resistance keeps output voltage changes small.

If a voltage source is applied directly to the input of an **ideal** amplifier with feedback, the input current will be:

$$i_{in} = \frac{v_{in} - v_{out}}{Z_f}$$

Where *vin* is the input voltage, v_{out} is the output voltage, and Z_f is the feedback impedance. If the voltage gain of the amplifier is defined as:

$$A_v = \frac{v_{out}}{v_{in}}$$

And the input admittance is defined as:

$$Y_i = \frac{i_{in}}{v_{in}}$$

Input admittance can be rewritten as:

$$Y_i \quad \frac{1 - A_v}{Z_f}$$

For the Wien Bridge, *Zf* is given by:

$$Z_f = R + \frac{1}{j\omega C}$$

$$Y_i = \frac{(1 - A_v)(\omega^2 C^2 R + j\omega C)}{1 + (\omega C R)^2}$$

If *Av* is greater than 1, the input admittance is a negative resistance in parallel with an inductance.

The inductance is:

$$L_{in} = \frac{\omega^2 C^2 R^2 + 1}{\omega^2 C (A_v - 1)}$$

If a capacitor with the same value of *C* is placed in parallel with the input, the circuit has a natural resonance at:

$$\omega = \frac{1}{\sqrt{L_{in} C}}$$

Substituting and solving for inductance yields:

$$L_{in} - \frac{R^2 C}{A_v - 2}$$

If *Av* is chosen to be 3: $Lin = R^2C$

Substituting this value yields:

$$\omega = \frac{1}{RC} \quad \text{Or} \quad f = \frac{1}{2\pi RC}$$

Similarly, the input resistance at the frequency above is:

$$R_{in} = \frac{-2R}{A_v - 1}$$

For $A_v = 3$: $R_{in} = -R$

If a resistor is placed in parallel with the amplifier input, it will cancel some of the negative resistance. If the net resistance is negative, amplitude will grow until clipping occurs.Similarly, if the net resistance is positive, oscillation amplitude will decay. If a resistance is added in parallel with exactly the value of R, the net resistance will be infinite and the circuit can sustain stable oscillation at any amplitude allowed by the amplifier.

Increasing the gain makes the net resistance more negative, which increases amplitude. If gain is reduced to exactly 3 when suitable amplitude is reached, stable, low distortion oscillations will result.Amplitude stabilization circuits typically increase gain until suitable output amplitude is reached. As long as R, C, and the amplifier are linear, distortion will be minimal.

5.9 THE SWITCHED CAPACITOR FILTER

Basic Representation:

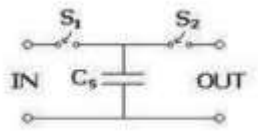


Figure 5.9.1.Switched –Capacitor resistor

[source: https://www.brainkart.com/subject/Linear-Integrated-Circuits_220/]

Figure 5.9.1 shown above is the Switched –Capacitor resistor. The simplest switched capacitor (SC) circuit is the switched capacitor resistor, made of one capacitor C and two switches S_1 and S_2 which connect the capacitor with a given frequency alternately to the input and output of the SC. Each switching cycle transfers a charge *q* from the input to the output at the switching frequency *f*. Recall that the charge *q* on a capacitor *C* with a voltage *V* between the plates is given by:

$$q=CV$$

where *V* is the voltage across the capacitor. Therefore, when S1 is closed while S2 is open, the charge transferred from the source to CS is:

$$q_{IN}=C_S V_{IN}$$

And when S_2 is closed while S_1 is open, the charge transferred from CS to the load is:

$$q_{OUT} = C_S V_{OUT}$$

Thus, the charge transferred in each cycle is:

$$Q=q_{OUT}-q_{IN}=C_s(V_{OUT}-V_{IN})$$

Since a charge *q* is transferred at a rate *f*, the rate of transfer of charge per unit time is:

$$I=qf$$

Note that we use *I*, the symbol for electric current, for this quantity. This is to demonstrate that a continuous transfer of charge from one node to another is equivalent to a current. Substituting for *q* in the above, we have:

$$I=C_s(V_{OUT}-V_{IN})f$$

Let us define V, the voltage across the SC from input to output, thus:

$$V=V_{OUT}-V_{IN}$$

We now have a relationship between I and V, which we can rearrange to give an equivalent resistance *R*:

$$R=V/I=1/C_sf$$

Thus, the SC behaves like a resistor whose value depends on *CS* and *f*.

The SC resistor is used as a replacement for simple resistors in integrated circuits because it is easier to fabricate reliably with a wide range of values. It also has the benefit that its value can be adjusted by changing the switching frequency. See also: operational amplifier applications.

This same circuit can be used in discrete time systems (such as analog to digital converters) as a track and hold circuit. During the appropriate clock phase, the capacitor samples the analog voltage through switch one and in the second phase presents this held sampled value to an electronic circuit for processing.

SWITCHED CAPACITOR CIRCUITS

The switched capacitor filter allows for very sophisticated, accurate, and tunable analog circuits to be manufactured without using resistors.

Advantages: resistors are hard to build on integrated circuits (they take up a lot ofroom), and the circuits can be made to depend on ratios of capacitor values (which can be set accurately), and not absolute values (which vary between manufacturing runs).

THE SWITCHED CAPACITOR RESISTOR

Consider the circuit shown in figure 5.9.2 with a capacitor connected to two switches and two different voltages.

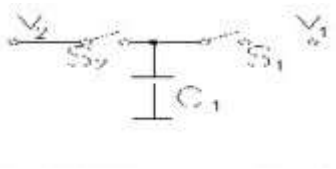


Figure 5.9.2,Sample circuit

[source: https://www.brainkart.com/subject/Linear-Integrated-Circuits_220/]

If S2 closes with S1 open, then S1 closes with switch S2 open, a charge (q is transferred from V_2 to V_1 with

$$\Delta q=C1(v_2-v_1)$$

If this switching process is repeated N times in a time (t, the amount of charge transferred per unit time is given by

$$\Delta q/\Delta t=C_1(v_2-v_1)\ N/\Delta t$$

the number of cycles per unit time is the switching frequency (or clock frequency, f_{CLK})

$$i= C_1(v_2-v_1)\ f_{CLK}$$

Rearranging we get

$$(v_2-v_1) / I = [\ 1/ C_1\ f_{CLK}\ ] -R$$

Which states that the switched capacitor is equivalent to a resistor? The value of this resistor decreases with increasing switching frequency or increasing capacitance, as either will increase the amount of charge transferred from V_2 to V_1 in a given time.

THE SWITCHED CAPACITOR INTEGRATOR

Now consider the integrator circuit. You have shown (in a previous lab) that the input-output relationship for this circuit is given by (neglecting initial conditions):

$$v_o(t) = -\frac{1}{RC_2}\int v_i(t)dt = -\omega'\int v_i(t)dt$$

We can also write this with the "s" notation (assuming a sinusoidal input, Ae^{st}, $s=j\omega$)

$$V_o(s) = -\frac{\omega'}{s}$$

If you replaced the input resistor with a switched capacitor resistor, you would get

$$\omega' = \frac{1}{RC_2} = f_{CLK}\frac{C_1}{C_2}$$

Thus, you can change the equivalent ω' of the circuit by changing the clock frequency. The value of ω' can be set very precisely because it depends only on the ratio of C1 and C2, and not their absolute value.

SWITCHED CAPACITOR FILTER ICS

Some of the Switched capacitor filter ICs is MF 5, MF10 and MF100

MF10:

The MF10 contains two of the second-order universal filter sections found in the MF5. Therefore with MF10, two second order filters or one fourth-order filter can be built. As the MF5 and MF10 have similar filter sections, the design procedure for them is same. Figure 5.9.3.shown below is the Switched Capacitor Filter MF10

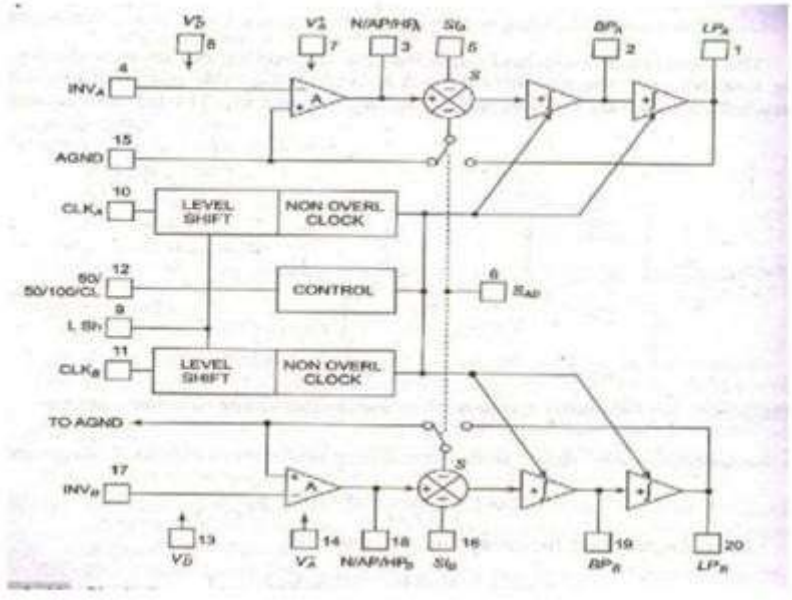


Figure 5.9.3 Switched Capacitor Filter MF10

[source:"Linear Integrated Circuits"by D.Roy Choudhry, Shail Bala Jain, Page-332]

5.4 THE 555 TIMER IC

The 555 is a monolithic timing circuit that can produce accurate & highly stable time delays or oscillation. The timer basically operates in one of two modes: either

(i) Monostable multivibrator or (one - shot)

(ii) Astable multivibrator or (free running)

The important features of the 555 timer are these:

1. It operates on +5v to +18 v supply voltages
2. It has an adjustable duty cycle
3. Timing is from microseconds to hours
4. It has a current o/p

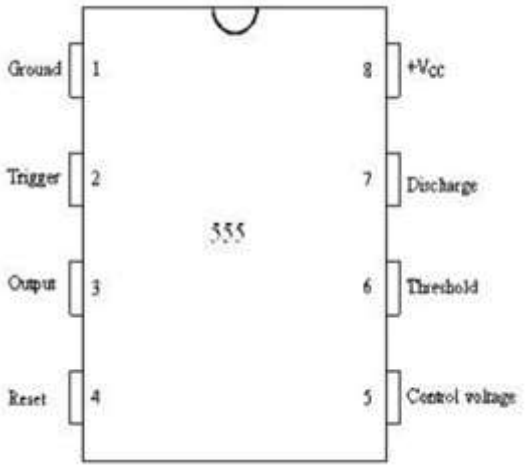


Figure 5.4.1 Pin configuration of 555 timer

[source: https://www.brainkart.com/subject/Linear-Integrated-Circuits_220/]

Pin description: Pin configuration of 555 timer is shown in figure 5.4.1.

Pin 1: Ground:

All voltages are measured with respect to this terminal.

Pin 2: Trigger:

The o/p of the timer depends on the amplitude of the external trigger pulse applied to this pin.

Pin 3: Output:

There are 2 ways a load can be connected to the o/p terminal either between pin3 & ground or between pin 3 & supply voltage

(Between Pin 3 & Ground ON load) (Between Pin 3 & + Vcc OFF load)

1. When the input is low:

   The load current flows through the load connected between Pin 3 & +Vcc in to the output terminal & is called the sink current.

2. When the output is high:

   The current through the load connected between Pin 3 & +Vcc (i.e. ON load) is zero. However the output terminal supplies current to the normally OFF load. This current is called the source current.

Pin 4: Reset:

The 555 timer can be reset (disabled) by applying a negative pulse to this pin. When the reset function is not in use, the reset terminal should be connected to +Vcc to avoid any false triggering.

Pin 5: Control voltage:

An external voltage applied to this terminal changes the threshold as well as trigger voltage. In other words by connecting a potentiometer between this pin & GND, the pulse width of the output waveform can be varied. When not used, the control pin should be bypassed to ground with 0.01 capacitor to prevent any noise problems.

Pin 6: Threshold:

This is the non inverting input terminal of upper comparator which monitors the voltage across the external capacitor.

Pin 7: Discharge:

This pin is connected internally to the collector of transistor Q1.

When the output is high Q1 is OFF.

When the output is low Q is (saturated) ON.

Pin 8: +Vcc:

The supply voltage of +5V to +18V is applied to this pin with respect to ground.

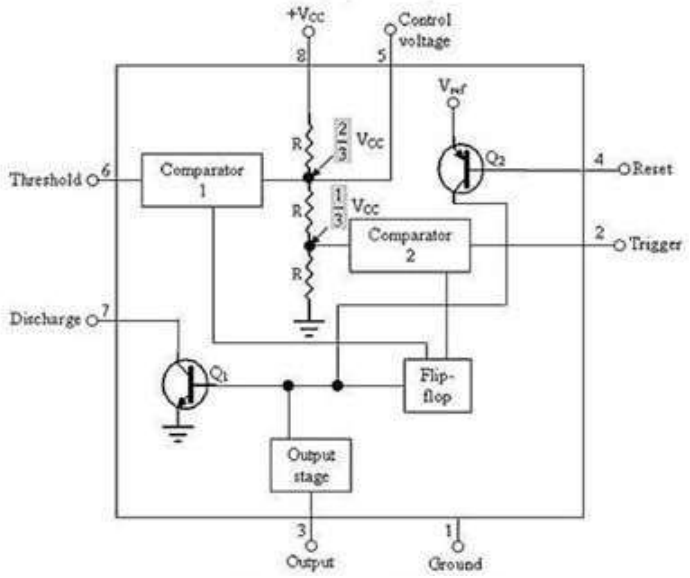


Figure 5.4.2.Block diagram of IC555 Timer

[source: https://www.brainkart.com/subject/Linear-Integrated-Circuits_220/]

From the above figure 5.4.2 three 5k internal resistors act as voltage divider providing bias voltage of 2/3 Vcc to the upper comparator & 1/3 Vcc to the lower comparator. It is possible to vary time electronically by applying a modulation voltage to the control voltage input terminal (5).

(i) In the Stable state:

The output of the control FF is high. This means that the output is low because of power amplifier which is basically an inverter. Q = 1; Output = 0

(ii) At the Negative going trigger pulse:

The trigger passes through (Vcc/3) the output of the lower comparator goes high & sets the FF. Q = 1; Q = 0

(iii) At the Positive going trigger pulse:

It passes through 2/3Vcc, the output of the upper comparator goes high and resets the FF. Q = 0; Q = 1

The reset input (pin 4) provides a mechanism to reset the FF in a manner which overrides the effect of any instruction coming to FF from lower comparator.

MONOSTABLE OPERATION

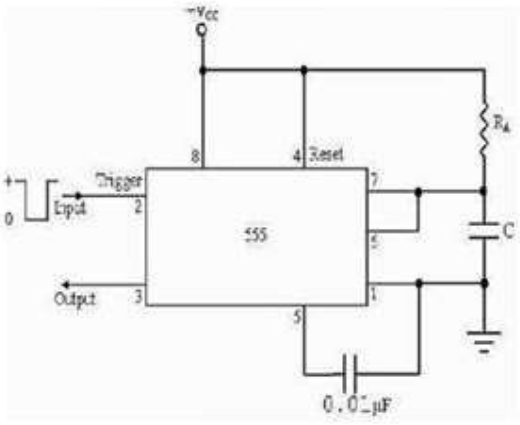


Figure 5.4.3.Monostable Multivibrator using IC 555

[source: https://www.brainkart.com/subject/Linear-Integrated-Circuits_220/]

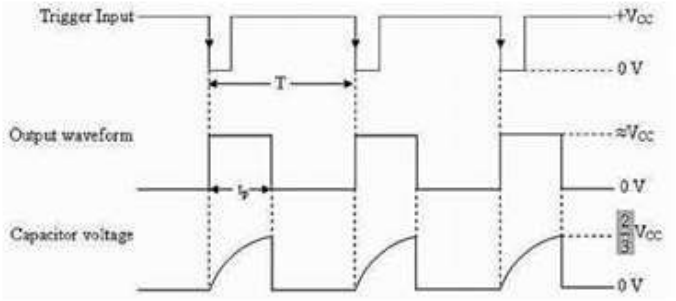


Figure 5.4.4.Waveforms of Monostable multivibrator

[source: https://www.brainkart.com/subject/Linear-Integrated-Circuits_220/]

Monostable Multivibrator using IC 555 is shown in figure 5.4.3.Initially when the output is low, i.e. the circuit is in a stable state, transistor Q1 is ON & capacitor C is shorted to ground. The output remains low. During negative going trigger pulse, transistor Q1 is OFF, which releases the short circuit across the external capacitor C & drives the output high. Now the capacitor C starts charging toward Vcc through RA. When the voltage across the capacitor

equals 2/3 Vcc, upper comparator switches from low to high. i.e. Q = 0, the transistor Q1 = OFF ; the output is high.

Since C is unclamped, voltage across it rises exponentially through R towards Vcc with a time constant RC (figure 5.4.4) as shown in above. After the time period, the upper comparator resets the FF, i.e. Q = 1, Q1 = ON; the output is low. The voltage across the capacitor is given by

$$Vc = Vcc\ (1-e^{-t/RC}) \ldots\ldots (1)$$

Therefore At t = T, Vc = 2/3 Vcc

$$2/3\ Vcc = Vcc(1-e^{-T/RC})$$

or

$$T = RC \ln (1/3)$$

Or

$$T = 1.1RC \text{ seconds} \ldots\ldots\ldots\ldots (2)$$

If the reset is applied Q2 = OFF, Q1 = ON, timing capacitor C immediately discharged. The output now will be as in figure (d & e). If the reset is released output will still remain low until a negative going trigger pulse is again applied at pin 2.

APPLICATIONS OF MONOSTABLE MODE OF OPERATION

(a) FREQUENCY DIVIDER

The 555 timer as a monostable mode. It can be used as a frequency divider by adjusting the length of the timing cycle tp with respect to the time period T of the trigger input. To use the monostable multivibrator as a divide by 2 circuit, the timing interval tp must be a larger than the time period of the trigger input. [Divide by 2, tp> T of the trigger]

By the same concept, to use the monostable multivibrator as a divide by 3 circuit, tp must be slightly larger than twice the period of the input trigger signal & so on, [divide by 3 tp > 2T of trigger]

(b) PULSE WIDTH MODULATION

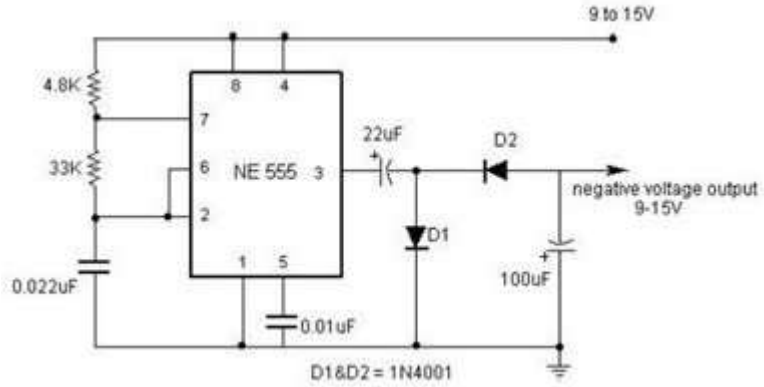


Figure 5.4.5. Pulse width modulation

[source: https://www.brainkart.com/subject/Linear-Integrated-Circuits_220/]

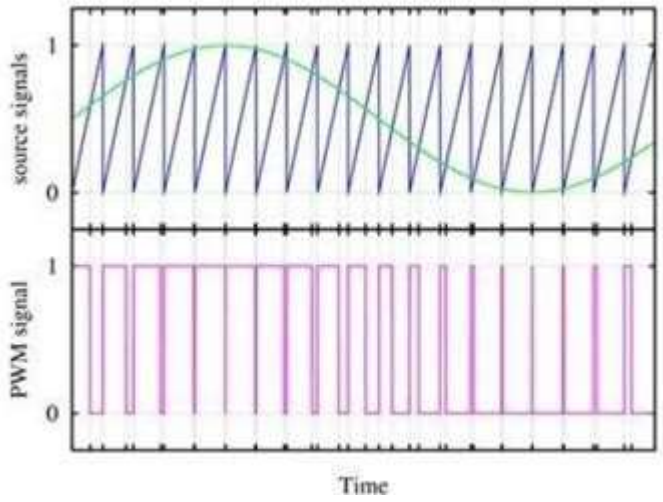


Figure 5.4.6 Output waveforms

[source: https://www.brainkart.com/subject/Linear-Integrated-Circuits_220/]

Pulse width modulation is shown in figure 5.4.5.Pulse width of a carrier wave changes in accordance with the value of a incoming (modulating signal) is known as PWM. It is basically monostable multivibrator.A modulating signal is fed in to the control voltage (pin 5). Internally, the control voltage is adjusted to 2/3 Vcc externally applied modulating signal changes the control voltage level of upper comparator. As a result, the required to change the capacitor up to threshold voltage level changes, giving PWM output. Output waveforms are shown in figure 5.4.6.

(c) PULSE STRETCHER

This application makes use of the fact that the output pulse width (timing interval) of the monostable multivibrator is of longer duration than the negative pulse width of the input trigger. As such, the output pulse width of the monostable multivibrator can be viewed as a stretched version of the narrow input pulse, hence the name “Pulse stretcher”. Pulse Stretcher is shown in figure 5.4.7.

Often, narrow –pulse width signals are not suitable for driving an LED display, mainly because of their very narrow pulse widths. In other words, the LED may be flashing but not be visible to the eye because its on time is infinitesimally small compared to its off time. The 55 pulse stretcher can be used to remedy this problem. The LED will be ON during the timing interval tp = 1.1RAC which can be varied by changing the value of RA & C.

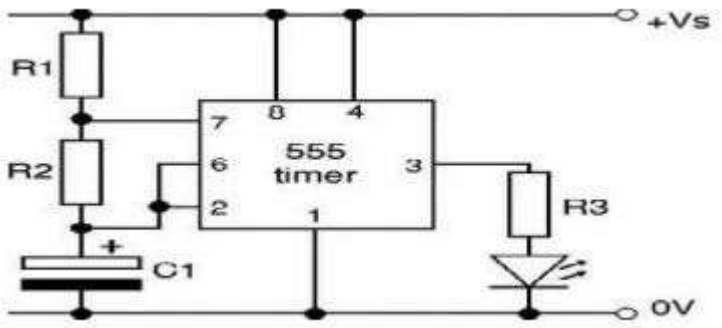


Figure 5.4.7 Pulse Stretcher

[source: https://www.brainkart.com/subject/Linear-Integrated-Circuits_220/]

THE 555 TIMER AS AN ASTABLE MULTIVIBRATOR

An Astable multivibrator, often called a free running multivibrator, is a rectangular wave generating circuit. Unlike the monostable multivibrator, this circuit does not require an external trigger to change the state of the output, hence the name free running. However, the time during which the output is either high or low is determined by 2 resistors and capacitors, which are externally connected to the 55 timer.

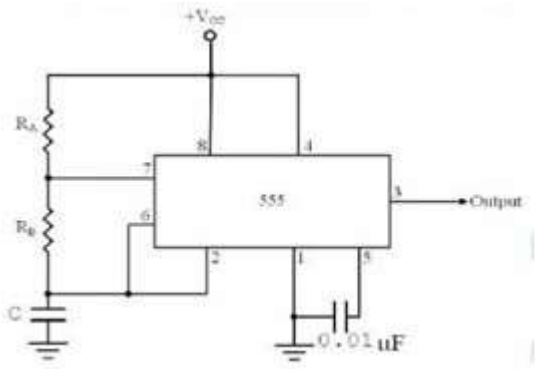


Figure 5.4.8 Astable multivibrator using IC555 Timer

[source: https://www.brainkart.com/subject/Linear-Integrated-Circuits_220/]

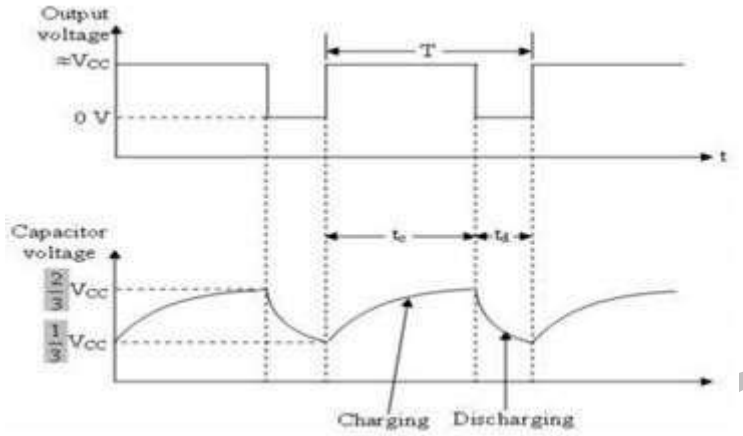


Figure 5.4.9 waveforms of Astable multibrator

[source: https://www.brainkart.com/subject/Linear-Integrated-Circuits_220/]

The above Figure 5.4.8 and figure 5.4.9 show the 555 timer connected as an astable multivibrator and its model graph

Initially, when the output is high :

Capacitor C starts charging toward Vcc through RA & RB. However, as soon as voltage across the capacitor equals 2/3 Vcc. Upper comparator triggers the FF & output switches low.

When the output becomes Low:

Capacitor C starts discharging through RB and transistor Q1, when the voltage across C equals 1/3 Vcc, lower comparator output triggers the FF & the output goes high. Then cycle repeats. The capacitor is periodically charged & discharged between 2/3 Vcc & 1/3 Vcc

respectively. The time during which the capacitor charges from 1/3 Vcc to 2/3 Vcc equal to the time the output is high & is given by

$$tc = (RA+RB)C \ln 2 \quad \text{.....(1) Where } [\ln 2 = 0.69]$$

$$= 0.69 (RA+RB) C$$

Where RA & RB are in ohms. And C is in farads.

Similarly, the time during which the capacitors discharges from 2/3 Vcc to 1/3 Vcc is equal to the time, the output is low and is given by,

$$tc = RB\ C \ln 2$$

$$td = 0.69\ RB\ C \quad \text{.....(2)}$$

where RB is in ohms and C is in farads.

Thus the total period of the output waveform is

$$T = tc + td \qquad = 0.69 (RA+2RB) C \quad \text{.....(3)}$$

This, in turn, gives the frequency of oscillation as, $f_0 = 1/T = 1.45/(RA+2RB)C$ ..... (4)

Equation 4 indicates that the frequency f_0 is independent of the supply voltage Vcc. Often the term duty cycle is used in conjunction with the astable multivibrator. The duty cycle is the ratio of the time tc during which the output is high to the total time period T. It is generally expressed as a percentage.

$$\% \text{ duty cycle} = (tc / T)* 100$$

$$\% DC = [(RA+RB)/ /(RA+2RB)] * 100$$

ASTABLE MULTIVIBRATOR APPLICATIONS:

(a) SQUARE WAVE OSCILLATOR

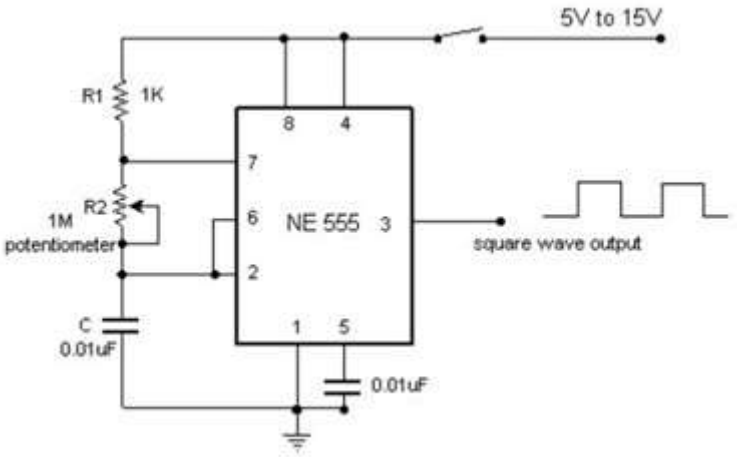


Figure 5.4.10.Square wave oscillator

[source: https://www.brainkart.com/subject/Linear-Integrated-Circuits_220/]

Figure 5.4.10 shows the Square wave oscillator. Without reducing RA = 0 ohm, the astable multivibrator can be used to produce square wave output. Simply by connecting diode D across Resistor RB. The capacitor C charges through RA & diode D to approximately 2/3Vcc & discharges through RB & Q1 until the capacitor voltage equals approximately 1/3Vcc, then the cycle repeats.To obtain a square wave output, RA must be a combination of a fixed resistor & potentiometer so that the potentiometer can be adjusted for the exact square wave.

(b) FREE – RUNNING RAMP GENERATOR

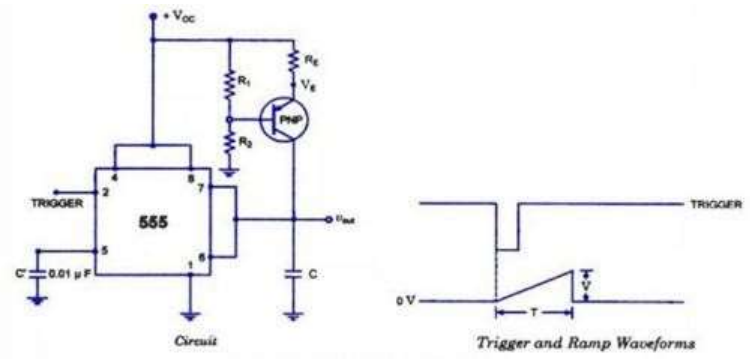


Figure 5.4.11 Ramp generator using IC 555 Timer and its waveforms

[source: https://www.brainkart.com/subject/Linear-Integrated-Circuits_220/]

- Ramp generator using IC 555 Timer and its waveforms is shown in figure 5.4.11. The astable multivibrator can be used as a free – running ramp generator when resistor
- RA & RB is replaced by a current mirror.
- The current mirror starts charging capacitor C toward Vcc at a constant rate.
- When voltage across **C equals to 2/3 Vcc**, upper comparator turns transistor Q1 ON and C rapidly discharges through transistor Q1.
- When voltage across **C equals to 1/3 Vcc**, lower comparator switches transistor OFF & then capacitor C starts charging up again.
- Thus the charge – discharge cycle keeps repeating.
- The discharging time of the capacitor is relatively negligible compared to its charging time.

The time period of the ramp waveform is equal to the charging time & is approximately is given by,

$$T = VccC/3I_C$$

$$I_C = (Vcc - V_{BE})/R = \text{constant current}$$

Therefore the free – running frequency of ramp generator is

$$f_0 = 3I_C/ Vcc\ C$$