

Analog and Digital Data Conversion

The natural state of audio and video signals is analog. When digital technology was not yet around, they are recorded or played back in analog devices like vinyl discs and cassette tapes. The storage capacity of these devices is limited and doing multiple runs of re-recording and editing produced poor signal quality. Developments in digital technology like the CD, DVD, Blu-ray, flash devices and other memory devices addressed these problems.

For these devices to be used, the analog signals are first converted to digital signals using analog to digital conversion (ADC). For the recorded audio and video signals to be heard and viewed again, the reverse process of digital to analog conversion (DAC) is used. ADC and DAC are also used in interfacing digital circuits to analog systems. Typical applications are control and monitoring of temperature, water level, pressure and other real-world data.

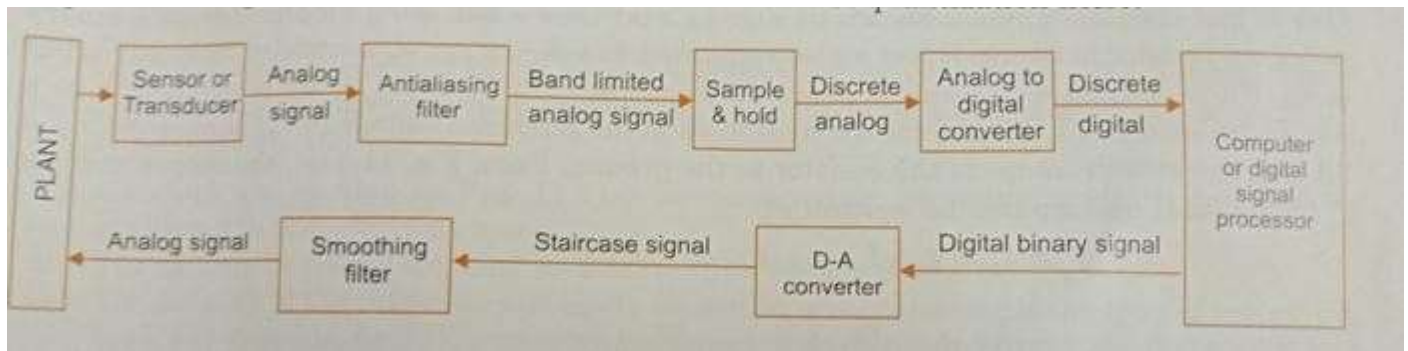


Fig 1 Circuit showing application of A/D and D/A converter(source: D.Roy Choudhry, Shail Jain, —Linear Integrated Circuits, New Age International Pvt. Ltd., 2018, Fifth Edition.)

Fig 1. highlights a typical application within which A/D and D/A conversion is used. The analog signal obtained from the transducer is band limited by antialiasing filter. The signal is then sampled at a frequency rate more than twice the maximum frequency of the band limited signal. The sampled signal has to be held constant while conversion is taking place in A/D converter. This requires that ADC should be preceded by a sample and hold circuit. The ADC output is a sequence in binary digit. The micro-computer or digital signal processor performs the numerical calculations of the desired control algorithm. The D/A converter is to convert digital signal into analog and hence the function of DAC is exactly opposite to that of ADC. The D/A converter is usually operated at the same frequency as the ADC. The output of a D/A converter is commonly a staircase. This staircase-like digital output is passed through a smoothing filter to reduce the effect of quantization noise.

The scheme given in figure is used either in full or in part in applications such as digital audio recording and playback, computer, music and video synthesis, pulse code modulation transmission, data acquisition, digital multimeter, direct digital control, digital signal processing, microprocessor based instrumentation.

Both ADC and DAC are also known as data converters and are available in IC form. It may be mentioned here that for slowly varying signal, sometimes sample and hold circuit may be avoided without considerable error.

Basic D/A Conversion Techniques

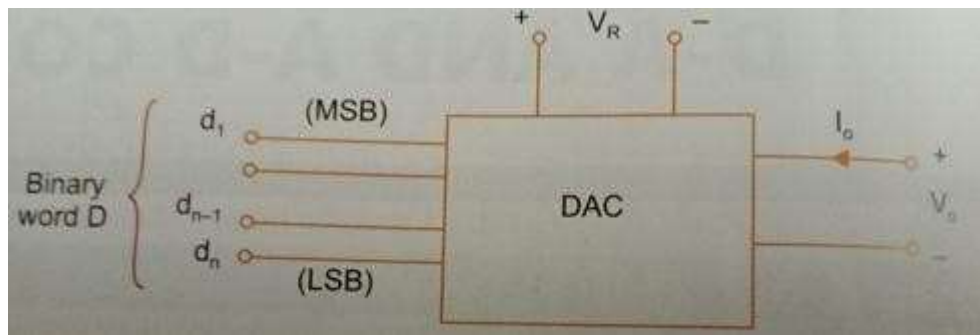


Fig 2.Schematic of a DAC(source: D.Roy Choudhry, Shail Jain, —Linear Integrated Circuits, New Age International Pvt. Ltd., 2018, Fifth Edition.)

Fig 2 shown above is the schematic of a DAC.The i/p is a n-bit binary word D.& is combined with a reference voltage V_R . To give an analog o/p signal.The o/p of a DAC can be either a voltage or current.For a voltage o/p DAC ,the D/A converter is mathematically described as

$$V_o = KV_{FS}(d_12^{-1} + d_22^{-2} + \dots + d_n2^{-n})$$

where, V_o = output voltage

V_{FS} = full scale output voltage

K = scaling factor usually adjusted to unity

$d_1, d_2, \dots, d_n = n$ -

bit binary fractional word with the decimal point located at the left

$$\begin{aligned} d_1 &= \text{MSB with a weight of } V_{FS} \\ &= \text{LSB with a weight of } \frac{V_{FS}}{2^n} \end{aligned}$$

Types of DAC

- Weighted Resistor DAC
- R-2R Ladder DAC
- Voltage mode R-2R Ladder D/A converter
- Inverted or Current mode R-2R Ladder D/A converter

4.7 A/D USING VOLTAGE TO TIME CONVERSION

The Block diagram shows the basic voltage to time conversion type of A to D converter. Here the cycles of variable frequency source are counted for a fixed period. It is possible to make an A/D converter by counting the cycles of a fixed-frequency source for a variable period. For this, the analog voltage required to be converted to a proportional time period. Figure 4.7.1. Shown below is the diagram for A/D Using Voltage to Time Conversion.

As shown in the figure 4.7.1 a negative reference voltage $-V_R$ is applied to an integrator, whose output is connected to the inverting input of the comparator. The output of the comparator is at 1 as long as the output of the integrator V_o is less than V_a .

At $t = T$, V_c goes low and switch S remains open. When V_{EN} goes high, the switch S is closed, thereby discharging the capacitor. Also the NAND gate is disabled. The waveforms are shown in figure 4.7.2.

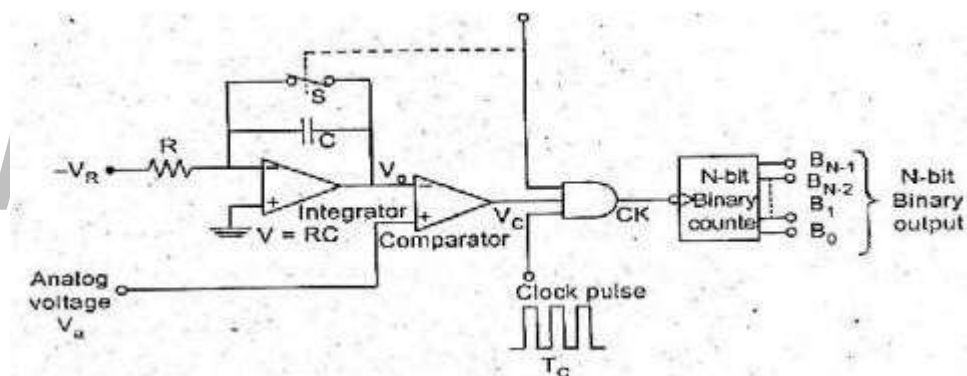


Figure 4.7.1 A/D Using Voltage to Time Conversion

[source: https://www.brainkart.com/subject/Linear-Integrated-Circuits_220/]

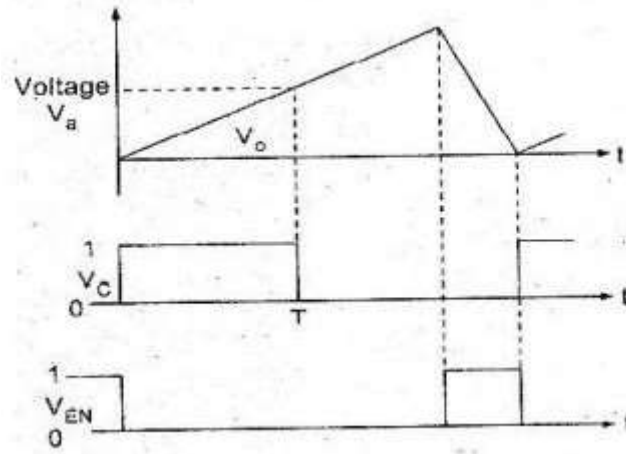


Figure 4.7.2. Wave form for conversion process

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DAC/ADC Specifications

Both D/A and A/D converters are available with wide range of specifications specified by manufacturer.

Resolution:

The resolution of a converter is the smallest change in voltage which may be produced at the output (or input) of the converter. For example, an 8-bit D/A converter has $2^8 - 1 = 255$ equal intervals. Hence the smallest change in output voltage is $(1/255)$ of the full scale output range.

$$\text{Resolution} = \frac{V_{FS}}{2^n - 1} = 1\text{LSB increment}$$

The resolution of an A/D converter is defined as the smallest change in analog input for a one bit change at the output. Example, the input range of an 8-bit A/D converter is divided into 255 intervals. The following table 1 shows the resolution for 6 to 16 bit DACs

S.No.	Bits	Intervals	LSB size (% of full-scale)	LSB size (For a 10 V full-scale)
1.	6	63	1.588	158.8 mV
2.	8	255	0.392	39.2 mV
3.	10	1023	0.0978	9.78 mV
4.	12	4095	0.0244	2.44 mV
5.	14	16383	0.0061	0.61 mV
6.	16	65535	0.0015	0.15 mV

Table 1. Resolution for 6 to 16 bit DACs (source: D.Roy Choudhry, Shail Jain, —Linear Integrated Circuits, New Age International Pvt. Ltd., 2018, Fifth Edition.)

Linearity:

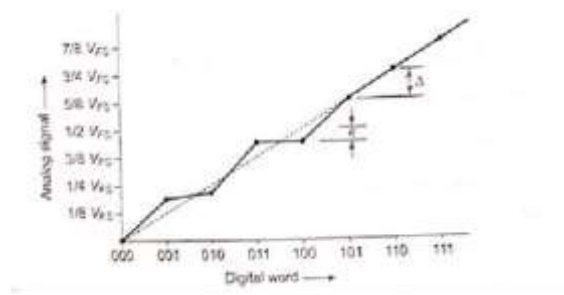


Fig 1 Linearity error of a 3-bit D/A converter (source: S.Salivahanan & V.S. Kanchana Bhaskaran, —Linear Integrated Circuits, TMH, 2nd Edition, 4th Reprint, 2016.)

The linearity of an A/D or D/A converter is an important measure of its accuracy. In an ideal DAC, equal increment in the digital input should produce equal increment in the analog output and the transfer curve should be linear. In an actual DAC, output voltages do not fall on

a straight line because of gain and offset errors as shown by the solid line curve. The static performance of a DAC is determined by fitting a straight line through the measured output points. Linearity error of a 3-bit D/A converter is shown in fig 1.

The linearity error measures the deviation of the actual output from the fitted line and is given by ϵ/Δ . The error is usually expressed as a fraction of LSB increment or percentage of full scale voltage. A good converter exhibits a linearity error of less than $\pm(1/2)\text{LSB}$.

Accuracy :

Absolute accuracy is the maximum deviation between the actual converter output and the ideal converter output. Relative accuracy is the maximum deviation after gain and offset errors have been removed.

Monotonicity :

A monotonic DAC is the one whose analog output increases for an increase in digital input. A monotonic characteristics is essential in control applications, otherwise oscillations can result. If a DAC has to be monotonic, the error should be less than $\pm(1/2)\text{LSB}$ at each output level.

Settling time :

Settling time represents the time it takes for the output to settle within a specified band $\pm(1/2)\text{LSB}$ of its final value, after the change in digital input. It should be as small as possible. Settling time ranges from 100 ns to 10 μs depending on word length and type of circuit used.

Stability :

The performance of converter changes with temperature, age and power supply variations. So all the relevant parameters such as offset, gain, linearity error and monotonicity must be specified over the full temperature and power supply ranges.

4.5 HIGH SPEED SAMPLE AND HOLD CIRCUITS

Introduction:

Sample-and-hold (S/H) is an important analog building block with many applications, including analog-to-digital converters (ADCs) and switched-capacitor filters. The function of the S/H circuit is to sample an analog input signal and hold this value over a certain length of time for subsequent processing.

Taking advantages of the excellent properties of MOS capacitors and switches, traditional switched capacitor techniques can be used to realize different S/H circuits. The simplest S/H circuit in MOS technology is shown in Figure 4.5.1, where V_{in} is the input signal, M_1 is an MOS transistor operating as the sampling switch, C_s is the hold capacitor, ck is the clock signal, and V_{out} is the resulting sample-and-hold output signal.

As depicted by Figure 4.5.1, in the simplest sense, a S/H circuit can be achieved using only one MOS transistor and one capacitor. The operation of this circuit is very straightforward.

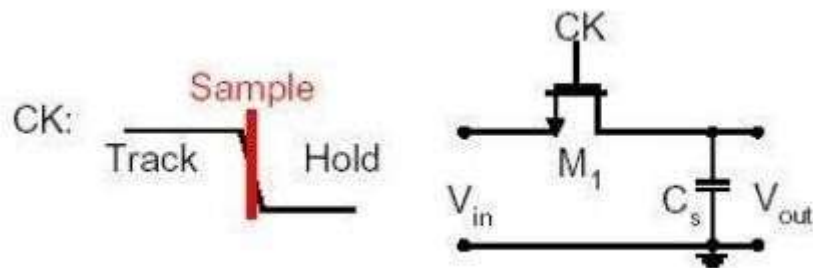


Figure 4.5.1 simplest sample and hold circuits in MOS technology

[source: https://www.brainkart.com/subject/Linear-Integrated-Circuits_220/]

Whenever ck is high, the MOS switch is on, which in turn allows V_{out} to track V_{in} . On the other hand, when ck is low, the MOS switch is off. During this time, C_h will keep V_{out} equal to the value of V_{in} at the instance when ck goes low.

Unfortunately, in reality, the performance of this S/H circuit is not as ideal as described above. The two major types of errors occur. They are charge injection and clock feed through,

that are associated with this S/H implementation. Three new S/H techniques, all of which try to minimize the errors caused by charge injection and/or clock feed through.

ALTERNATIVE CMOS SAMPLE-AND-HOLD CIRCUITS

Three alternative CMOS S/H circuits that are developed with the intention to minimize charge injection and/or clock feed through are

SERIES SAMPLING

The S/H circuit of Figure 4.5.4 is classified as parallel sampling because the hold capacitor is in parallel with the signal. In parallel sampling, the input and the output are dc-coupled. On the other hand, the S/H circuit shown in Figure 4.5.2 is referred to as series sampling because the hold capacitor is in series with the signal.

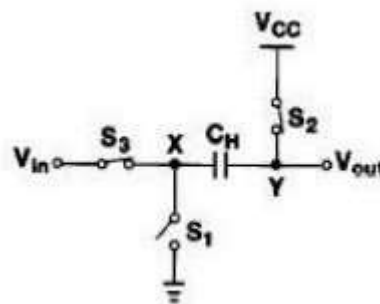


Figure 4.5.2 Series Sampling

[source: https://www.brainkart.com/subject/Linear-Integrated-Circuits_220/]

When the circuit is in sample mode, both switches S_2 and S_3 are on, while S_1 is off. Then, S_2 is turned off first, which means V_{out} is equal to V_{CC} (or V_{DD} for most circuits) and the voltage drop across Ch will be $V_{CC} - V_{in}$. Subsequently, S_3 is turned off and S_1 is turned on simultaneously. By grounding node X , V_{out} is now equal to $V_{CC} - V_{in}$, and the drop from V_{CC} to $V_{CC} - V_{in}$ is equal to the instantaneous value of the input.

As a result, this is actually an inverted S/H circuit, which requires inversion of the signal at a later stage. Since the hold capacitor is in series with the signal, series sampling can isolate the common-mode levels of the input and the output.

This is one advantage of series sampling over parallel sampling. In addition, unlike parallel sampling, which suffers from signal-dependent charge injection, series sampling does not exhibit such behavior because S_2 is turned off before S_3 . Thus, the fact that the gate-to-source voltage, V_{GS} , of S_2 is constant means that charge injection coming from S_2 is also constant (as opposed to being signal-dependent), which means this error can be easily eliminated through differential operation.

Limitations:

On the other hand, series sampling suffers from the nonlinearity of the parasitic capacitance at node Y . This parasitic capacitance introduces distortion to the sample-and hold value, thus mandating that C_h be much larger than the parasitic capacitance. On top of this disadvantage, the settling time of the S/H circuit during hold mode is longer for series sampling than for parallel sampling. The reason for this is because the value of V_{out} in series sampling is being reset to V_{CC} (or V_{DD}) for every sample, but this is not the case for parallel sampling.

SWITCHED OP-AMP BASED SAMPLE-AND-HOLD CIRCUIT

This S/H technique takes advantage of the fact that when a MOS transistor is in the saturation region, the channel is pinched off and disconnected from the drain. Therefore, if the hold capacitor is connected to the drain of the MOS transistor, charge injection will only go to the source junction, leaving the drain unaffected. Based on this concept, a switched op- amp (SOP) based S/H circuit, as shown in Figure 4.5.3 .

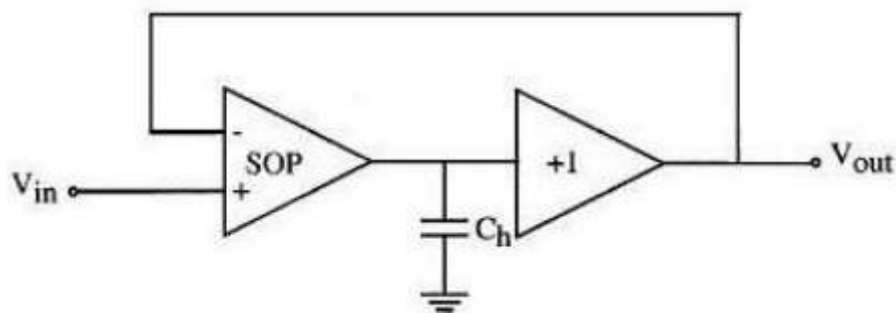


Figure 4.5.3. switched op- amp (SOP) based S/H circuit

[source: https://www.brainkart.com/subject/Linear-Integrated-Circuits_220/]

During sample mode, the SOP behaves just like a regular op-amp, in which the value of the output follows the value of the input. During hold mode, the MOS transistors at the output node of the SOP are turned off while they are still operating in saturation, thus preventing any channel charge from flowing into the output of the SOP. In addition, the SOP is shut off and its output is held at high impedance, allowing the charge on C_s to be preserved throughout the hold mode. On the other hand, the output buffer of this S/H circuit is always operational during sample and hold mode and is always providing the voltage on C_s to the output of the S/H circuit.

S/H circuits that operate in closed loop configuration can achieve high resolution, but their requirements for high gain circuit block, such as an op-amp, limits the speed of the circuits. As a result, better and faster S/H circuits must be developed.

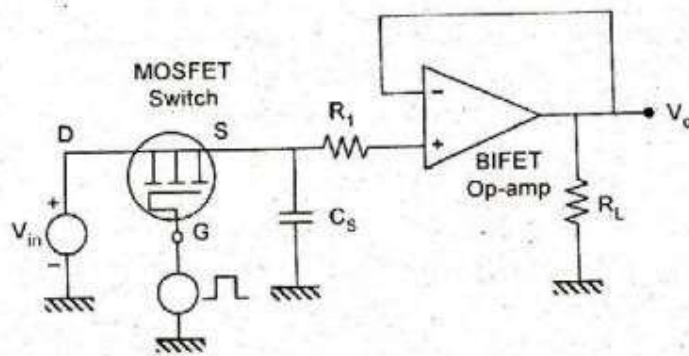


Figure 4.5.4.High speed sample and holds circuit with MOSFET

[source: https://www.brainkart.com/subject/Linear-Integrated-Circuits_220/]

The above figure 4.5.4 shows a sample and holds circuit with MOSFET as Switch acting as a sampling device and also consists of a holding capacitor C_s to store the sample values until the next sample comes in. This is a high speed circuit as it is apparent that CMOS switch has a very negligible propagation delay.

Three S/H circuits to reduce error:

- series sampling
- SOP based S/H circuit
- bottom plate S/H circuit with bootstrapped switch

4.8 SIGMA-DELTA ADCS/ OVER SAMPLING CONVERTERS

It consists of 2 main parts - modulator and digital filter. The modulator includes an integrator and a comparator with a feedback loop that contains a 1-bit DAC. The modulator oversamples the input signal, converting it to a serial bit stream with a frequency much higher than the required sampling rate. This is then transformed by the output filter to a sequence of parallel digital words at the sampling rate.

The characteristics of sigma-delta converters are

- high resolution
- high accuracy
- Low noise and low cost.
- Typical applications are for speech and audio.

A **Sigma-Delta ADC** (also known as a Delta-Sigma ADC) oversamples the desired signal by a large factor and filters the desired signal band. Generally, a smaller number of bits than required are converted using a Flash ADC after the Filter. The resulting signal, along with the error generated by the discrete levels of the Flash, is fed back and subtracted from the input to the filter. This negative feedback has the effect of noise shaping the error due to the Flash so that it does not appear in the desired signal frequencies.

A digital filter (decimation filter) follows the ADC which reduces the sampling rate, filters off unwanted noise signal and increases the resolution of the output. (sigma-delta modulation, also called delta-sigma modulation). sigma-delta ADCs is shown in figure 4.8.1

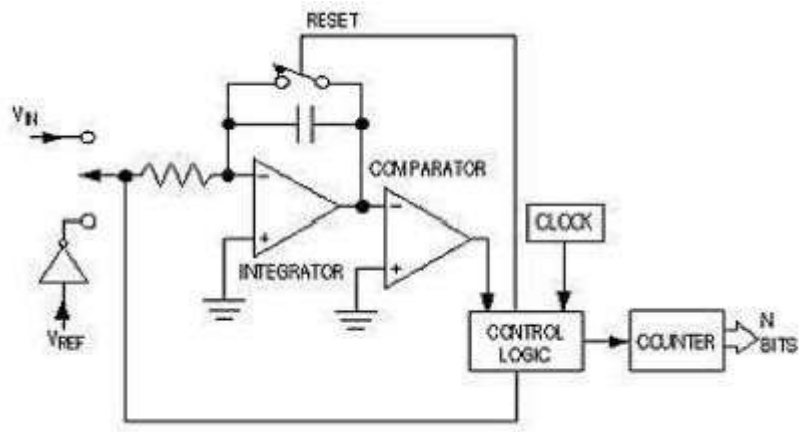


Figure 4.8.1. sigma-delta ADCs/over sampling converters

[source: https://www.brainkart.com/subject/Linear-Integrated-Circuits_220/]

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4.4 SWITCHES FOR DAC

The Switches which connects the digital binary input to the nodes of a D/A converter is an electronic switch. Although switches can be made of using diodes, bipolar junction Transistors, Field Effect transistors or MOSFETs, there are four main configurations used as switches for DACs. They are

- Switches using overdriven Emitter Followers.
- Switches using MOS Transistor- Totem pole MOSFET Switch and CMOS Inverter
- Switch.
- CMOS switch for Multiplying type DACs.
- CMOS Transmission gate switches.

These configurations are used to ensure the high speed switching operations for different types of DACs.

SWITCHES USING OVERDRIVEN EMITTER FOLLOWERS

The bipolar transistors have a negligible resistance when they are operated in saturation. The bipolar transistor operating in saturation region indicates a minimum resistance and thus represents ON condition. When they are operating in cut-off region indicates a maximum resistance and thus represents OFF condition.

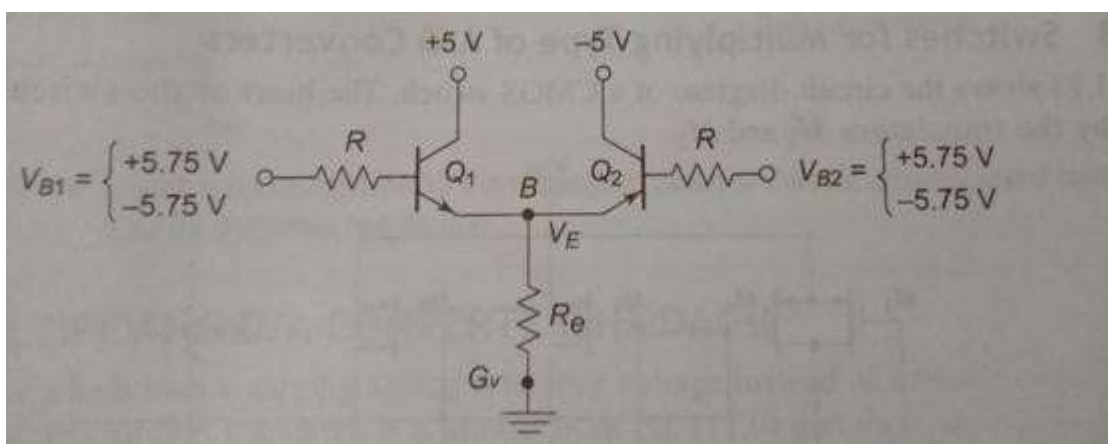


Figure 4.4.1 Switches for D/A converters using overdriven emitter followers

[source: "Linear Integrated Circuits" by S.Salivahanan & V.S. Kanchana Bhaskaran, Page-461]

The circuit shown in figure 4.4.1 is the arrangement of two transistors connected as emitter followers. A silicon transistor operating in saturation will have an offset voltage of 0.2V dropped across them. To have a zero offset voltage condition, the transistors must be overdriven because the saturation factor becomes negative. The two transistors Q1 (NPN) and Q2 (PNP) acts as a double pole switch. The bases of the transistors are driven by +5.75V and -5.75V.

Case 1:

When $V_{B1} = V_{B2} = +5.75V$, Q1 is in saturation and Q2 is OFF. And $V_E \approx 5V$ with $V_{BE1} = V_{BE2} = 0.75V$

Case 2:

When $V_{B1} = V_{B2} = -5.75V$, Q2 is in saturation and Q1 is OFF. And $V_E \approx -5V$ with $V_{BE1} = V_{BE2} = 0.75V$

Thus the terminal B of the resistor R_e is connected to either -5V or +5V depending on the input bit.

SWITCHES USING MOS TRANSISTOR

i) TOTEM POLE MOSFET SWITCH

As shown in the figure 4.4.2, the totem pole MOSFET Switch is connected in series with resistors of R-2R network. The MOSFET driver is connected to the inverting terminal of the summing op-amp.

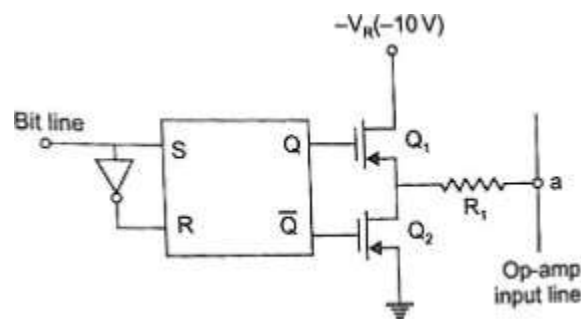


Figure 4.4.2. Totem pole MOSFET Switch

[source: "Linear Integrated Circuits" by S.Salivahan & V.S. Kanchana Bhaskaran, Page-462]

The complementary outputs Q and \bar{Q} drive the gates of the MOSFET M_1 and M_2 respectively. The SR flip flop holds one bit of digital information of the binary word under conversion. Assuming the negative logic (-5V for logic 1 and +5V for logic 0) the operation is given as two cases.

Case 1:

When the bit line is 1 with $S=1$ and $R=0$ makes $Q=1$ and $\bar{Q}=0$. This makes the transistor M_1 ON, thereby connecting the resistor R to reference voltage $-V_R$. The transistor M_2 remains in OFF condition.

Case 2:

When the bit line is 0 with $S=0$ and $R=1$ makes $Q=0$ and $\bar{Q}=1$. This makes the transistor M_2 ON, thereby connecting the resistor R to Ground. The transistor M_1 remains in OFF condition.

ii) CMOS INVERTER SWITCH

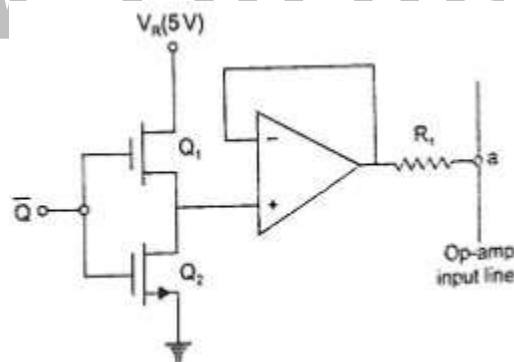


Figure 4.4.3 CMOS Inverter Switch

[source: "Linear Integrated Circuits" by S.Salivahanan & V.S. Kanchana Bhaskaran, Page-462]

The figure 4.4.3 of CMOS inverter is shown here. It consists of a CMOS inverter connected with an op-amp acting as a buffer. The buffer drives the resistor R with very low output impedance. Assuming positive logic (+5V for logic 1 and 0V for logic 0), the operation can be explained in two cases.

Case1:

When the complement of the bit line Q is low, M_1 becomes ON connecting V_R to the non-inverting input of the op-amp. This drives the resistor R HIGH.

Case2:

When the complement of the bit line Q is high, M_2 becomes ON connecting Ground to the non-inverting input of the op-amp. This pulls the resistor R LOW (to ground).

CMOS SWITCH FOR MULTIPLYING TYPE DACS

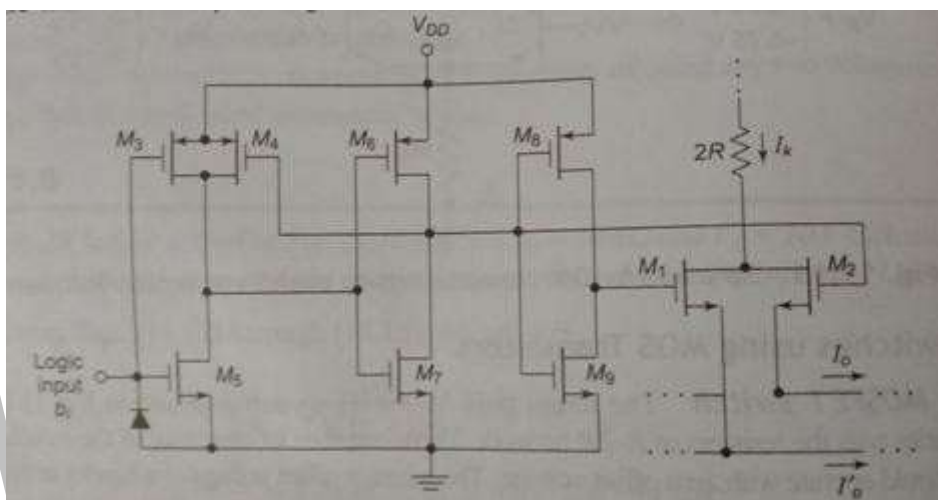


Figure 4.4.4 CMOS switch for Multiplying type DACs

[source: "Linear Integrated Circuits" by S.Salivahanan & V.S. Kanchana Bhaskaran, Page-462]

The CMOS switch for Multiplying type DACs is shown in figure 4.4.4. The heart of the switching element is formed by transistors M_1 and M_2 . The remaining transistors accept TTL or CMOS compatible logic inputs and provides the anti-phase gate drives for the transistors M_1 and M_2 . The operation for the two cases is as follows.

Case 1:

When the logic input is 1, M_1 is ON and M_2 is OFF. Thus current I_K is diverted to I_o bus.

Case 2:

When the logic input is 0, M_2 is ON and M_1 is OFF. Thus current I_K is diverted to I_o bus.

CMOS TRANSMISSION GATE SWITCHES

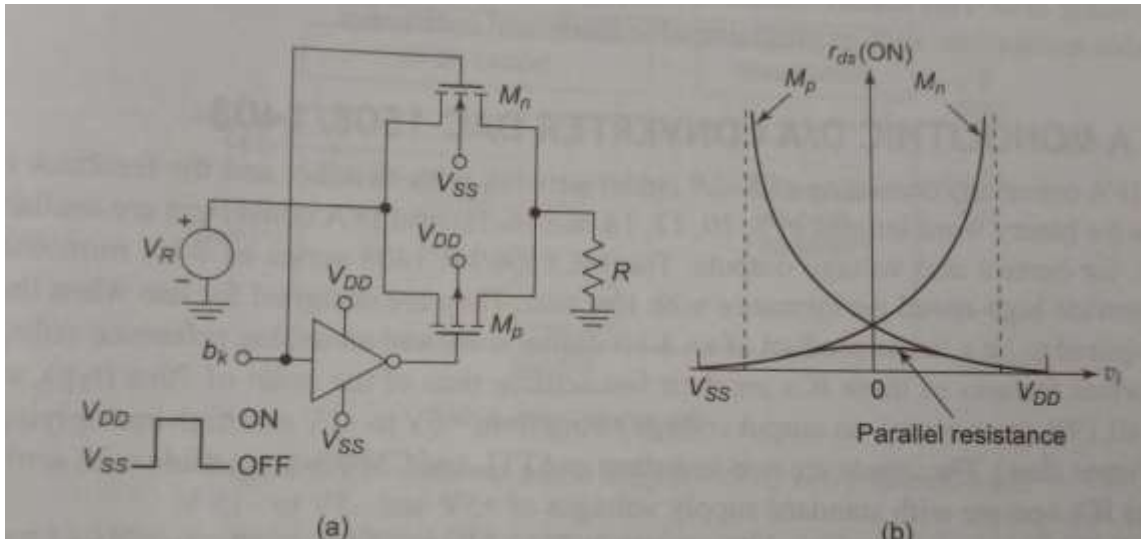


Figure 4.4.5a).Switches using CMOS transmission gate and

Figure 4.4.5 b) is its dynamic characteristics

[source: "Linear Integrated Circuits" by S.Salivahanan & V.S. Kanchana Bhaskaran, Page-463]

The disadvantage of using individual NMOS and PMOS transistors are threshold voltage drop (NMOS transistor passing only minimum voltage of $V_R - V_{TH}$ and PMOS transistor passing minimum voltage of V_{TH}). This is eliminated by using transmission gates which uses a parallel connection of both NMOS and PMOS. The arrangement shown in figure 4.4.5 a) can pass voltages from V_R to $0V$ acting as a ideal switch. The following cases explain the operation.

Case 1:

When the bit-line b_k is HIGH, both transistors M_n and M_p are ON, offering low resistance over the entire range of bit voltages.

Case 2:

When the bit-line b_k is LOW, both the transistors are OFF, and the signal transmission is inhibited (Withdrawn).

Figure 4.4.5 b) shows the dynamic characteristics. Thus the NMOS offers low resistance in the lower portion of the signal and PMOS offers low resistance in the upper portion of the signal. As a combination, they offer a low parallel resistance throughout the operating range of voltage. Wide varieties of these kinds of switches were available. Example: CD4066 and CD4051.

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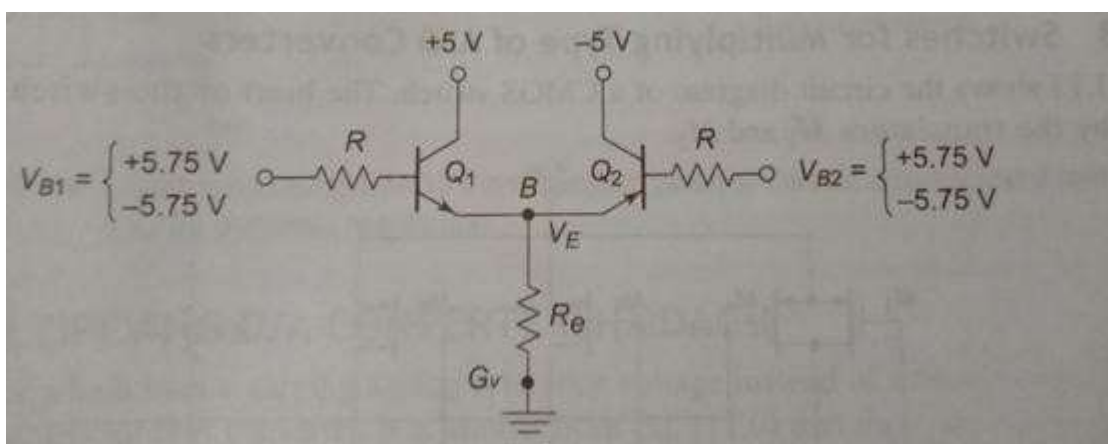


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Case 2:

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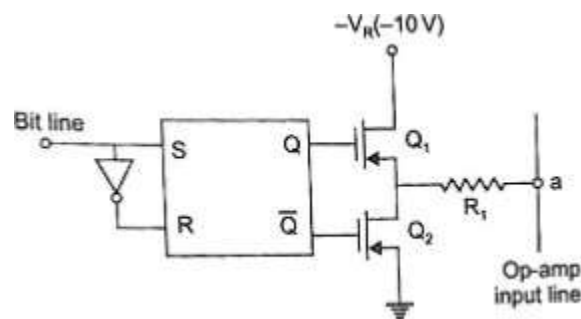


Figure 4.4.2. Totem pole MOSFET Switch

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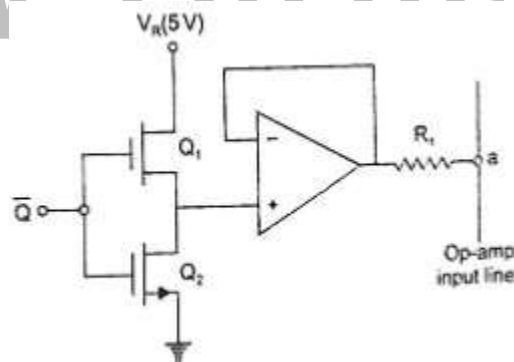


Figure 4.4.3 CMOS Inverter Switch

[source: "Linear Integrated Circuits" by S.Salivahanan & V.S. Kanchana Bhaskaran, Page-462]

The figure 4.4.3 of CMOS inverter is shown here. It consists of a CMOS inverter connected with an op-amp acting as a buffer. The buffer drives the resistor R with very low output impedance. Assuming positive logic (+5V for logic 1 and 0V for logic 0), the operation can be explained in two cases.

Case1:

When the complement of the bit line Q is low, M_1 becomes ON connecting V_R to the non- inverting input of the op-amp. This drives the resistor R HIGH.

Case2:

When the complement of the bit line Q is high, M_2 becomes ON connecting Ground to the non- inverting input of the op-amp. This pulls the resistor R LOW (to ground).

CMOS SWITCH FOR MULTIPLYING TYPE DACS

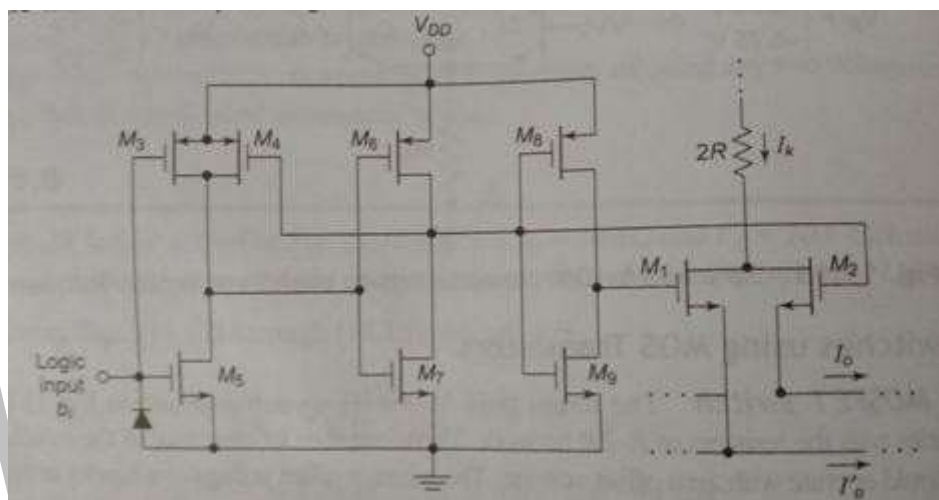


Figure 4.4.4 CMOS switch for Multiplying type DACs

[source: "Linear Integrated Circuits" by S.Salivahanan & V.S. Kanchana Bhaskaran, Page-462]

The CMOS switch for Multiplying type DACs is shown in figure 4.4.4. The heart of the switching element is formed by transistors M_1 and M_2 . The remaining transistors accept TTL or CMOS compatible logic inputs and provides the anti-phase gate drives for the transistors M_1 and M_2 . The operation for the two cases is as follows.

Case 1:

When the logic input is 1, M_1 is ON and M_2 is OFF. Thus current I_K is diverted to I_o bus.

Case 2:

When the logic input is 0, M_2 is ON and M_1 is OFF. Thus current I_K is diverted to Io bus.

CMOS TRANSMISSION GATE SWITCHES

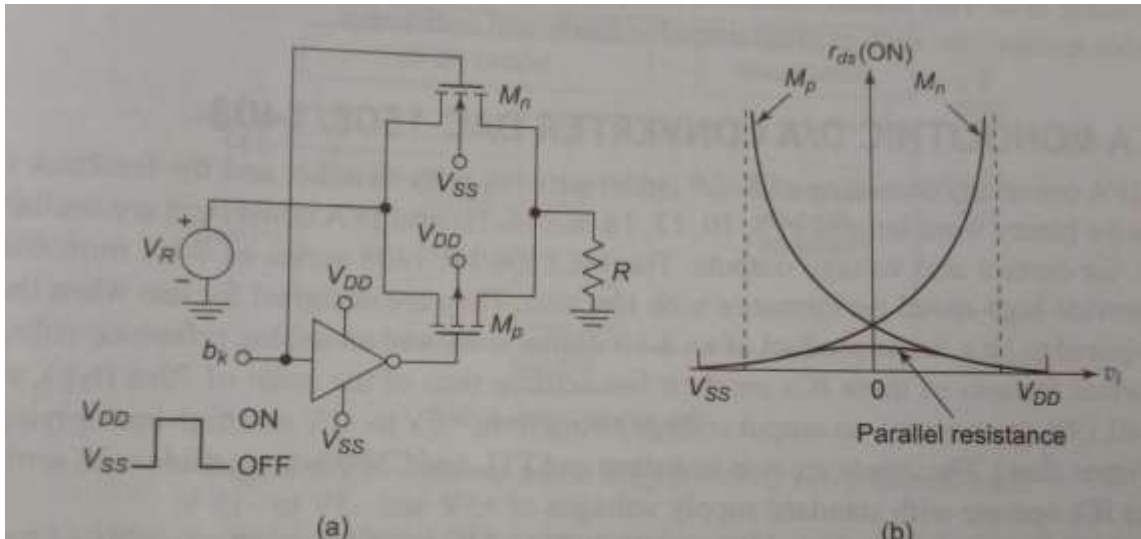


Figure 4.4.5a).Switches using CMOS transmission gate and

Figure 4.4.5 b) is its dynamic characteristics

[source: "Linear Integrated Circuits" by S.Salivahanan & V.S. Kanchana Bhaskaran, Page-463]

The disadvantage of using individual NMOS and PMOS transistors are threshold voltage drop (NMOS transistor passing only minimum voltage of $V_R - V_{TH}$ and PMOS transistor passing minimum voltage of V_{TH}). This is eliminated by using transmission gates which uses a parallel connection of both NMOS and PMOS. The arrangement shown in figure 4.4.5 a) can pass voltages from V_R to $0V$ acting as a ideal switch. The following cases explain the operation.

Case 1:

When the bit-line b_k is HIGH, both transistors M_n and M_p are ON, offering low resistance over the entire range of bit voltages.

Case 2:

When the bit-line b_k is LOW, both the transistors are OFF, and the signal transmission is inhibited (Withdrawn).

Figure 4.4.5 b) shows the dynamic characteristics. Thus the NMOS offers low resistance in the lower portion of the signal and PMOS offers low resistance in the upper portion of the signal. As a combination, they offer a low parallel resistance throughout the operating range of voltage. Wide varieties of these kinds of switches were available. Example: CD4066 and CD4051.

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4.6 TYPES OF ADC

FLASH TYPE ADC

Flash type ADC produces an equivalent digital output for a corresponding analog input in no time. Hence, flash type ADC is the fastest ADC. The circuit diagram of a 3-bit flash type ADC is shown in the following figure 4.6.1.

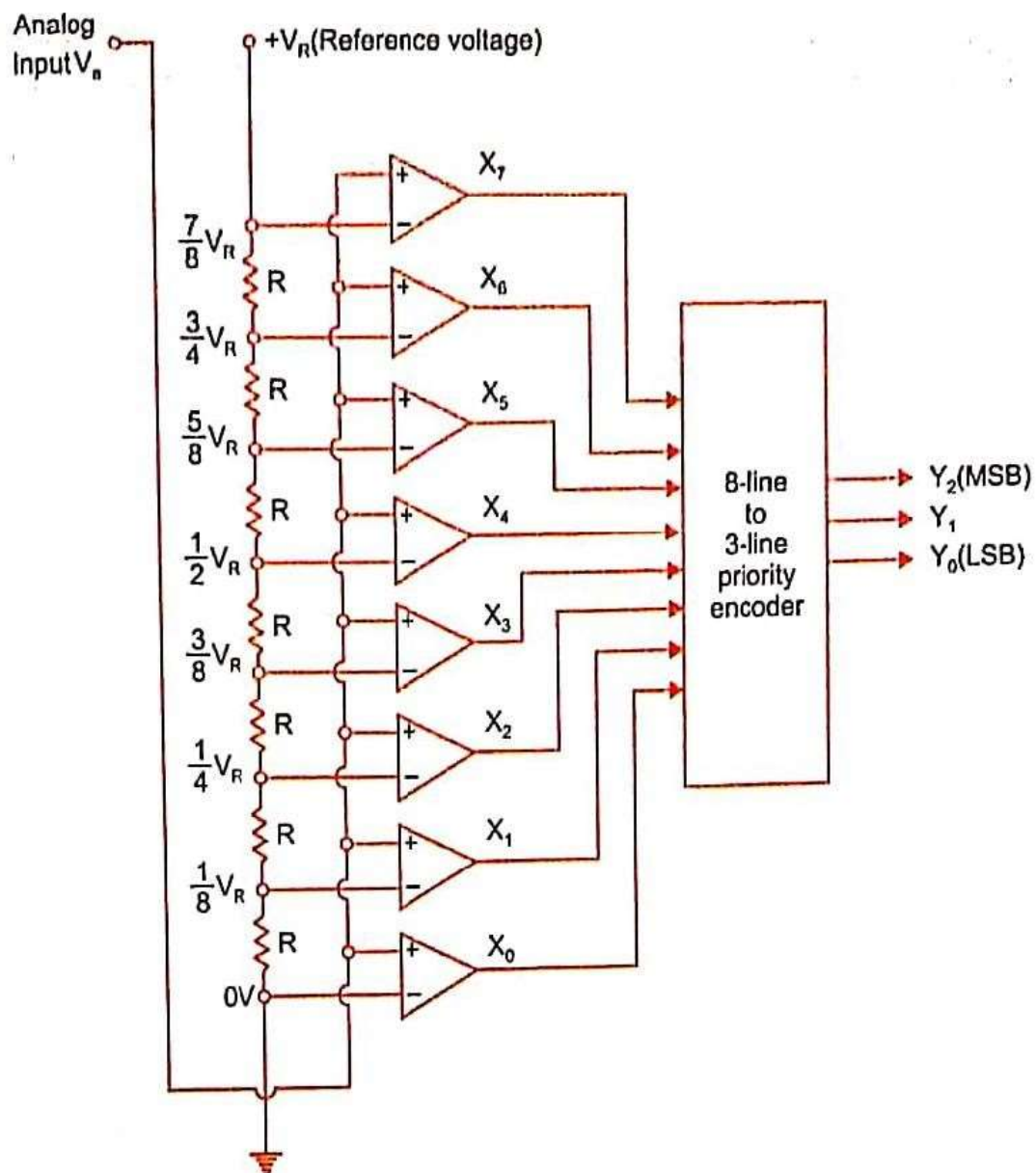


Figure 4.6.1. Basic circuit for flash type A/D converter

[source: "Linear Integrated Circuits" by D.Roy Choudhry, Shail Bala Jain, Page-413]

The 3-bit flash type ADC consists of a voltage divider network, 7 comparators and a priority encoder.

The **working** of a 3-bit flash type ADC is as follows.

- The **voltage divider network** contains 8 equal resistors. A reference voltage V_R is applied across that entire network with respect to the ground. The voltage drop across each resistor from bottom to top with respect to ground will be the integer multiples (from 1 to 8) of $V_R/8$.
- The external **input voltage** V_i is applied to the non-inverting terminal of all comparators. The voltage drop across each resistor from bottom to top with respect to ground is applied to the inverting terminal of comparators from bottom to top.
- At a time, all the comparators compare the external input voltage with the voltage drops present at the respective other input terminal. That means, the comparison operations take place by each comparator **parallelly**.
- The **output of the comparator** will be '1' as long as V_i is greater than the voltage drop present at the respective other input terminal. Similarly, the output of comparator will be '0', when, V_i is less than or equal to the voltage drop present at the respective other input terminal.
- All the outputs of comparators are connected as the inputs of **priority encoder**. This priority encoder produces a binary code (digital output), which is corresponding to the high priority input that has '1'.
- Therefore, the output of priority encoder is nothing but the binary equivalent (**digital output**) of external analog input voltage, V_i .

The flash type ADC is used in the applications where the conversion speed of analog input into digital data should be very high.

SUCCESSIVE APPROXIMATION TYPE ADC

Successive Approximation type ADC is the most widely used and popular ADC method. The conversion time is maintained constant in successive approximation type ADC, and is proportional to the number of bits in the digital output, unlike the counter and continuous type A/D converters. The basic principle of this type of A/D converter is that the unknown analog input voltage is approximated against an n-bit digital value by trying one bit at a time,

beginning with the MSB. The principle of successive approximation process for a 4-bit conversion is explained here. This type of ADC operates by successively dividing the voltage range by half, as explained in the following steps.

(1) The MSB is initially set to 1 with the remaining three bits set as 000. The digital equivalent voltage is compared with the unknown analog input voltage.

(2) If the analog input voltage is higher than the digital equivalent voltage, the MSB is retained as 1 and the second MSB is set to 1. Otherwise, the MSB is set to 0 and the second MSB is set to 1. Comparison is made as given in step (1) to decide whether to retain or reset the second MSB.

The above steps are more accurately illustrated with the help of an example. Let us assume that the 4-bit ADC is used and the analog input voltage is $V_A = 11\text{ V}$. when the conversion starts, the MSB bit is set to 1.

Now $V_A = 11\text{V} > V_D = 8\text{V} = [1000]_2$. Since the unknown analog input voltage V_A is higher than the equivalent digital voltage V_D , as discussed in step (2), the MSB is retained as 1 and the next MSB bit is set to 1 as follows $V_D = 12\text{V} = [1100]_2$

Now $V_A = 11\text{V} < V_D = 12\text{V} = [1100]_2$. Here now, the unknown analog input voltage V_A is lower than the equivalent digital voltage V_D . As discussed in step (2), the second MSB is set to 0 and next MSB set to 1 as $V_D = 10\text{V} = [1010]_2$

Now again $V_A = 11\text{V} > V_D = 10\text{V} = [1010]_2$. Again as discussed in step (2) $V_A > V_D$, hence the third MSB is retained to 1 and the last bit is set to 1. The new code word is $V_D = 11\text{V} = [1011]_2$. Now finally $V_A = V_D$, and the conversion stops. The functional block diagram of successive approximation type of ADC is shown in figure 4.6.2 below.

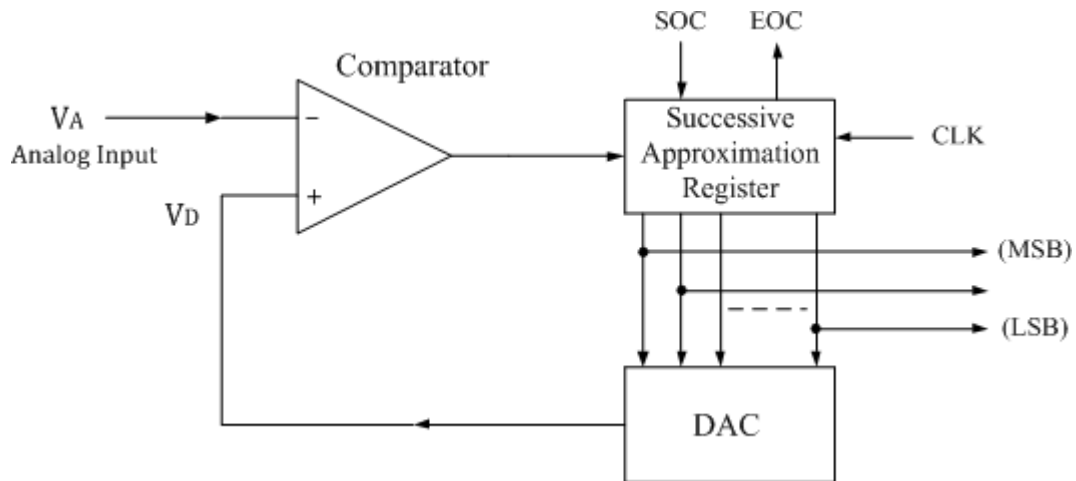


Figure 4.6.2 Functional diagram of successive approximation type of ADC

[<https://www.electronics-tutorial.net/analog-integrated-circuits/data-converters/successive-approximation-type-adc/>]

It consists of a successive approximation register (SAR), DAC and comparator. The output of SAR is given to n-bit DAC. The equivalent analog output voltage of DAC, V_D is applied to the non-inverting input of the comparator. The second input to the comparator is the unknown analog input voltage V_A . The output of the comparator is used to activate the successive approximation logic of SAR. When the start command is applied, the SAR sets the MSB to logic 1 and other bits are made logic 0, so that the trial code becomes 1000.

Advantages:

1. Conversion time is very small.
2. Conversion time is constant and independent of the amplitude of the analog input signal V_A .

Disadvantages:

1. Circuit is complex.
2. The conversion time is more compared to flash type ADC.

SINGLE SLOPE ADC

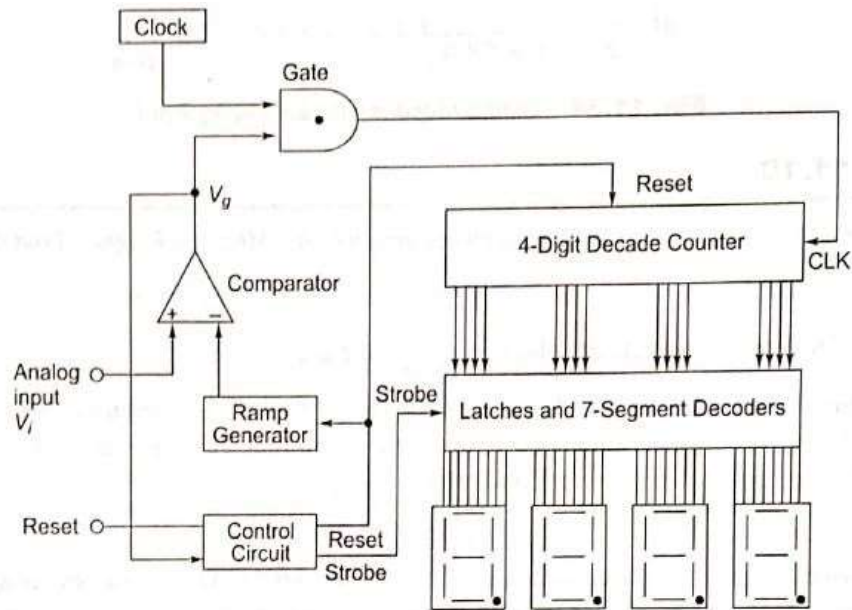


Figure 4.6.3. Block Diagram of single slope ADC

[source: "Linear Integrated Circuits" by S. Salivahanan & V.S. Kanchana Bhaskaran, Page-488]

Figure 4.6.3 shown above is the block diagram of single slope ADC. These converter techniques are based on comparing the unknown analog i/p voltage with a reference voltage that begins at 0v & increases linearly with time. The time required for the reference voltage to reach the value of unknown analog i/p voltage is proportional to the amplitude of unknown analog i/p voltage. The time period can be measured using a digital counter. The main circuit of this converter is a ramp generator which on receiving a RESET from the control circuit increases linearly with time from 0v to a max volt V_m . Assume a +ive analog i/p voltage V_i is applied at the non-inverting i/p of the comparator. When a RESET signal is applied to the control logic, the 4-digit decade counter resets to 0 & the ramp begins to increase. V_i is +ive the comparator o/p is in HIGH state.

This allows the clk pulse to pass to the i/p of the 4-digit counter through the AND gate & the counter is incremented. This process continues until the analog i/p voltage is greater than the ramp generator voltage. When the ramp generator voltage is equal to the analog i/p voltage, the comparator o/p becomes negatively saturated or logic 0. The clk is prevented from passing through the gate causing the counter operation. Then the control circuit generates a STROBE

signal, which latches the counter values in the 4-digit latch, which is displayed on 7-segment displays. The displayed value is then equivalent to the amplitude of analog input voltage.

DUAL SLOPE ADC

The analog part of the circuit consists of a high input impedance buffer A_1 , precision integrator A_2 and a voltage comparator. The converter first integrates the analog input signal V_a for a fixed duration of 2^n clk periods. Then it integrates an internal reference voltage V_R of opposite polarity until the integrator output is zero. Functional diagram of the dual slope ADC and Integrated output waveform for the dual slope ADC is shown in figure 4.6.4 a) and b).

Before the START command arrives, the switch SW_1 is connected to ground and SW_2 is closed. Any offset voltage present in the A_1, A_2 , comparator loop after integration appears across the capacitor CAZ till the threshold of the comparator is achieved. The capacitor CAZ thus provides automatic compensation for the input-offset voltages of all the three amplifiers.

Later when SW_2 opens, CAZ acts as a memory to hold the voltages required to keep the offset nulled. At the arrival of the START command at $t=t_1$, the control logic opens SW_2 and connects to V_a and enables the counter starting from zero. The circuit uses an n -stage ripple counter and therefore the counter resets to zero after counting 2^n pulses. The analog voltage V_a is integrated for a fixed number 2^n counts of clk pulses after which the counter resets to zero. If the clock period is T the integration take place for a time $T=2^n \times T$ and the output is a ramp going downwards.

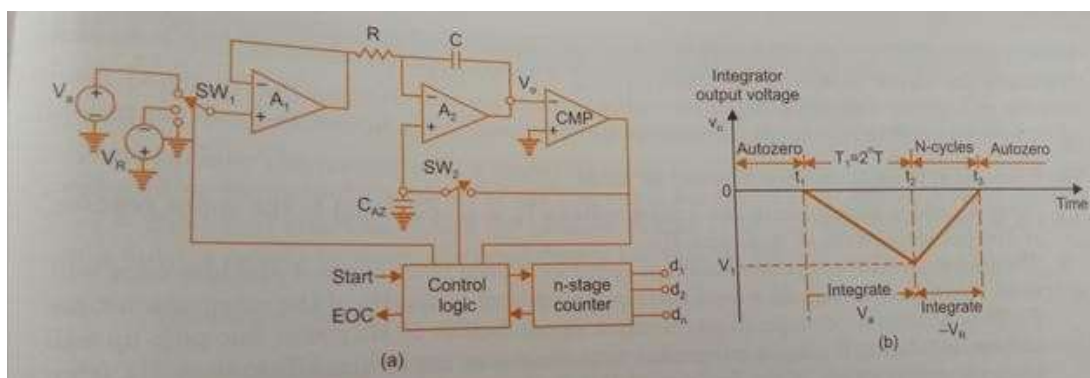


Figure 4.6.4.a) Functional diagram of the dual slope ADC b) Integrated output waveform for the dual slope ADC

[source: "Linear Integrated Circuits" by D.Roy Choudhry, Shail Bala Jain, Page-419]

The counter resets itself to zero at the end of the integral T_1 and the switch SW_1 is connected to the reference voltage $-V_R$. The output voltage V_o will now have a +ive slope. As long as V_o is -ive, the output of the comparator is +ive and the control logic allows the clock pulse to be counted. When V_o become just zero at time $t=t_3$, the control logic issues an end of conversion (EOC) command and no further clock pulses enter the counter.

$$T_1 = t_2 - t_1 = \frac{2^n \text{ counts}}{\text{clock rate}}$$

$$t_3 - t_2 = \frac{\text{digital count } N}{\text{clock rate}}$$

$$\text{For an integrator, } \Delta V_o = \left(-\frac{1}{RC}\right)V(\Delta t)$$

Voltage V_o will be equal to V_1 at the instant t_2 and can be given as

$$V_1 = \left(-\frac{1}{RC}\right)V_a(t_2 - t_1)$$

The voltage V_1 is also given by

$$V_1 = \left(-\frac{1}{RC}\right)(-V_R)(t_2 - t_3)$$

$$\text{so, } V_a(t_2 - t_1) = V_R(t_3 - t_2)$$

$$\text{sub } t_2 - t_1 = 2^n \text{ \& } t_3 - t_2 = N$$

$$V_a(2^n) = V_R(N)$$

$$V_a = V_R\left(\frac{N}{2^n}\right)$$