1.7 AC CHARACTERISTICS

For small signal sinusoidal (AC) application one has to know the ac characteristics such as frequency response and slew-rate.

FREQUENCY RESPONSE

The variation in operating frequency will cause variations in gain magnitude and its phase angle. The manner in which the gain of the op-amp responds to different frequencies is called the frequency response. Op-amp should have an infinite bandwidth BW =∞ (i.e.) if its open loop gain in 90dB with dc signal its gain should remain the same 90 dB through audio and onto high radio frequency. The op-amp gain decreases (roll-off) at higher frequency what reasons to decrease gain after a certain frequency reached. There must be a capacitive component in the equivalent circuit of the op-amp. For an op-amp with only one break (corner) frequency all the capacitors effects can be represented by a single capacitor C. Below figure 1.7.1 is a modified variation of the low frequency model with capacitor C at the output.

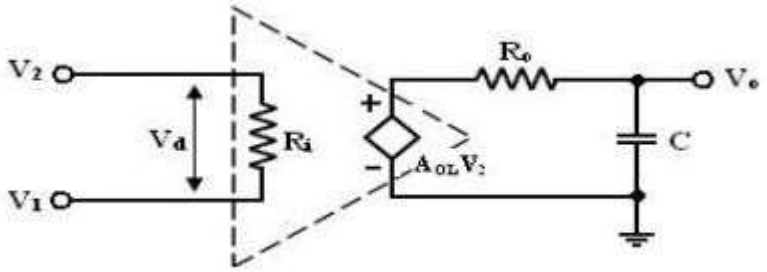

Figure1.7.1 High frequency model of an op-amp with single corner frequency

[source:"Linear Integrated Circuits"by D.Roy Choudhry, Shail Bala Jain, Page-125]

There is one pole due to R_0C and one -20dB/decade. The open loop voltage gain of an op-amp with only one corner frequency is obtained from above figure 1.7.1.f_1 is the corner frequency or the upper 3 dB frequency of the op-amp. The magnitude and phase angle of the open loop volt gain are f1 of frequency can be written as, The magnitude and phase angle characteristics:

1. For frequency $f << f_1$ the magnitude of the gain is 20 log AOL in db.
2. At frequency $f = f_1$ the gain in 3 dB down from the dc value of AOL in db. This

frequency f_1 is called corner frequency.

3. For f>> f_1 the fain roll-off at the rate off -20dB/decade or -6dB/decade. Figure 1.7. 2.shows the open loop magnitude characteristics and phase characteristics for an op-amp with single break frequency

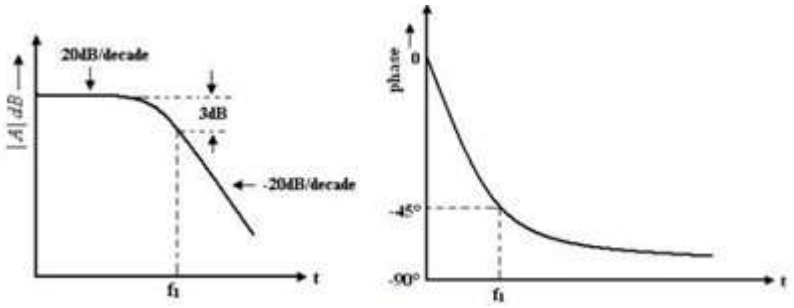

Figure 1.7.2 shows the open loop magnitude characteristics and phase characteristics for an op-amp with single break frequency

[source:"Linear Integrated Circuits"by D.Roy Choudhry, Shail Bala Jain, Page-126]

From the phase characteristics that the phase angle is zero at frequency f = 0. At the corner frequency f1 the phase angle is -45º (lagging and an infinite frequency the phase angle is -90 . It shows that a maximum of 90 phase change can occur in an op- amp with a single capacitor C. Zero frequency is taken as the decade below the corner frequency and infinite frequency is one decade above the corner frequency. Figure 1.7.3. Below shows the open loop gain vs frequency curve.

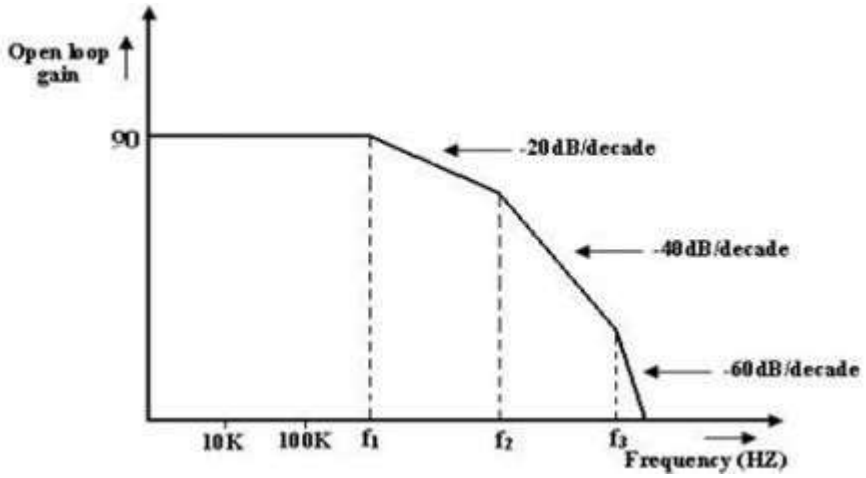

Figure 1.7.3 shows the open loop gain vs frequency curve

[source:"Linear Integrated Circuits"by D.Roy Choudhry, Shail Bala Jain, Page-127]

CIRCUIT STABILITY

A circuit or a group of circuit connected together as a system is said to be stable, if its o/p reaches a fixed value in a finite time. A system is said to be unstable, if its o/p increases with time instead of achieving a fixed value. In fact, the o/p of an unstable sys keeps on increasing until the system break down. The unstable system is impractical and need be made stable. The criterion given for stability is used when the system is to be tested practically. In theoretically, always used to test system for stability, ex: Bode plots. Bode plots are compared of magnitude Vs Frequency and phase angle Vs frequency. Any system whose stability is to be determined can represented by the block diagram shown in figure 1.7.4 below.

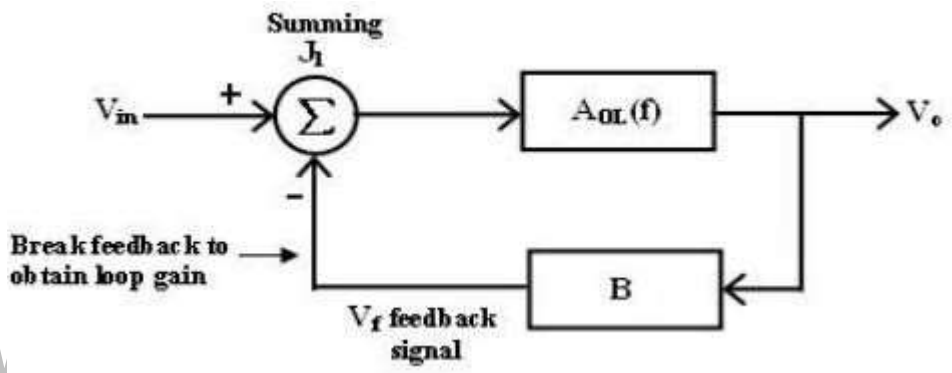

Figure 1.7.4 feedback loop system

[source: https://www.brainkart.com/subject/Linear-Integrated-Circuits_220/]

The block between the output and input is referred to as forward block and the block between the output signal and f/b signal is referred to as feedback block. The content of each block is referred as transfer frequency. From fig. we represented it by AOL (f) which is given by

$$A_{OL}(f) = V_0/V_{in} \text{ if } V_f = 0 \quad (1)$$

where A_{OL} (f) = open loop volt gain.

The closed loop gain A_f is given by $A_F = V_0/V_{in}$

$$= A_{OL} / (1+(A_{OL}) (B) \text{ ---- } (2)$$

B = gain of feedback circuit.

B is a constant if the feedback circuit uses only resistive components.Once the magnitude Vs frequency and phase angle Vs frequency plots are drawn, system stability may be determined as follows

Case 1:

Determine the phase angle when the magnitude of (AOL) (B) is 0dB (or) 1.If phase angle is >-180 , the system is stable. However, the some systems the magnitude may never be 0, in that cases method 2, must be used.

Case 2:

Determine the phase angle when the magnitude of (AOL) (B) is 0dB (or) 1.If phase angle is > - 180 , If the magnitude is –ve decibels then the system is stable. However, the some systems the phase angle of a system may reach -1800, under such conditions method 1 must be used to determine the system stability.

STABILITY SPECIFICATIONS

Gain cross over frequency: The frequency at which the loop gain magnitude $|A_{OL}(f)\beta|$ is unity ie,$20 \log|A_{OL}(f)\beta|=0$ is called gain cross over frequency.

Phase cross over frequency: The frequency at which the phase shift introduced by the loop gain is -180° or nπ radians is called phase cross over frequency.

FREQUENCY COMPENSATION

In applications where one desires large bandwidth and lower closed loop gain satiable compensation techniques are used. Two types of compensating techniques are used

1. External compensation
2. Internal compensation

EXTERNAL FREQUENCY COMPENSATION

Some types of op-amp are made to be used with externally connected compensating components specially if they are to be used for relatively low closed loop gain. The compensating network alters the open loop gain so that the roll-off rate is -20

dB/decade over a wide range of frequency. The common methods for accomplishing this are:

Dominant-pole compensation

Pole-zero (lag) compensation

DOMINANT-POLE COMPENSATION

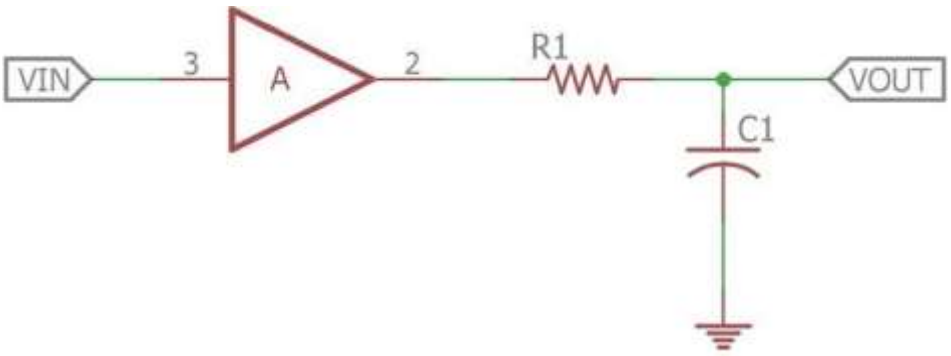

Figure 1.7.5 Dominant-pole compensation

[source: https://circuitdigest.com/tutorial/frequency-compensation-of-op-amp]

Suppose A is the uncompensated transfer function of the op-amp in open-loop condition as given by

$$A = \frac{A_{0L}.\omega_1.\omega_2.\omega_3}{(s+\omega_1)(s+\omega_2)(s+\omega_3)}$$

Introduce a dominant pole by adding RC-network in series with op-amp as in fig 5.or by connecting a capacitor C from a suitable high resistance point to ground. Gain vs Frequency curve for dominant pole compensation is shown in figure1.7.6. The compensated transfer function A' becomes

$$A' = \frac{V_o}{V_1}$$

$$= A.\frac{\frac{-j}{\omega C}}{R - \frac{j}{\omega C}} = \frac{A}{1 + j\frac{f}{f_d}}$$

where, $f_d = \frac{1}{2\pi Rc}$

Using equation A=

$$\frac{A_{OL}}{\left(i + j\frac{f}{f_1}\right)\left(i + j\frac{f}{f_2}\right)\left(i + j\frac{f}{f_3}\right)}; o < f_1 < f_2 < f_3$$

We get, A'=

$$\frac{A_{OL}}{\left(i + j\frac{f}{f_1}\right)\left(i + j\frac{f}{f_2}\right)\left(i + j\frac{f}{f_3}\right)}; o < f_1 < f_2 < f_3$$

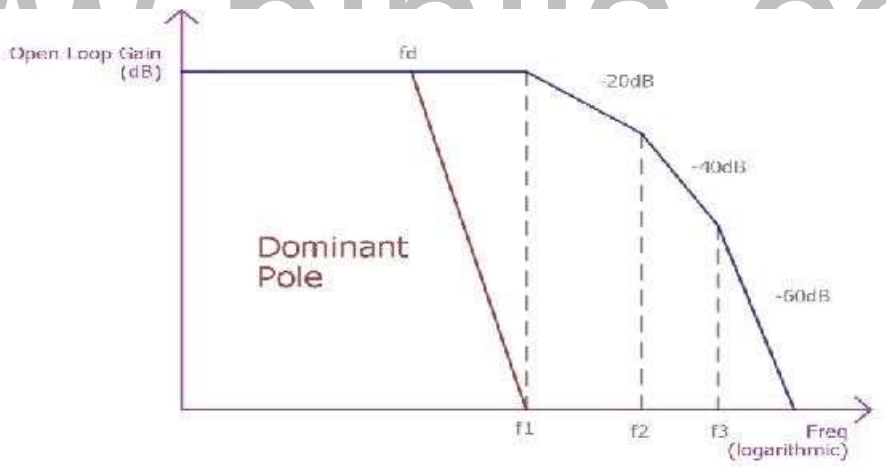

Figure 1.7.6 Gain vs Frequency curve for dominant pole compensation

[source:"Linear Integrated Circuits"by D.Roy Choudhry, Shail Bala Jain, Page-133]

Disadvantages :

It reduces the open –loop bandwidth drastically. But the noise immunity of the system is improved since the noise frequency components outside the bandwidth are eliminated.

POE-ZERO COMPENSATION

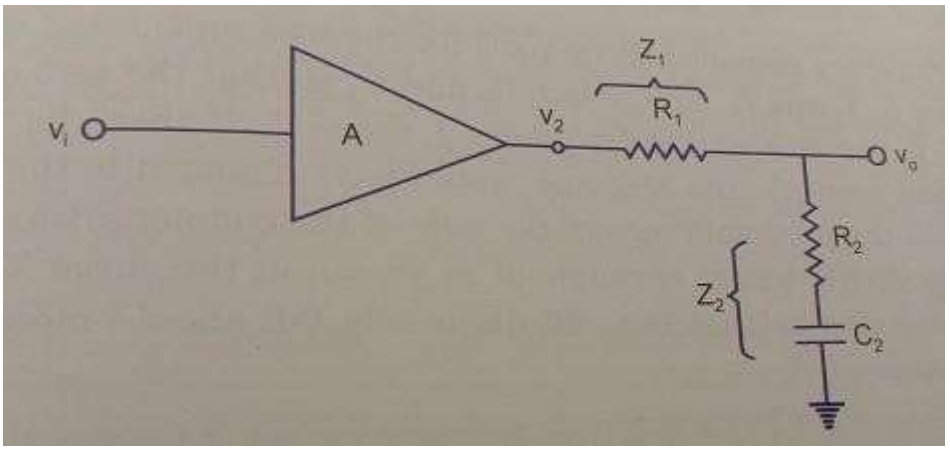

Figure 1.7.7 pole-zero compensation

[source:"Linear Integrated Circuits"by D.Roy Choudhry, Shail Bala Jain, Page-133]

Here the uncompensated transfer function A is altered by adding both pole and a zero as shown in figure1.7.7.The zero should be at higher frequency than pole.The transfer function of the compensating network alone is ,

$$\frac{V_o}{V_1} = \frac{Z_2}{Z_1 + Z_2} = \frac{R_2}{R_1 + R_2} \frac{1 + j\frac{f}{f_1}}{1 + j\frac{f}{f_0}}$$

$$\text{where, } Z_1 = R_1 \text{ , } Z_2 = R_2 + \frac{1}{j\omega C_2} \text{ , } f_1 = \frac{1}{2\pi R_2 c_2} \text{ , } f_0 = \frac{1}{2\pi(R_1 + R_2)C_2}$$

The compensating network is designed to produce a zero at the first corner frequency f_1 of the uncompensated transfer function A. Figure 1.7.8.shown below is the open loop gain vs frequency for Pole-zero compensation.

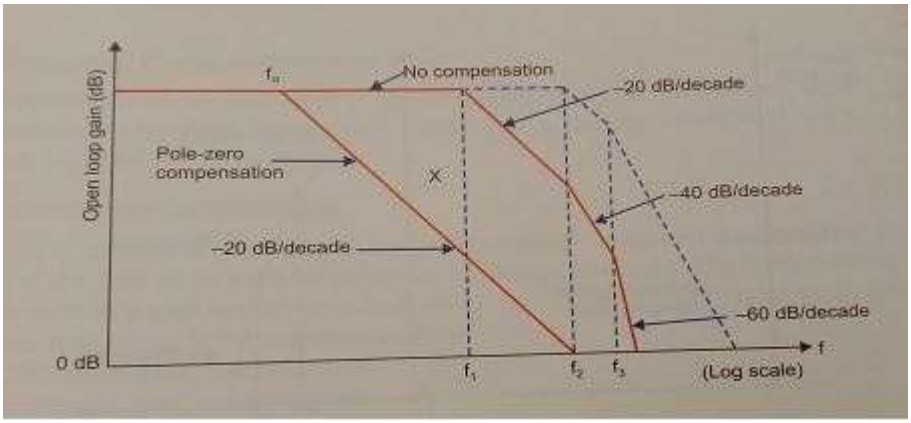

Figure1.7.8.open loop gain vs frequency for Pole-zero compensation

[source:"Linear Integrated Circuits"by D.Roy Choudhry, Shail Bala Jain, Page-135]

The compensated transfer function is given as

$$A' = \frac{V_o}{V_1} = \frac{V_o}{V_2} = \frac{V_2}{V_1} = A.\frac{R_2 \quad 1+j\frac{f}{f_1}}{R_1+R_2 1+j\frac{f}{f_0}}$$

$$= \frac{A_{OL}}{\left(i+j\frac{f}{f_1}\right)\left(i+j\frac{f}{f_2}\right)\left(i+j\frac{f}{f_3}\right)} \cdot \frac{R_2 \quad 1+j\frac{f}{f_1}}{R_1+R_2 1+j\frac{f}{f_0}}$$

$$= \frac{A_{OL}}{\left(i+j\frac{f}{f_1}\right)\left(i+j\frac{f}{f_2}\right)\left(i+j\frac{f}{f_3}\right)}$$

with $0 < f_o < f_1 < f_2 < f_3$

INTERNAL COMPENSATION

In this case we are not using any compensation techniques. During the fabrication of IC we are compensating and designing the IC. Capacitor is fabricated internally and miller effect compensation is used.

SLEW RATE

The rate of change of output voltage with respect to time is called slew rate. It can be represented as V/μsec

$$SR = \frac{dVo}{dt}/max \text{ or } SR = \frac{I_{max}}{}$$

1.5 BASIC INFORMATION ABOUT OPERATIONAL AMPLIFIERS

An operational amplifier is a direct coupled high gain amplifier consisting of one or more differential amplifiers, followed by a level translator and an output stage. It is a versatile device that can be used to amplify ac as well as dc input signals & designed for computing mathematical functions such as addition, subtraction ,multiplication, integration & differentiation.

IDEAL OPERATIONAL AMPLIFIERS

Infinite input resistance R_i, so that almost any signal source can drive it and there is no loading of the proceeding stage. Figure1.5.1 shows the circuit symbol of an op-amp.

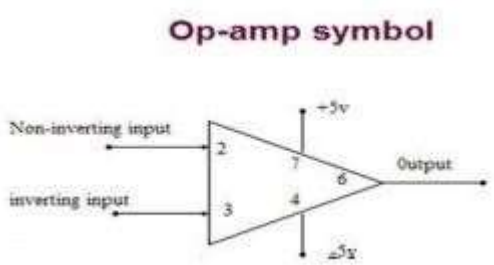

Figure 1.5.1 Op-amp circuit

[source: https://www.brainkart.com/subject/Linear-Integrated-Circuits_220/]

IDEAL OP-AMP CHARACTERISTICS

- Infinite voltage gain A.
- Infinite input resistance R_i, so that almost any signal source can drive it and there is no loading of the proceeding stage.
- Zero output resistance Ro, so that the output can drive an infinite number of other devices.
- Zero output voltage, when input voltage is zero.
- Infinite bandwidth, so that any frequency signals from o to ∞ HZ can be amplified without attenuation.
- Infinite common mode rejection ratio, so that the output common mode noise voltage is zero.

- Infinite slew rate, so that output voltage changes occur simultaneously with input voltage changes.

GENERAL OPERATIONAL AMPLIFIER STAGES AND INTERNAL CIRCUIT DIAGRAMS OF IC 741

An operational amplifier generally consists of three stages, namely

1. A differential amplifier
2. Additional amplifier stages to provide the required voltage gain and dc level shifting.
3. An emitter-follower or source follower output stage to provide current gain and low output resistance.

A low-frequency or dc gain of approximately 104 is desired for a general purpose op-amp and hence, the use of active load is preferred in the internal circuitry of op-amp.The output voltage is required to be at ground, when the differential input voltages are zero, and this necessitates the use of dual polarity supply voltage. Since the output resistance of op-amp is required to be low, a complementary push-pull emitter – follower or source follower output stage is employed. Figure 1.5.2. Shows the Stages of general Operational Amplifier and internal circuit diagrams of IC 741. Moreover, as the input bias currents are to be very small of the order of pico amperes, an FET input stage is normally preferred.

INPUT STAGE

The input differential amplifier stage uses p-channel JFETs M_1 and M_2. It employs a three-transistor active load formed by Q_3, Q_4, and Q_5. The bias current for the stage is provided by a two-transistor current source using PNP transistors Q_6 and Q_7. Resistor R_1increases the output resistance seen looking into the collector of Q_4 as indicated by R_{04}. This is necessary to provide bias current stability against the transistor parameter variations. Resistor R_2 establishes a definite bias current through Q_5. A single ended output is taken out at the collector of Q_4. MOSFET's are used in place of JFETs with

additional devices in the circuit to prevent any damage for the gate oxide due to electrostatic discharges.

GAIN STAGE

The second stage or the gain stage uses Darlington transistor pair formed by Q_8 and Q_9as shown in figure 1.5.2. The transistor Q8 is connected as an emitter follower, providing large input resistance. Therefore, it minimizes the loading effect on the input differential amplifier stage. The transistor Q_9 provides an additional gain and Q_{10} acts as an active load for this stage. The current mirror formed by Q_7 and Q_{10} establishes the bias current for Q_9. The VBE drop across Q_9 and drop across R_5 constitute the voltage drop across R_4, and this voltage sets the current through Q_8. It can be set to a small value, such that the base current of Q_8 also is very less.

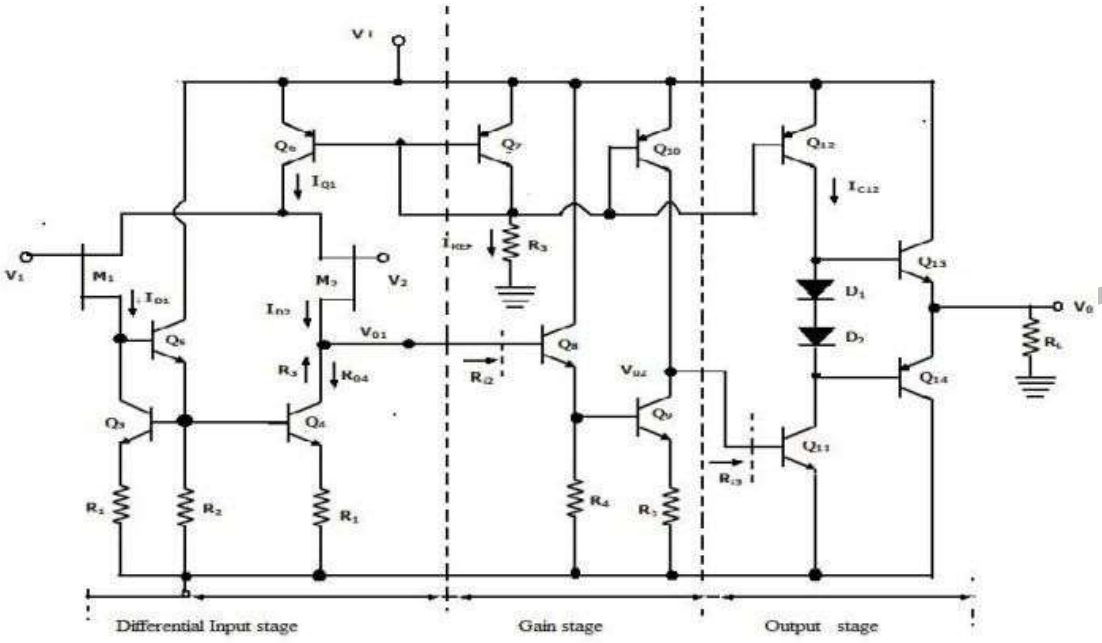

Figure 1.5.2. Stages of general Operational Amplifier and internal circuit diagrams of IC 741

[source: https://www.brainkart.com/subject/Linear-Integrated-Circuits_220/]

OUTPUT STAGE

The final stage of the op-amp is a class AB complementary push-pull output stage. Q_{11} is an emitter follower, providing a large input resistance for minimizing the loading effects on the gain stage. Bias current for Q_{11} is provided by the current mirror formed

by $Q_7$and Q_{12}, through Q_{13} and Q_{14} for minimizing the cross over distortion. Transistors can also be used in place of the two diodes.

The overall voltage gain AV of the op-amp is the product of voltage gain of each stage as given by

$$A_V=|A_d|\ |A_2||A_3|$$

Where A_d is the gain of the differential amplifier stage, A_2 is the gain of the second gain stage and A_3 is the gain of the output stage.

IC 741 BIPOLAR OPERATIONAL AMPLIFIER INTERNAL CIRCUIT DIAGRAM

The IC 741 produced since 1966 by several manufactures is a widely used general purpose operational amplifier. Figure 1.5.2 shows that equivalent circuit of the 741 op-amp, divided into various individual stages. The op-amp circuit consists of three stages.

1. The input differential amplifier
2. The gain stage
3. the output stage.

A bias circuit is used to establish the bias current for whole of the circuit in the I_C. The op-amp is supplied with positive and negative supply voltages of value ± 15V and the supply voltages as low as ±5V can also be used.

BIAS CIRCUIT

The reference bias current IREF for the 741 circuit is established by the bias circuit consisting of two diodes-connected transistors Q_{11} and Q_{12} and resistor R_5. The Widlar current source formed by Q_{11}, Q_{10} and R_4 provide bias current for the differential amplifier stage at the collector of Q_{10}. Transistors Q_8 and Q_9 form another current mirror providing bias current for the differential amplifier. The reference bias current IREF also provides mirrored and proportional current at the collector of the double –collector lateral PNP transistor Q_{13}. The transistor Q_{13} and Q_{12} thus form a two-output current mirror with Q_{13}A providing bias current for output stage and Q13B providing bias current for Q_{17}. The transistor Q_{18} and Q_{19} provide dc bias for the output stage. Formed by Q_{14} and

Q_{20} and they establish two VBE drops of potential difference between the bases of Q_{14} and Q_{18}.

INPUT STAGE

The input differential amplifier stage consists of transistors Q_1 through Q_7 with biasing provided by Q_8 through Q_{12}. The transistor Q_1 and Q_2 form emitter – followers contributing to high differential input resistance, and whose output currents are inputs to the common base amplifier using Q_3 and Q_4 which offers a large voltage gain. The transistors Q_5, Q_6 and Q_7 along with resistors R_1, R_2 and R_3 from the active load for input stage. The single-ended output is available at the collector of Q6. The two null terminals in the input stage facilitate the null adjustment. The lateral PNP transistors Q3 and Q4 provide additional protection against voltage breakdown conditions. The emitter-base junction Q3 and Q4 have higher emitter-base breakdown voltages of about 50V. Therefore, placing PNP transistors in series with NPN transistors provide protection against accidental shorting of supply to the input terminals.

GAIN STAGE

The Second or the gain stage consists of transistors Q_{16} and Q_{17}, with Q_{16} acting as an emitter – follower for achieving high input resistance. The transistor Q_{17} operates in common emitter configuration with its collector voltage applied as input to the output stage. Level shifting is done for this signal at this stage.

Internal compensation through Miller compensation technique is achieved using the feedback capacitor C_1 connected between the output and input terminals of the gain stage.

OUTPUT STAGE

The output stage is a class AB circuit consisting of complementary emitter follower transistor pair Q_{14} and Q_{20}. Hence, they provide an effective loss output resistance and current gain. The output of the gain stage is connected at the base of Q_{22}, which is connected as an emitter follower providing a very high input resistance, and it offers no appreciable loading effect on the gain stage. It is biased by transistor Q_{13} which also drives Q18 and Q19, that are used for establishing a quiescent bias current in the output transistors Q_{14} and Q_{20}.

1.4 DIFFERENTIAL AMPLIFIER

The function of a differential amplifier is to amplify the difference between two signals. The need for differential amplifier arises in many physical measurements where response from DC too many MHz of frequency is required. This forms the basic input stage of an integrated amplifier.

The basic differential amplifier has the following important properties of

- Excellent stability
- High versatility and
- High immunity to interference signals

The differential amplifier as a building block of the op-amp has the advantages of

- Lower cost
- Easier fabrication as IC component and
- closely matched components.

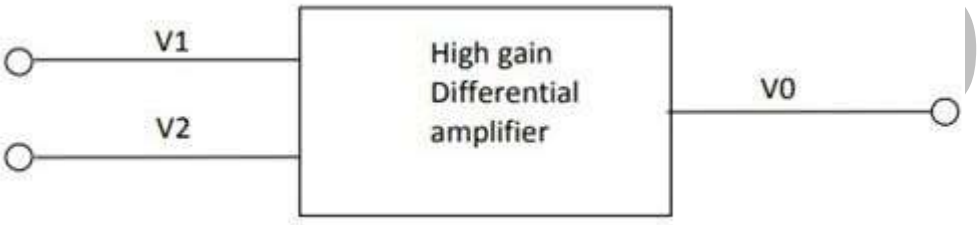

Figure1.4.1.Block diagram of differential Amplifier

[source: https://www.brainkart.com/subject/Linear-Integrated-Circuits_220/]

The above figure1.4.1 shows the basic block diagram of a differential amplifier, with two input terminals and one output terminal. The output signal of the differential amplifier is proportional to the difference between the two input signals.

$$V_0 = A_{dm} (V_1 – V_2)$$

If $V_1 = V_2$, then the output voltage is zero. A non-zero output voltage V0 is obtained when V_1 and V_2 are not equal. The difference mode input voltage is defined as $V_m = V_1 – V_2$ and the common mode input voltage is defined as

$$V_{CM}=\frac{V1+V2}{2}$$

These equation show that if $V_1 = V_2$, then the differential mode input signal is zero and common mode input signal is $V_{cm} = V_1 = V_2$.

DIFFERENTIAL AMPLIFIER WITH ACTIVE LOAD

Differential amplifier is designed with active loads to increase the differential mode voltage gain. The open circuit voltage gain of an op-amp is needed to be as large as possible. This is got by cascading the gain stages which increase the phase shift and the amplifier also becomes vulnerable to oscillations. The gain can be increased by using large values of collector resistance. For such a circuit, the voltage gain is given by

$$A_{dm} = g_m RC$$

To increase the gain the IC RC product must be made very large. However, there are limitations in IC fabrication such as,

1. A large value of resistance needs a large chip area.
2. For large RC, the quiescent drop across the resistor increase and a large power supply will be required to maintain a given operating current.
3. Large monolithic resistor introduces large parasitic capacitances which limits the frequency response of the amplifier.
4. for linear operation of the differential pair, the devices should not be allowed to enter into saturation.

This limits the max input voltage that can be applied to the bases of transistors Q_1 and Q_2 the base-collector junction must be allowed to become forward-biased by more than 0.5V. The large value of load resistance produces a large dc voltage drop $(I_{EE} / 2) R_C$, so that the collector voltage will be V_C=Vcc - (IEE/2) RC and it will be substantially less than the supply voltage Vcc. This will reduce the input voltage range of the differential amplifier. Due to the reasons cited above, an active load is preferred in the differential amplifier configurations.

BJT DIFFERENTIAL AMPLIFIER USING ACTIVE LOADS

A simple active load circuit for a differential amplifier is the current mirror active load as shown in figure. The active load comprises of transistors Q_3 and Q_4 with the transistor Q_3 connected as a Diode with its base and collector shorted. The circuit is shown to drive a load RL. When an ac input voltage is applied to the differential amplifier, the various currents of the circuit are given by

$$I_{C4} = I_{C3} = I_{C1} = g_m V_{id}/2$$

where $I_{C4} = I_{C3}$ due to current mirror action.

$$I_{C2} = - g_m V_{id}/2 .$$

We know that the load current IL entering the next stage is

$$I_L = I_{C2} - I_{C4} = - g_m V_{id}/2 - g_m V_{id}/2 = - g_m V_{id}$$

Then, the output voltage from the differential= amplifier= is given by

$$V_0 = - I_L R_L = g_m R_L V_{id}.$$

The ac voltage gain of the circuit is given by

$$A_v = v_0/v_{id} = g_m R_L.$$

The amplifier can amplify the differential input signals and it provides single-ended output with a ground reference since the load R_L is connected to only one output terminal. This is made possible by the use of the current mirror active load. Figure1.4.2 shown below is the BJT Differential Amplifier with current mirror active load. The output resistance R0 of the circuit is that offered by the parallel combination of transistors Q_2 (NPN) and Q_4(PNP). It is given by $R_r = r_{02} \parallel r_{04}$.

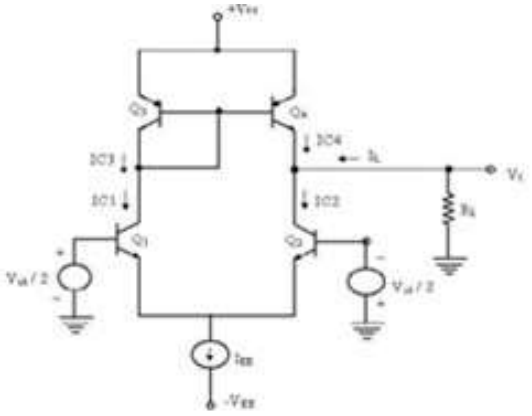

Figure 1.4.2.BJT Differential Amplifier with current mirror active load

[source: https://www.brainkart.com/subject/Linear-Integrated-Circuits_220/]

ANALYSIS OF BJT DIFFERENTIAL AMPLIFIER WITH ACTIVE LOAD

The collector currents of all the transistors are equal.

$$I_{C1} = I_{C2} = I_{C3} = I_{C4} = I_{EE}/2 .$$

The Collector -emitter voltages of Q_1 and Q_2 are given by

$$V_{CE1}\text{-}V_{CE2} = V_C\text{-}V_E = V_{CC} - V_{EB}\text{-}(-V_{EB}) = V_{CC}$$

Eqn. shows that, the offset is higher than that of a resistive loaded differential amplifier A. This can be reduced by the use of emitter resistors for Q_3 and Q_4 , and a transistor Q_5in the current mirror load.

CMRR OF THE DIFFERENTIAL AMPLIFIER USING ACTIVE LOAD

The differential amplifier using active load provides high voltage gain to the differential input signal and a single – ended output that is referenced to the ground is obtained. The differential amplifier which provides conversion for a differential signal to a single ended signal is necessary in differential input signal ended output amplifiers. The op-amp is one such circuit. The changes in the common-mode signal of the bias current source. This induces a change in I_{C2} and an identical change in I_{C1}. The change in I_{C1}will then produce a change in the PNP load devices, and thereby a change in I_{C4}, which is the collector current Q_4, The current I_{C4} is in such a direction as to cancel the change in I_{C2}. As a result of this, any common mode input does not cause a change in output.

The voltage gain of the differential amplifier is independent of the quiescent current I_{EE}. This makes it possible to use very small value of I_{EE} as low as 20μA, while still maintaining a large voltage gain. Small value of I_{EE} is preferred, since it results in a small value of bias current and a large value for the input resistance. A limitation in choosing a small I_{EE} is, however, the fact that, it will result in a poor frequency response of the amplifier. Improved differential circuit using active load is shown in figure1.4.3.

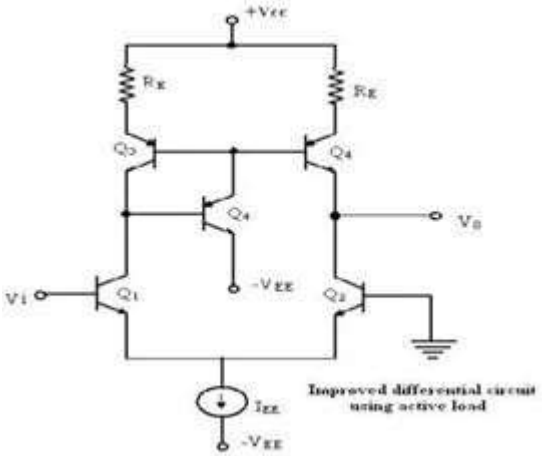

Figure1.4.3 Improved differential circuit using active load

[source: https://www.brainkart.com/subject/Linear-Integrated-Circuits_220/]

When a small value of bias current is required, the best approach is to use a JFET or MOSFET differential amplifier that is operated at comparatively higher values of I_{EE}.figure1.4.4 shown below is the differential to single ended conversion and output stage.

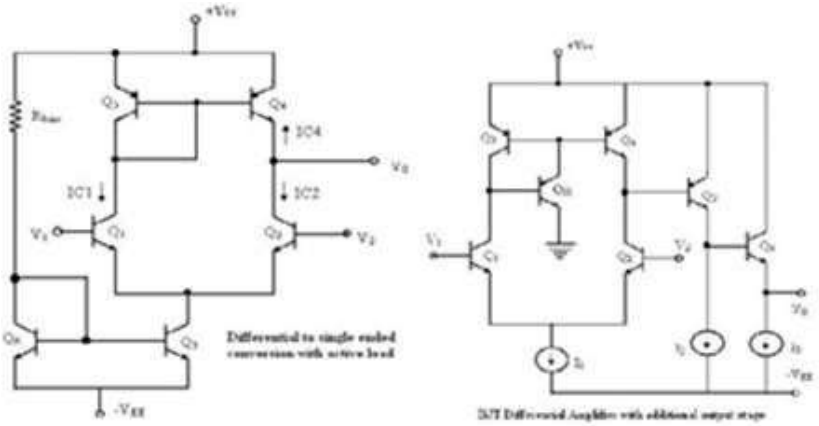

Figure1.4.4 Differential to single ended conversion and output stage.

[source: https://www.brainkart.com/subject/Linear-Integrated-Circuits_220/]

DIFFERENTIAL MODE SIGNAL ANALYSIS

The ac analysis of the differential amplifier can be made using the circuit model as shown below. The differential input transistor pair produces equal and opposite currents whose amplitude us given by gm2 V_{id} /2 at the collector of Q_1 and Q_2. The collector current I_{c1} is fed by the transistor Q_3 and it is mirrored at the output of Q_4. Therefore, the total current i_0 flowing through the load resistor R_L is given by

$$i_0 = [2g_{m2}V_{id}]/2 = g_{m2}V_{id}.$$

Then the output voltage is

$$v_0 = i_0R_L - g_{m2}R_LV_{id}$$

and the differential mode gain Ad of the differential amplifier is

$$A_{dm} = \frac{v_0}{v_{dm}} = g_{m2}R_L$$

This current mirror provides a single ended output which has a voltage equal to the maximum gain of the common emitter amplifier. The power of the current mirror can be increased by including additional common collector stages at the o/p of the differential input stage. A bipolar differential amplifier structure with additional stages is shown in figure1.4.5. The resistance at the output of the differential stage is now given by the parallel combination of transistors Q_2 and Q_4 and the input resistance is offered by Q_5. Then, the equivalent resistance is expressed by $R_{eq} = r_{o2} \parallel r_{04} \parallel r_{i5} = r_{i5}$.

The gain of the differential stage then becomes

$$Adm = g_{m2} R_{eq} = g_{m2} r_{i5} = \beta I_{C2}/I_{C5} .$$

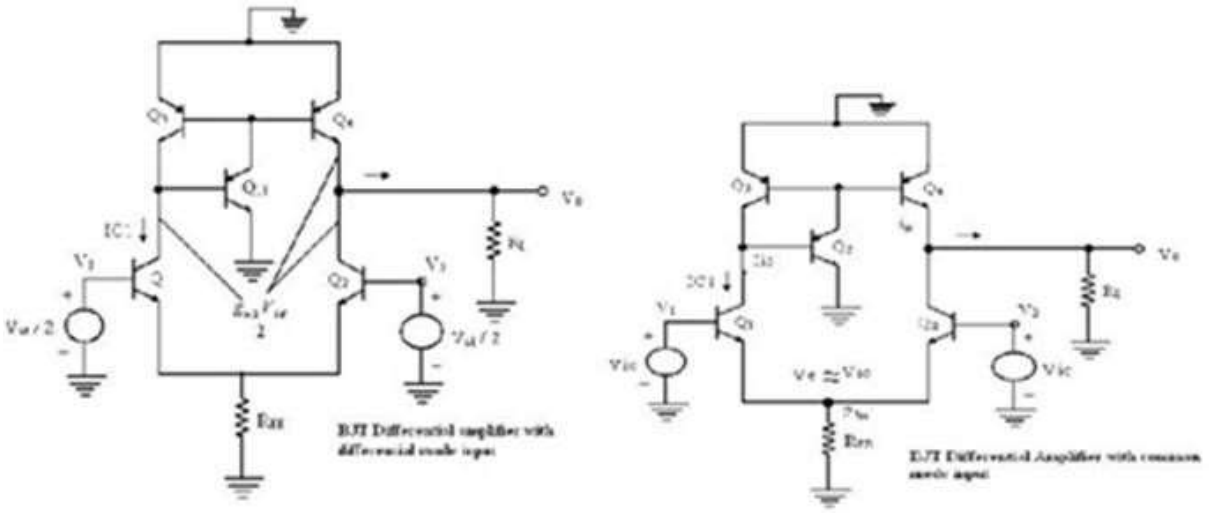

Figure1.4.5. Differential amplifier with differential mode input and common mode input.

[source: https://www.brainkart.com/subject/Linear-Integrated-Circuits_220/]

1.1 CONSTANT CURRENT SOURCE (CURRENT MIRROR)

A constant current source makes use of the fact that for a transistor in the active mode of operation, the collector current is relatively independent of the collector voltage. In the basic BJT Current mirror circuit shown in figure 1.1.1 and Volt-ampere characteristics for transistor Q_2 as in figure.1.1.2

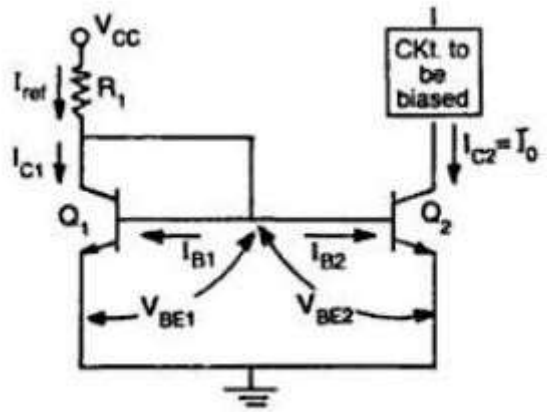

Figure 1.1.1 BJT Current mirror circuit

[source:"Linear Integrated Circuits"by D.Roy Choudhry, Shail Bala Jain, Page-70]

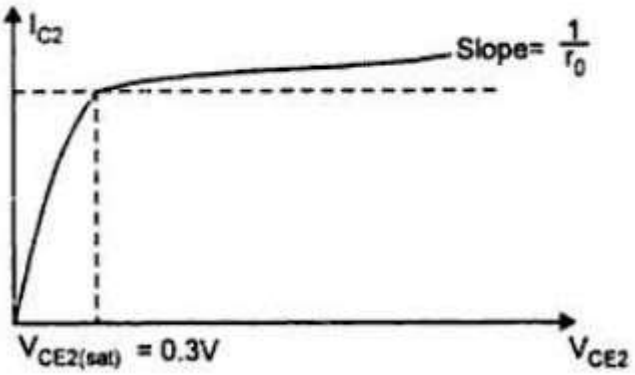

Figure1.1.2 Volt-ampere characteristics for transistor Q_2

[source:"Linear Integrated Circuits"by D.Roy Choudhry, Shail Bala Jain, Page-71]

Transistors Q_1&Q_2 are matched as the circuit is fabricated using IC technology. Base and emitter of Q_1& Q_2 are tied together and thus have the same VBE. In addition, transistor Q_1 is connected as a diode by shorting its collector to base. The input current I_{ref} flows through the diode connected transistor Q_1 and thus establishes a voltage across Q_1. This voltage in turn appears between the base and emitter of Q_2 .Since Q_2 is identical

to Q_1, the emitter current of Q_2 will be equal to emitter current of Q_1 which is approximately equal to I_{ref}. As long as Q_2 is maintained in the active region ,its collector current $I_{C2}=I_o$ will be approximately equal to I_{ref} . Since the output current Io is a reflection or mirror of the reference current I_{ref}, the circuit is often referred to as a current mirror.

Analysis:

The collector current I_{C1} and I_{C2} for the transistor Q_1 and Q_2 can be approximately expressed as

$$I_{C1(t)=\alpha}\, I_{ESe}{}^{V_{BE1}/V_T} \text{ ---------- (1)}$$

$$I_{C2(t)=\alpha}\, I_{ESe}{}^{V_{BE2}/V_T} \text{ ---------- (2)}$$

Where I_{ES} is reverse saturation current in emitter junction and VT is temperature equivalent of voltage.

From equation (1) & (2)

Since $V_{BE1}=V_{BE2}$ we obtain $I_{C2}=I_{C1}=I\backslash_C=I_O$

Also since both the transistors are identical, $I_{C1}= I_{C2}$

KCL at the collector of Q_1 gives

$I_{ref}= I_{C1}+I_{B1}+I_{B2}$

$$I_{ref} = I_{C1}+I_{B1}+I_{B2}$$

$$= I_{C1} + \frac{I_{C1}}{\beta} + \frac{I_{C2}}{\beta} = I_{C1} + 2\frac{I_{C1}}{\beta} \quad \text{When } I_{C1} = I_{C2} = I_C = I_o \text{ ---------- (4)}$$

Solving Eq (4)

$$I_{ref}=(V_{CC} - V_{BE(ON)})/R$$

$$I_{ref}=I_{C1} + 2\frac{I_{C1}}{\beta} = I_{C1}\left(1 + \frac{2}{\beta}\right)$$

$$I_C = I_{C1} \approx I_{C2} = \frac{I_{ref}}{1+\frac{2}{\beta}} = \frac{\beta}{\beta+2}(V_{CC} - V_{BE(ON)})/R \text{ ---------- (5)}$$

$$I_0 = I_{ref}$$

From Eq.5 for β/ [β +1] >>1, is almost unity and the output current I0 is equal to the reference current, ref which for a given R_1 is constant. Typically I_o varies by about 3% for $50 \leq \beta \leq 200$.

The circuit however operates as a constant current source as long as Q_2 remains in the active region.

WIDLAR CURRENT SOURCE

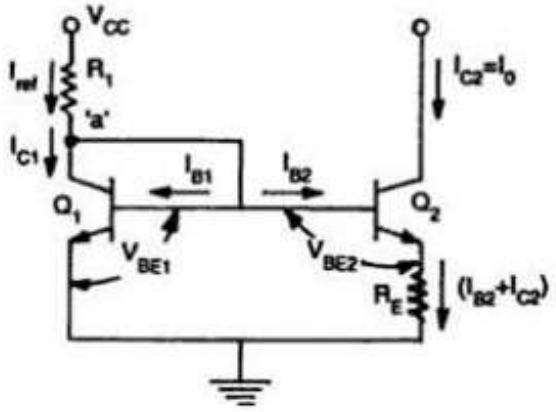

Figure 1.1.3 Widlar current source

[source:"Linear Integrated Circuits"by D.Roy Choudhry, Shail Bala Jain, Page-72]

Widlar current source which is particularly suitable for low value of currents. To overcome the limitations of constant current source connect R_E to the emitter terminal of Q_2.Figure 1.1.3.shows the wildar current source.The circuit differs from the basic current mirror only in the resistance R_E that is included in the emitter lead of Q_2. It can be seen that due to R_E the base-emitter voltage V_{BE2} is less than VBE1 and consequently current Io is smaller than I_{C1}

The ratio of collector currents I_{C1}&I_{C2} using

$$\frac{I_{C1}}{I_{C2}} = e^{\frac{V_{BE1}-V_{BE2}}{V_T}} - \quad (1)$$

Taking natural logarithm of both sides, we get

$$V_{BE1} - V_{BE2} = V_T \ln \frac{I_{C1}}{I_{C2}} \quad \text{----- (2)}$$

Writing KVL for the emitter base loop

$$V_{BE1}=V_{BE2}+(I_{B2}+I_{C2})R_E \quad \text{----------(3)}$$

Or $$V_{BE1}-V_{BE2}=(1/\beta +1)I_{C2}R_E \quad \text{----------(4)}$$

From eqn. (2) & (4) we obtain

$$V_T \ln \frac{I_{C1}}{I_{C2}} = (1/\beta +1)\, I_{C2}R_E \quad \text{---------- (5)}$$

A relation between I_{C1} and the reference current I_{ref} is obtained by writing KCL at the collector point of Q1

$$I_{ref} = I_{C1} + I_{B1} + I_{B2}$$

$$I_{ref} = I_{C1} + I_{C1}/\beta + I_{C2}/\beta$$

Neglecting I_{C2}/β,

$$I_{ref} = I_{C1}\,(1 + 1/\beta)$$

$$I_{ref} = [\ Vcc - V_{BE}\ ]\ /R_1$$

When $\beta >> 1$, $I_{C1} = I_{ref}$

WILSON CURRENT SOURCE

The Wilson current source shown in figure 1.1.4

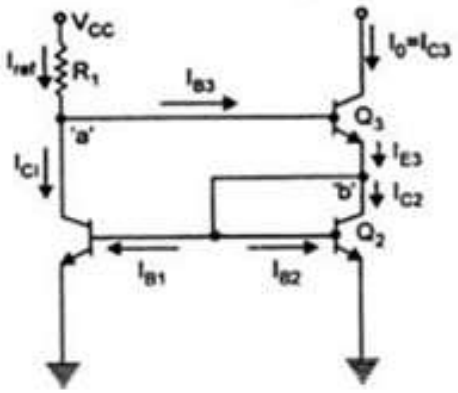

Figure 1.1.4.Wilson current source

[source:"Linear Integrated Circuits"by D.Roy Choudhry, Shail Bala Jain, Page-77]

It provides an output current I_0 which is very nearly equal to V_{ref} and also exhibits a very high output resistance.

Analysis

Since $V_{BE1}=V_{BE2}$

$I_{C1}=I_{C2}$ and $I_{B1}=I_{B2}=I_B$

At node 'b'

$I_{E3}=2I_B+I_{C2}=(\frac{2}{\beta}+1)I_{C2}$ ---------- (1)

I_{E3} is equal to

$I_{E3}=I_{C3}+I_{B3}=I_{C3}(1+1/\beta)$ ---------- (2)

From (1) and (2)

$I_{C3}(1+1/\beta)=I_{C2}(1+2/\beta)$

From Eqn. (1) & (2) we obtain

$I_{C3}=I_o=I_{C2}(\beta\ 2)/(\beta+1)=I_{C1}(\beta\ 2)/(\beta+1)$ Since $I_{C1}=I_{C2}$

At node 'a' $I_{ref}=I_{C1}+I_{B3}=\frac{\beta+1}{\beta+2}I_o+\frac{I_o}{\beta}=$

$I_{ref}=\frac{\beta^2+2\beta+2}{\beta^2+2\beta}I_o$ and $I_{ref}=\frac{V_{cc}-2V_{BE}}{R_1}$; $I_o-I_{ref}=\frac{2}{\beta^2+2\beta+2}$ I ref is very small for modest β.

But output resistance is greater than Widlar source.

But output resistance is greater than Widlar source.

CURRENT SOURCES AS ACTIVE LOADS

The current source can be used as an active load in both analog and digital IC's. The active load realized using current source in place of the passive load (i.e. a resistor) in the collector arm of differential amplifier makes it possible to achieve high voltage gain without requiring large power supply voltage. The active load so achieved is basically R0 of a PNP transistor.

1.6 DC CHARACTERISTICS OF OP-AMP

Current is taken from the source into the op-amp inputs respond differently to current and voltage due to mismatch in transistor.

DC output voltages are,

- Input bias current
- Input offset current
- Input offset voltage
- Thermal drift

INPUT BIAS CURRENT

The op-amp's input is differential amplifier, which may be made of BJT or FET.In an ideal op-amp, we assumed that no current is drawn from the input terminals the base currents entering into the inverting and non-inverting terminals (I_{B^-} & I_{B^+} respectively).Even though both the transistors are identical, I_B^- and I_B^+ are not exactly equal due to internal imbalance between the two inputs. Input bias current and Inverting amplifier with bias currents is shown in figure 1.6.1. Manufacturers specify the input bias current I_B

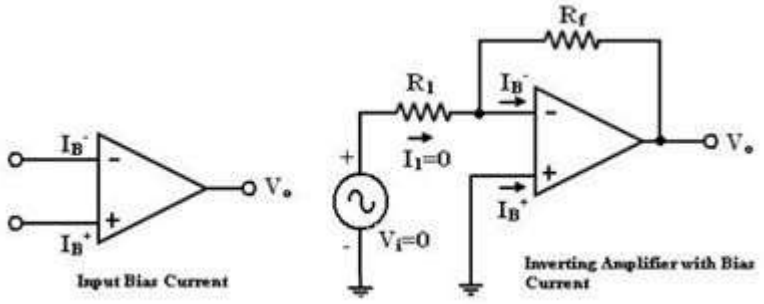

Figure 1.6.1 a) input bias current b) Inverting amplifier with bias currents

[source:"Linear Integrated Circuits"by D.Roy Choudhry, Shail Bala Jain, Page-118]

$$I_B = \frac{I_B^+ + I_B^-}{2}$$

If input voltage V_i = 0V. The output Voltage Vo should also be (V_o = 0) but for I_B = 500nA We find that the output voltage is offset by Op-amp with a 1M feedback resistor

Vo = 500nA X 1M = 500mV

The output is driven to 500mV with zero input, because of the bias currents.

In application where the signal levels are measured in mV, this is totally unacceptable. This can be compensated by a compensation resistor R_{comp} has been added between the non-inverting input terminal and ground as shown in the figure 1.6.2 below.

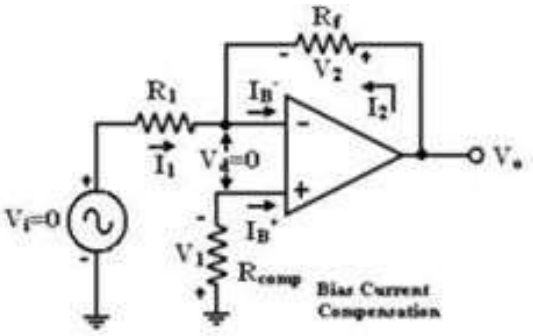

Figure 1.6.2 Bias compensated circuit in non-inverting amplifier

[source:"Linear Integrated Circuits"by D.Roy Choudhry, Shail Bala Jain, Page-119]

Current I_B^+ flowing through the compensating resistor R_{comp}, then by KVL we get,

$$- V_1+0+V_2-V_o = 0 \text{ (or)}$$

$$V_o = V_2 - V_1 \text{ ---------- (1)}$$

By selecting proper value of R_{comp}, V_2 can be cancelled with V_1 and the V_o = 0. The value of Rcomp is derived as

$$V_1 = I_B^+ R_{comp} \quad \text{(or)}$$

$$I_B^+ = V_1/R_{comp} \text{ - - - - - - - - - - - - - - - - (2)}$$

The node 'a' is at voltage ($-V_1$). Because the voltage at the non-inverting input terminal is ($-V_1$).

So with V_i = 0 we get,

$$I_1 = V_1/R_1 \quad (3)$$

$$I_2 = V_2/R_f \quad (4)$$

For compensation, V_o should equal to zero ($V_o = 0$, $V_i = 0$). i.e. from equation (3) $V_2 = V_1$. So that,

$$I_2 = V_1/R_f \longrightarrow (5)$$

KCL at node 'a' gives,

$$I_B^- = I_2 + I_1 = (V_1/R_f) + (V_1/R_1) = V_1(R_1+R_f)/R_1R_f \quad \text{----------} \quad (5)$$

Assume $I_B^- = I_B^+$ and using equation (2) & (5) we get

$$V_1 (R_1+R_f)/R_1R_f = V_1/R_{comp}$$

$$R_{comp} = R_1 \,||\, R_f \quad \text{----------} \quad (6)$$

i.e. to compensate for bias current, the compensating resistor, Rcomp should be equal to the parallel combination of resistor R_1 and R_f.

INPUT OFFSET CURRENT

i. Bias current compensation will work if both bias currents I_B^+ and I_B^- are equal.

ii. Since the input transistor cannot be made identical. There will always be some small difference between I_B^+ and I_B^-. This difference is called the offset current

$$|Ios| = I_B^+ - I_B^- \quad (7)$$

Offset current I_{os} for BJT op-amp is 200nA and for FET op-amp is 10pA. Even with bias current compensation, offset current will produce an output voltage when $V_i = 0$.

$$V_1 = I_B^+ R_{comp} \quad \text{----------} \quad (11)$$

$$\text{And } I_1 = V_1/R_1 \quad \text{----------} \quad (12)$$

KCL at node a gives,

$$I_2 = (I_B^- - I_1) = I_B^- - (I_B^+ \frac{R_{comp}}{R_1})$$

Output voltage $V_o = R_f I_{OS}$

Again $V_0 = I_2 R_f - V_1$

$$Vo = I_2 R_f - I_B^+ R_{comp}$$

Vo = 1M Ω X 200nA

Vo = 200mV with $V_i = 0$

By using the above Equation the offset current can be minimized by keeping feedback resistance small.

- Unfortunately to obtain high input impedance, R1 must be kept large.
- R1 large, the feedback resistor Rf must also be high. So as to obtain reasonable gain.

The T-feedback network is a good solution. This will allow large feedback resistance, while keeping the resistance to ground low (in dotted line).

The T-network provides a feedback signal as if the network were a single feedback resistor.

By T to Π conversion,

$$R_f = \frac{R_t^2 + 2R_tR_s}{R_s}$$

To design T- network first pick Rt<<Rf/2 and=calculate

$$R_s \approx \frac{R_t^2}{R_f - 2R_t}$$

INPUT OFFSET VOLTAGE

In spite of the use of the above compensating techniques, it is found that the output voltage may still not be zero with zero input voltage [Vo ≠ 0 with Vi= 0]. This is due to unavoidable imbalances inside the op-amp and one may have to apply a small voltage at the input terminal to make output (Vo) = 0.figure 1.6.3 a) shown below is the op-amp showing input offset voltage.This voltage is called input offset voltage Vos. This is the voltage required to be applied at the input for making output voltage to zero (Vo = 0).

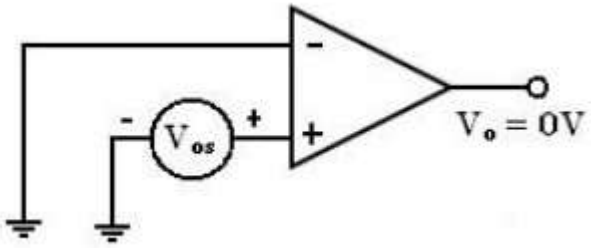

Figure 1.6.3 a)op-amp showing input offset voltage

[source:"Linear Integrated Circuits"by D.Roy Choudhry, Shail Bala Jain, Page-121]

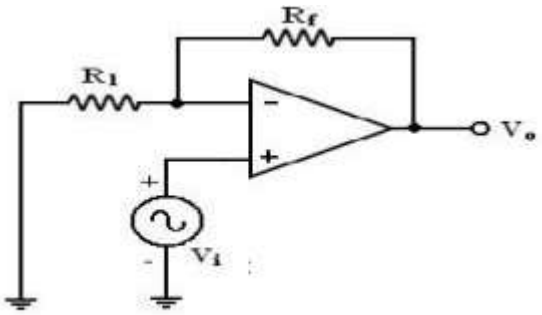

Figure 1.6.3 b)Non-inverting Amplifier

[source:"Linear Integrated Circuits"by D.Roy Choudhry, Shail Bala Jain, Page-122]

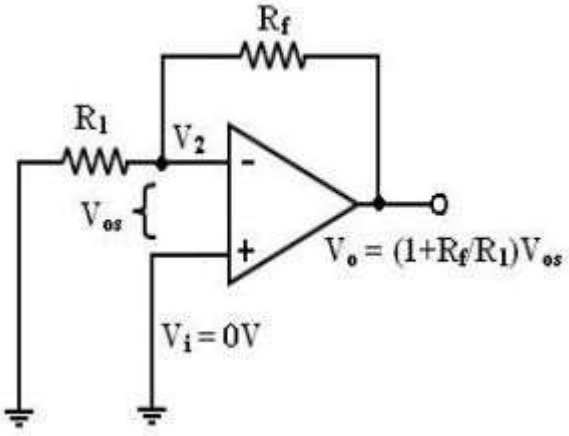

Figure 3c) Inverting Amplifier

[source:"Linear Integrated Circuits"by D.Roy Choudhry, Shail Bala Jain, Page-122]

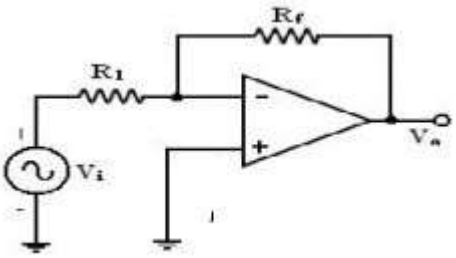

Figure 1.6.3 d) Equivalent circuit for Vi=0

[source:"Linear Integrated Circuits"by D.Roy Choudhry, Shail Bala Jain, Page-122]

Let us determine the Vos on the output of inverting and non-inverting amplifier. If V_i = 0 (Figure 1.6.3(b) and1.6.3 (c)) become the same as in figure1.6.3(d).

TOTAL OUTPUT OFFSET VOLTAGE

The total output offset voltage V_{OT} could be either more or less than the offset voltage produced at the output due to input bias current (I_B) or input offset voltage alone(V_{os}). This is because IB and Vos could be either positive or negative with respect to ground. Therefore the maximum offset voltage at the output of an inverting and non-inverting amplifier (figure 1.6.3 b, c) without any compensation technique used is given by many op amps provide offset compensation pins to nullify the offset voltage. A 10K potentiometer is placed across offset null pins 1&5. The wipes connected to the negative supply at pin 4. The position of the wipes is adjusted to nullify the offset voltage. Compensation circuit for offset voltage is shown in figure 1.6.4.

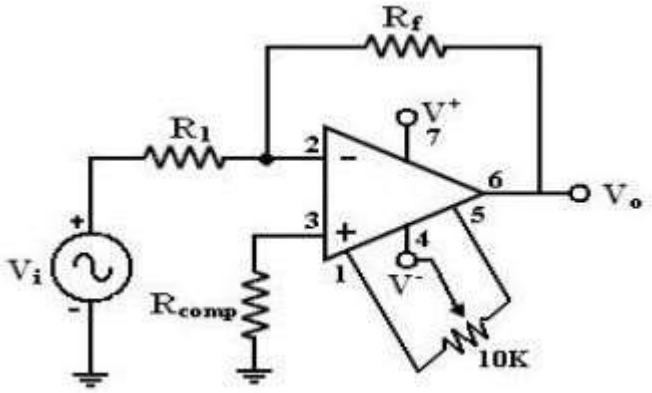

Figure 1.6.4. compensation circuit for offset voltage

[source:"Linear Integrated Circuits"by D.Roy Choudhry, Shail Bala Jain, Page-123]

When the given (below) op-amps does not have these offset null pins, external balancing techniques are used.

$$V_{OT} = \left(1 + \frac{R_f}{R_1}\right) V_{OS} + R_f I_B$$

With Rcomp, the total output offset

$$V_{OT} = \left(1 + \frac{R_f}{R_1}\right) V_{OS} + R_f I_{OS}$$

THERMAL DRIFT

Bias current, offset current, and offset voltage change with temperature. A circuit carefully nulled at 25ºC may not remain. So when the temperature rises to 35ºC. This is called drift. Offset current drift is expressed in nA/ºC. These indicate the change in offset for each degree Celsius change in temperature.

1.9 JFET OPERATIONAL AMPLIFIER

LF155 JFET OP-AMP

The input impedance of the op-amp increased by using JFET differential amplifier as its input stage**.** It is the first monolithic JFET which uses well matched high voltage JFETs on the same chip with standard bipolar transistors. It has offset adjust feature due to which drifts and CMRR do not degrade.

FEATURES

- Guaranteed Offset Voltage Drift on All Grades.
- Guaranteed Slew Rate on All Grades.
- Guaranteed Low Input Offset Current 10pA Max.
- Guaranteed Low Input Bias Current 50pA Max.
- Guaranteed High Slew Rate (156A/356A) 10V/µs Min.
- Fast Settling to 0.01% 1.5µS.

INTERNAL SCHEMATIC

Figure 1.9.1 and Figure1.9.2 shown the schematic diagram and pin diagram of LF155

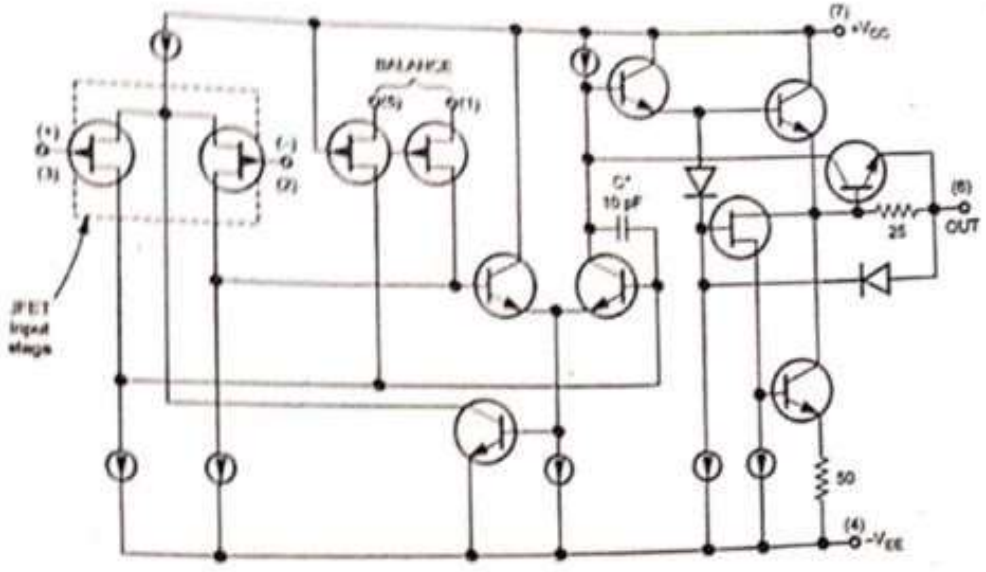

Figure 1.9.1 Schematic Diagram of LF155

[source: "Linear Integrated Circuits, by U.A.Bakshi, A.P.Godse, Page-S-27]

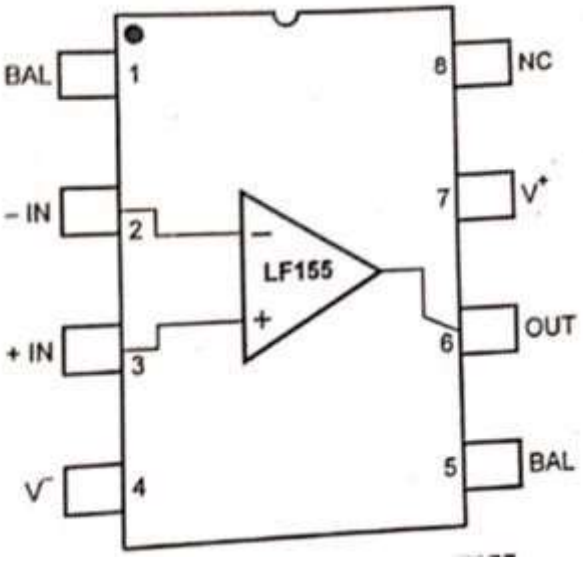

Figure1.9.2.Pin Diagram of LF155

[source: "Linear Integrated Circuits, by U.A.Bakshi, A.P.Godse, Page-S-27]

Applications:

- Precision high speed integrators
- Fast D/A and A/D converters
- High impedance buffers Wideband, low noise, low drift amplifiers
- Logarithmic amplifiers

TL082 JFET OP-AMP

The op-amp TL082 is low cost, high speed, dual JFET input op-amp with an internally trimmed input offset voltage.JFET has large reverse breakdown voltages from gate to source and drain hence clamping across the inputs is not required. This large differential input voltages can easily be accommodated without the need of large supply current.This op-amp requires low supply current and still maintain high slew rate and large gain bandwidth product. Due to JFET input stage, the input bias current and offset current is very low. Figure 1.9.3 and Figure 1.9.4 shows the pin diagram and internal schematic diagram of TL082.

FEATURES

- Internally Trimmed Offset Voltage: 15 mV
- Low Input Bias Current: 50 pA

- Low Input Noise Voltage: 16nV/√Hz
- Low Input Noise Current: 0.01 pA/√Hz
- Wide Gain Bandwidth: 4 MHz
- High Slew Rate: 13 V/μs
- Low Supply Current: 3.6 mA
- High Input Impedance: 1012Ω
- Low Total Harmonic Distortion: ≤0.02%
- Low 1/f Noise Corner: 50 Hz
- Fast Settling Time to 0.01%: 2 μs

INTERNAL SCHEMATIC

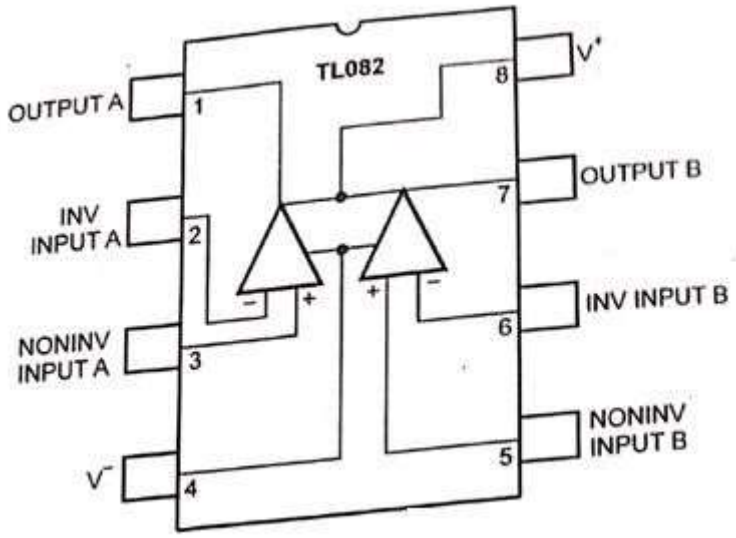

Figure 1.9.3 pin diagram of TL082

[source: "Linear Integrated Circuits, by U.A.Bakshi, A.P.Godse, Page-S-28]

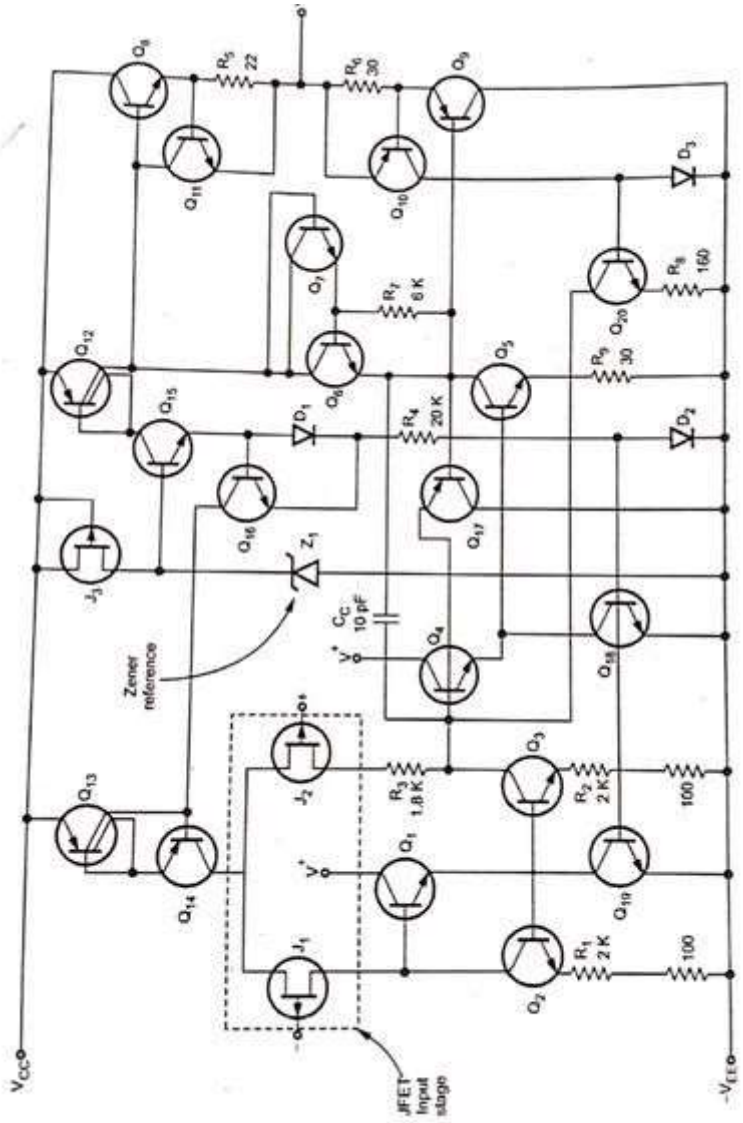

Figure 1.9.4 Internal Schematic of TL082

[source: "Linear Integrated Circuits, by U.A.Bakshi, A.P.Godse, Page-S-29]

1.8 OPEN LOOP CONFIGURATION OF OP AMP

Open Loop Configuration of Op amp – The simplest possible way to use an op-amp is in the open loop mode. Since the gain is very large in open loop condition the output voltage Vo is either at its positive saturation voltage +Vsat or –ive saturation voltage –Vsat as V1>V2 or V2>V1 Respectively.

The Figure 1.8.1 shows an op amp in the open loop condition.

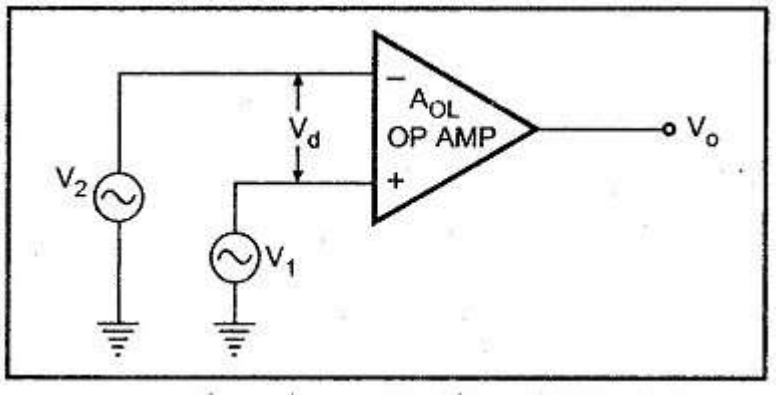

Figure 1.8.1Open loop operation of op-amp

[source: https://www.brainkart.com/subject/Linear-Integrated-Circuits_220/]

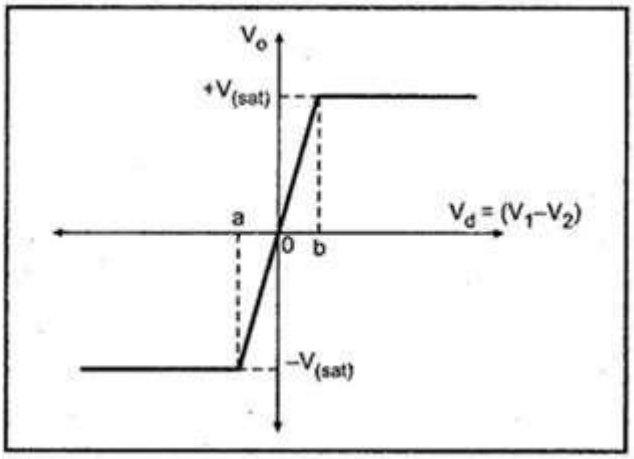

Figure1.7.2Voltage transfer characteristics

[source: https://www.brainkart.com/subject/Linear-Integrated-Circuits_220/]

For small range of input signal from point a to b it behaves linearly.This range is very small & practically due to high open loop gain op-amp either shows $+V_{sat}$ or $-V_{sat}$ level. This indicates the inability of op-amp to work as a linear small amplifier in the

open loop mode.Hence the op-amp is generally not used We know that the d.c. supply voltages applied to the op-amp are V_{cc} and $-V_{EE}$ and the output varies linearly only between V_{CC} and $-V_{EE}$.Since gain is very large in open loop condition, the output voltage V, is either at its positive saturation voltage ($+Vs_{at}$) or negative saturation voltage ($-V_{sat}$) as $V_1 > V2$ or $V2 > V_i$ respectively. This is shown in the Figure 1.8.2.Thus very small noise voltage present at the input also gets amplified due to its high open loop gain and op-amp gets saturated. It can be seen from the Fig.2 only for small range of input signal (from point a to b), it behaves linearly. This range is very small and practically due to high open loop gain, op-amp either shows + V_{sat} or – V_{sat} level.This indicates the inability of op-amp to work as a linear small signal amplifier in the open loop mode. Hence, the op-amp is generally not used in the open loop configuration. Such an open loop behavior of the op-amp finds some rare applications like voltage comparator, zero crossing detector etc.

CLOSED LOOP CONFIGURATION OF OP AMP

The utility of op-amp increases considerably if it is used in a closed loop mode. The Closed Loop Configuration of Op amp is possible using feedback. The feedback allows to feed some part of the output back to the input. In linear applications the op-amp is always used with negative feedback. The feedback helps to control gain which otherwise drives op-amp into saturation.

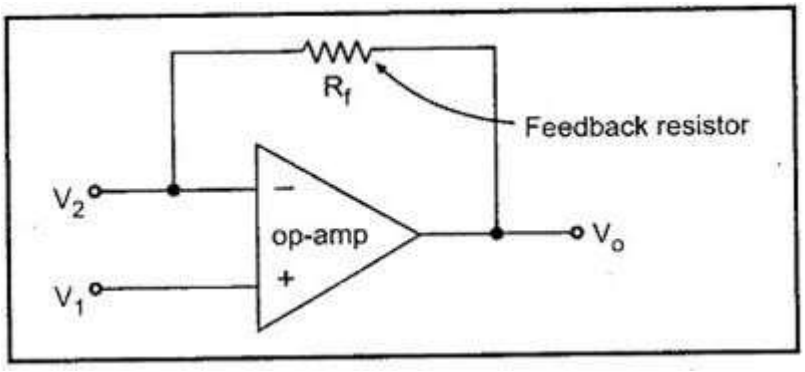

Figure 1.8.3 op-amp with negative feedback

[source: https://www.brainkart.com/subject/Linear-Integrated-Circuits_220/]

The negative feedback is possible by adding a resistor as shown figure1.8.3 Called **feedback resistor.** The feedback is said to be negative as the feedback resistor connects the output to the inverting input terminal.

The gain resulting with feedback is called **closed loop gain** of the op-amp. Due to feedback resistance there is reduction in the gain. The closed loop gain is much less than the open loop gain and is independent of it. Most of the linear circuits use op-amp in a closed loop mode with negative feedback with R_f. This is because, due to reduced gain, the output is not driven into the saturation and the circuit behaves in a linear manner.

1.3 VOLTAGE REFERENCES

The circuit that is primarily designed for providing a constant voltage independent of changes in temperature is called a voltage reference. The most important characteristic of a voltage reference is the temperature coefficient of the output= reference voltage Tc_R , and it is expressed as

$$T_{CR} = \frac{dV_R}{dT}$$

The desirable properties of a voltage reference are:

1. Reference voltage must be independent of any temperature change.
2. Reference voltage must have good power supply rejection which is as independent of the supply voltage as possible and
3. Output voltage must be as independent of the loading of output current as possible, or in other words, the circuit should have low output impedance.

The voltage reference circuit is used to bias the voltage source circuit, and the combination can be called as the voltage regulator. The basic design strategy is producing a zero T_{CR} at a given temperature, and thereby achieving good thermal ability. Temperature stability of the order of 100ppm/^{0} C is typically expected.

VOLTAGE REFERENCE CIRCUIT USING TEMPERATURE COMPENSATION SCHEME

The voltage reference circuit using basic temperature compensation scheme is shown in figure 1.3.1 below. This design utilizes the close thermal coupling achievable among the monolithic components and this technique compensates the known thermal drifts by introducing an opposing and compensating drift source of equal magnitude.

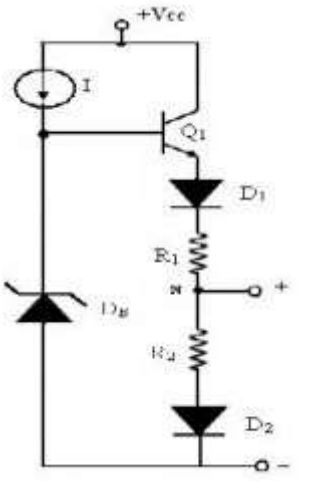

Figure 1.3.1.Voltage reference circuit using temperature compensation scheme

[source:"Linear Integrated Circuits"by S.Salivahanan& V.S. Kanchana Bhaskaran, Page-55]

A constant current I is supplied to the avalanche diode D_B and it provides a bias voltage of V_B to the base of Q_1. The temperature dependence of the V_{BE} drop across Q_1 and those across D_1 and D_2 results in respective temperature coefficients. Hence, with the use of resistors R_1 and R_2 with tapping across them at point N compensates for the temperature drifts in the base-emitter loop of Q_1. This results in generating a voltage reference V_R with normally zero temperature coefficient.

VOLTAGE REFERENCE CIRCUIT USING AVALANCHE DIODE REFERENCE

A voltage reference can be implemented using the breakdown phenomenon condition of a heavily doped PN junction. The Zener breakdown is the main mechanism for junctions, which breakdown at a voltage of 5V or less. For integrated transistors, the base-emitter breakdown voltage falls in the range of 6 to 8V. Therefore, the breakdown in the junctions of the integrated transistor is primarily due to avalanche multiplication. The avalanche breakdown voltage V_B of a transistor incurs a positive temperature coefficient, typically in the range of 2mV/0 C to 5mV/0 C.

Figure1.3.2 depicts a current reference circuit using avalanche diode reference. The base bias for transistor Q_1 is provided through register R_1 and it also provides the dc current needed to bias DB, D_1 and D_2 . The voltage at the base of Q_1 is equal to the Zener

voltage V_B added with two diode drops due to D_1 and D_2. The voltage across R_2 is equal to the voltage at the base of Q_1 less the sum of the base – emitter voltages of Q_1 and Q_2.

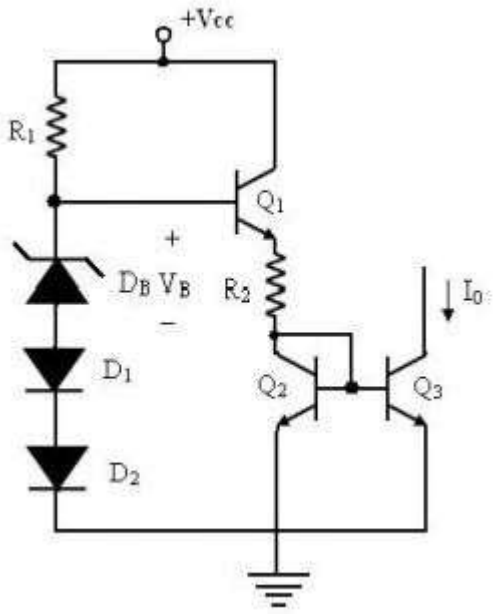

Figure 1.3.2.Voltage reference using avalanche diodes

[source:"Linear Integrated Circuits"by S.Salivahanan& V.S. Kanchana Bhaskaran, Page-56]

Hence, the voltage across R_2 is approximately equal to that across $D_B = V_B$. Since $Q_2$and Q_3 act as a current mirror circuit, current I_0 equals the current through R_2.

$$I_0 = VB/R2$$

It shows that, the output current I_0 has low temperature coefficient, if the temperature coefficient of R_2 is low, such as that produced by a diffused resistor in IC fabrication.

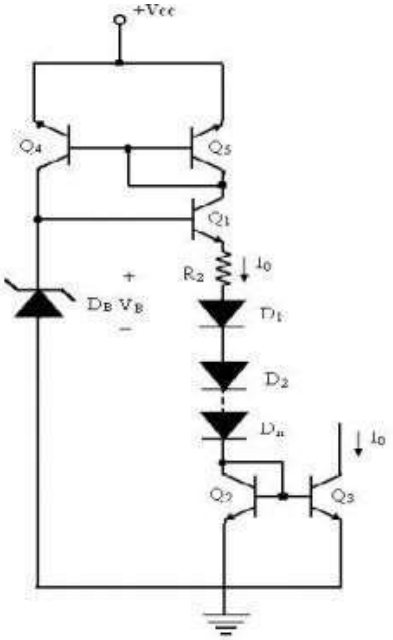

Figure 1.3.3.Voltage reference using temperature compensated avalanche diode reference source

[source:"Linear Integrated Circuits"by S.Salivahanan& V.S. Kanchana Bhaskaran, Page-56]

The zero temperature coefficients for output current can be achieved, if diodes are added in series with R_2, so that they can compensate for the temperature variation of R_2 and V_B. The temperature compensated avalanche diode reference source circuit is shown in figure 1.3.3. The transistor Q_4 and Q_5 form an active load current mirror circuit. The base voltage of Q_1 is the voltage V_B across Zener D_B.

Then, $V_B = (V_{BE} * n) + V_{BE}$ across $Q_1 + V_{BE}$ across Q_2 + drop across R_2.

Here, n is the number of diodes.

It can be expressed as $V_B = (n+ 2)\ V_{BE} - I_0 * R_2$

Differentiating for V_B, I_0, R_2 and V_{BE} +partially,2 with respect to temperature T, we get

$$\frac{\partial V_B}{\partial T} = n + 2\frac{\partial V_{BE}}{\partial T} + R_2\frac{\partial I_0}{\partial T} + I_0\frac{\partial R_2}{\partial T}$$

Dividing throughout by $I_0\ R_2$, we get

$$\frac{I}{I_o}\frac{\partial I_O}{\partial T} = 0 = \frac{1}{R_2 I_0}\left[\frac{\partial V_B}{\partial T} - (n+2)\frac{\partial V_{BE}}{\partial T} - \frac{1}{R_2}\frac{\partial R_2}{\partial T}\right.$$

Therefore, zero temperature coefficient of I_0 can be obtained, if the above condition is satisfied.

1.2 VOLTAGE SOURCES

A voltage source is a circuit that produces an output voltage V_0, which is independent of the load driven by the voltage source, or the output current supplied to the load. The voltage source is the circuit dual of the constant current source.

A number of IC applications require a voltage reference point with very low ac impedance and a stable dc voltage that is not affected by power supply and temperature variations. There are two methods which can be used to produce a voltage source, namely,

1. Using the impedance transforming properties of the transistor, which in turn determines the current gain of the transistor and
2. Using an amplifier with negative feedback.

VOLTAGE SOURCE CIRCUIT USING IMPEDANCE TRANSFORMATION

The voltage source circuit using the impedance transforming property of the transistor is shown in figure1.2.1 .The source voltage Vs drives the base of the transistor through a series resistance R_S and the output is taken across the emitter. From the circuit, the output ac resistance looking in to emitter is given by

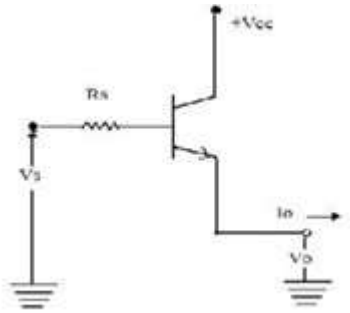

Figure1.2.1Voltage source circuit using impedance transformation

[source:"Linear Integrated Circuits"by S.Salivahanan& V.S. Kanchana Bhaskaran, Page-52]

It is to be noted that, equation is applicable only for small changes in the output current. The load regulation parameter indicates the changes in V_0 resulting from large changes in output current I_0 , Reduction in V_0 occurs as I_0 goes from no-load current to full-load current and this factor determines the output impedance of the voltage sources.

$$\frac{d_o}{dI_o} = R_0 = \frac{R_s}{\beta+1} + r_{eb} ;$$

With $\beta >> 100$, $R_0 = \frac{R_s}{\beta+1}$

EMITTER– FOLLOWER OR COMMON COLLECTOR TYPE VOLTAGE SOURCE

The figure1.2.2 shows an emitter follower or common collector type voltage source.

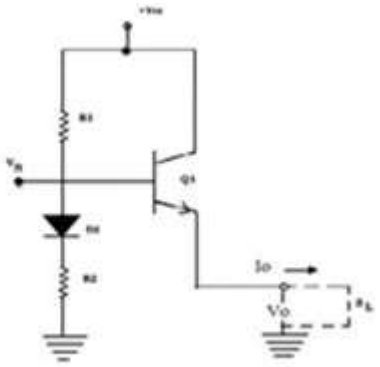

Figure1.2.2 Emitter –follower or common collector type voltage source

[source:"Linear Integrated Circuits"by S.Salivahanan& V.S. Kanchana Bhaskaran, Page-52]

This voltage source is suitable for the differential gain stage used in op-amps. This circuit has the advantages of

A. Producing low ac impedance and

B. Resulting in effective decoupling of adjacent gain stages.

The low output impedance of the common-collector stage simulates a low impedance voltage source with an output voltage level of V_0 represented= by

$$V_0 = V_{CC}\frac{R_2}{R_1 + R_2}$$

The diode D1 is used for offsetting the effect of dc value V_{BE} , across the E-B junction of the transistor, and for compensating the temperature dependence of V_{BE} drop of Q_1. The load Z_L shown in dotted line represents the circuit biased by the current through Q_1.

The impedance R_0 looking into the emitter= of Q_1 derived from the hybrid π model is given by

$$R_o = \frac{V_T}{I_1} + \frac{R_1 R_2}{\beta(R_1+R_2)}$$

VOLTAGE SOURCE USING TEMPERATURE COMPENSATED AVALANCHE DIODE

The voltage source using common collector stage has the limitations of its vulnerability for changes in bias voltage V_N and the output voltage V0 with respect to changes in supply voltage Vcc. This is overcome in the voltage source circuit using the breakdown voltage of the base- emitter junction shown in figure 1.2.3 below.

The emitter – follower stage of common – collector is eliminated in this circuit, since the impedance seen looking into the bias terminal N is very low. The current source I_1 is normally simulated by a resistor connected between Vcc and node n. Then, the output voltage level V0 at node N is given by

$$V_0 = V_B + V_{BE}$$

Where V_B is the breakdown voltage of diode D_B and V_{BE} is the diode drop across D_1.The breakdown diode D_B is normally realized using the base-emitter junction of the transistor. The diode D_1 provides partial compensation for the positive temperature coefficient effect of V_B. In a monolithic I_C structure, D_B and D_1 can be conveniently realized as a single transistor with two individual emitters as shown in figure 1.2.3.

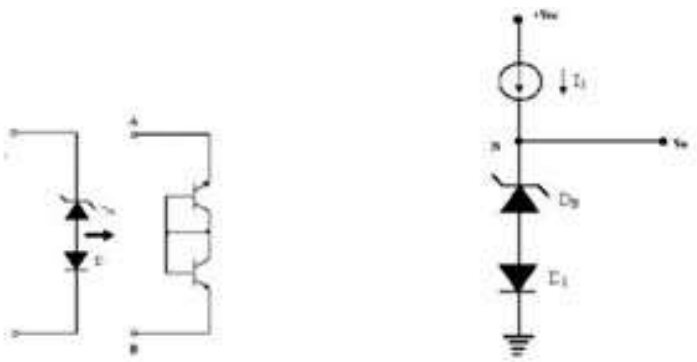

Figure 1.2.3 Temperature compensated avalanche diode

[source:"Linear Integrated Circuits"by S.Salivahanan& V.S. Kanchana Bhaskaran, Page-53]

The structure consists of composite connection of two transistors which are diode-connected back-to back. Since the transistors have their base to collector terminals common, they can be designed as a single transistor with two emitters.

The output resistance R0 looking into the output terminal in figure is given by

$$R_o = R_B + \frac{V_T}{I_1}$$

where R_B and V_T/I_1 are the ac resistances of the base–emitter resistance of diode D_B and D_1 respectively. Typically RB is in the range of 40Ω to 100Ω, and V0 in the range of 6.5V to 9V.

VOLTAGE SOURCE USING V_{BE} AS A REFERENCE

The output stage of op-amp requires stabilized bias voltage source, which can be obtained using a forward-biased diode connected transistor. The forward voltage drop for such a connection is approximately 0.7V, and it changes slightly with current.V_{BE} as multiplier circuit is shown in figure 1.2.4.

When a voltage level greater than 0.7V, is needed, several diodes can be connected in series, which can offer integral multiples of 0.7V. Alternatively, the figure shows a multiplier circuit, which can offer voltage levels that need not be integral multiplied of 0.7V. The drop across R2 equals VBE drop of Q_1. Considering negligible base current for Q_1, current through R2 is the same as that flowing through R1.

Therefore, the output voltage V_0 can be expressed as

$$V_0 = I_2(R_1 + R_2) = \frac{V_{BE}}{R_2}(R_1 + R_2) = V_{BE}\left(\frac{R_1}{R_2} + 1\right)$$

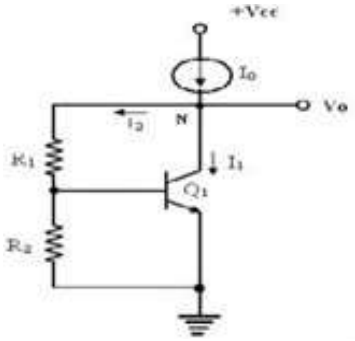

Figure 1.2.4.V_{BE} as multiplier circuit

[source:"Linear Integrated Circuits"by S.Salivahanan& V.S. Kanchana Bhaskaran, Page-53]

Hence, the voltage V_0 can be any multiple of V_{BE} by properly selecting the resistors $R_1$and R_2. Due to the shunt feedback provided by R_1, the transistor current I_1 automatically adjusts itself, towards maintaining I_2 and V_0 relatively independent of the changes in supply voltage.

The ac output resistance of the circuit R_0 is given= by,

$$R_O = \frac{dV_0}{dI_o} = \frac{R_1+R_2}{1+g_m R_2} \approx \frac{(R_1+R_2)}{R_2 g_m} \quad \text{When } g_m R_2 >> 1$$

$$R_O = \frac{V_0}{V_{BE}} \frac{1}{g_m} = \frac{V_O}{V_{BE}} \frac{V_1}{I_C} \quad \text{as } \frac{V_O}{V_{BE}} = \frac{(R_1+R_2)}{R_2}$$