Common Source Amplifier With Fixed Bias

Figure 3.2.1 shows Common Source Amplifier With Fixed Bias. The coupling capacitor C1 and C2 which are used to isolate the d.c biasing from the applied ac signal act as short c

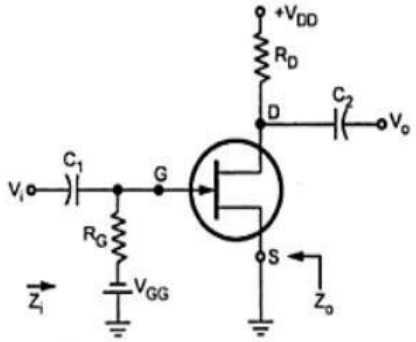

Figure 3.2.1 Common Source Amplifier With Fixed Bias

Diagram Source Electronic Tutorials

The following figure 3.2.2 shows the low frequency equivalent model for Common Source Amplifier With Fixed Bias. It is drawn by replacing all capacitors and d.c supply voltages with short circuit JFET with its low frequency a.c Equivalent circuit

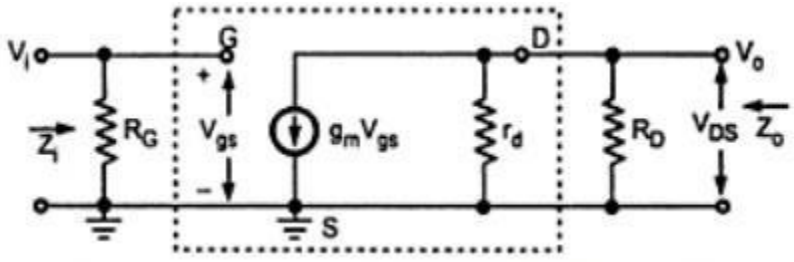

Figure 3.2.2 Common Source Amplifier With Fixed Bias

Diagram Source Brain Kart

low frequency equivalent model for Common Source Amplifier With Fixed Bias

Input Impedance Zi

$$Z_i = R_G$$

Output Impedance Zo

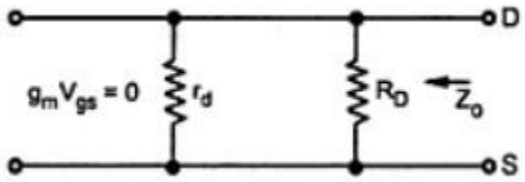

Figure 3.2.2

Figure 3.2.3 Equivalent Circuit model of JFET for output

Diagram Source Brain Kart

It is the impedance measured looking in figure 3.2.3 from the output side with input voltage Vi equal to Zero. As Vi=0,Vgs =0 and hence g_mVgs =0 . And it allows current source to be replaced by an open circuit. So,

$$Z_o = R_D \,||\, r_d$$

f the resistance rd is sufficiently large compared to R_D,then

$Z_o \approx R_D \qquad \because r_d >> R_D$

Voltage Gain A_v :

The voltage gain $A_v = \frac{V_{ds}}{V_{gs}} = \frac{V_o}{V_i}$

Looking at Fig. we can write

$$V_o = -g_m V_{gs} (r_d \| R_D)$$

As we know $V_i = V_{gs}$ we can write

$$V_o = -g_m V_i (r_d \| R_D)$$

$$\therefore \quad A_v = \frac{V_o}{V_i} = -g_m (r_d \| R_D)$$

and if $r_d >> R_D$,

$$A_v \approx -g_m R_D$$

Table summarizes performance of common source amplifier with fixed bias.

Parameter	Exact	With $r_d >> R_D$
Z_i	R_G	R_G
Z_o	$R_D \| r_d$	R_D
A_v	$-g_m (R_D \| r_d)$	$-g_m R_D$

Common source amplifier with self bias (Bypassed Rs)

Figure 3.2.4 shows Common Source Amplifier With self Bias. The coupling capacitor C1 and C2 which are used to isolate the d.c biasing from the applied ac signal act as short circuits for ac analysis. Bypass capacitor Cs also acts as a short circuits for low frequency analysis.

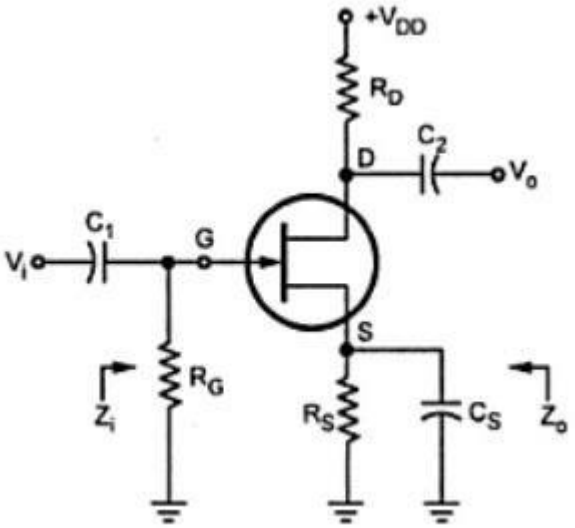

Figure 3.2.4 Common Source Amplifier With self Bias

Diagram Source Brain Kart

The following figure 3.2.5 shows the low frequency equivalent model for Common Source Amplifier With self Bias.

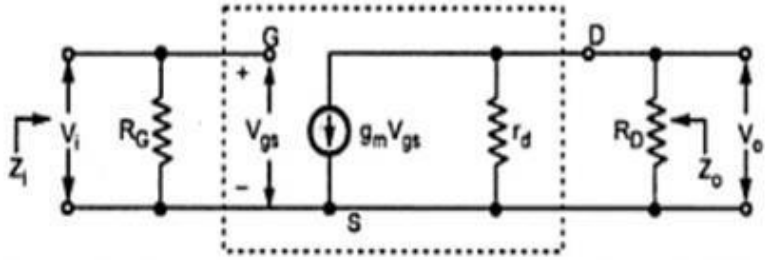

Figure 3.2.5 Common Source Amplifier With self Bias

Diagram Source Brain Kart

i) Input impedance Z_i : $Z_i = R_G$

ii) Output impedance Z_o : $Z_o = r_d \,||R_D$

if $r_d >> R_D$ $Z_o \approx R_D$

iii) Voltage gain A_v : $A_v = -g_m (r_d \,||R_D)$

If $r_d >> R_D$ $A_v = -g_m R_D$

FigureThe low frequency equivalent model for Common Source Amplifier With self Bias.The negative sign in the voltage gain indicates there is a 180o phase shift between input and output voltages.

Common source amplifier with self bias (unbypassed R_s)

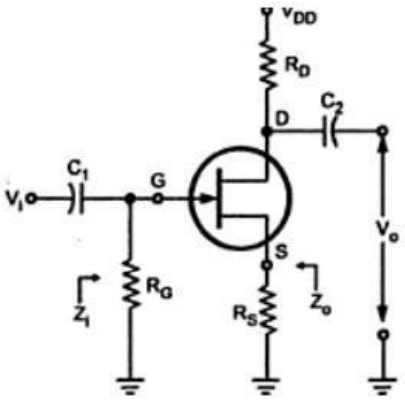

Fig3.7 **Common source amplifier** model of JFET

Figure 3.2.6 Common Source Amplifier model of JFET

Diagram Source Brain Kart

Now Rs will be the part of low frequency equivalent model as shown in figure 3.2.6

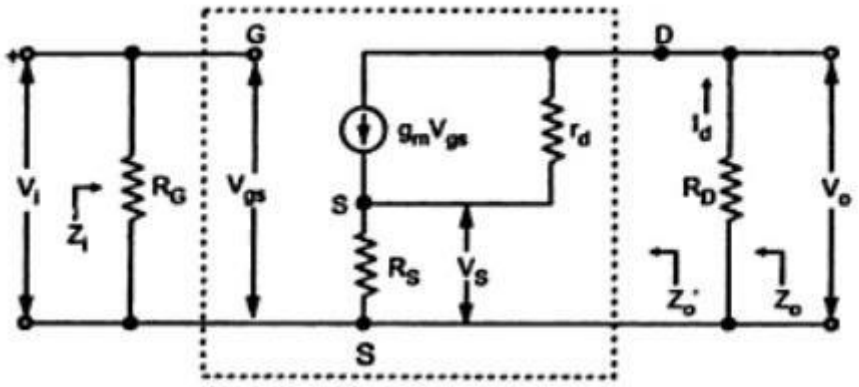

Figure 3.2.7 Small signal model for Common source amplifier model of JFET

Diagram Source Brain Kart

Figure 3.2.7 **Input Impedance Z_i**

$$Z_i = R_G$$

Output Impedance Z_o

It is given by

$$Z_o = Z_o' \| R_D$$

where $$Z_o' = \left.\frac{V_o}{I_d}\right|_{V_i = 0}$$

$$Z_o = [\, r_d + R_s (\mu + 1) \,] \| R_D$$

$$Z_o = [\, r_d + R_s (g_m r_d + 1) \,] \| R_D$$

Voltage gain (A_v)

It is given by

$$A_v = \frac{V_o}{V_i}$$

We know that,

$$V_o = - I_d R_D$$

$$A_v = \frac{V_o}{V_i} = \frac{- g_m r_d R_D}{r_d + R_s + R_D + g_m R_s r_d}$$

Dividing numerator and denominator by r_d we get,

$$\therefore \quad A_v = \frac{V_o}{V_i} = \frac{- g_m R_D}{1 + g_m R_s + \dfrac{R_s + R_D}{r_d}}$$

If $r_d >> R_s + R_D$

$$A_v = \frac{V_o}{V_i} = \frac{- g_m R_D}{1 + g_m R_s}$$

Table summarizes performance of common source amplifier with self bias.

Parameter	Bypassed R_S		Unbypassed R_S	
	Exact	$r_d >> R_D$	Exact	$r_d >> R_D$
Z_i	R_G	R_G	R_G	R_G
Z_o	$R_D \parallel r_d$	R_D	$[r_d + R_S(g_m r_d + 1)] \parallel R_D$ or $[r_d + R_S(\mu + 1)] \parallel R_D$	$[r_d + R_S(g_m r_d + 1)] \parallel R_D$ or $[r_d + R_S(\mu + 1)] \parallel R_D$
A_v	$-g_m(R_D \parallel r_d)$	$-g_m R_D$	$\frac{-g_m R_D}{1 + g_m R_S + \frac{R_S + R_D}{r_d}}$	$\frac{-g_m R_D}{1 + g_m R_S}$

Common source amplifier with Voltage divider bias (Bypassed R_s)

Figure 3.2.8 shows Common Source Amplifier With voltage divider Bias. The coupling capacitor C_1 and C_2 which are used to isolate the d.c biasing from the applied ac signal act as short circuits for ac analysis. Bypass capacitor Cs also acts as a short

SHAPE * MERGEFORM
circuits for low frequency analysis.

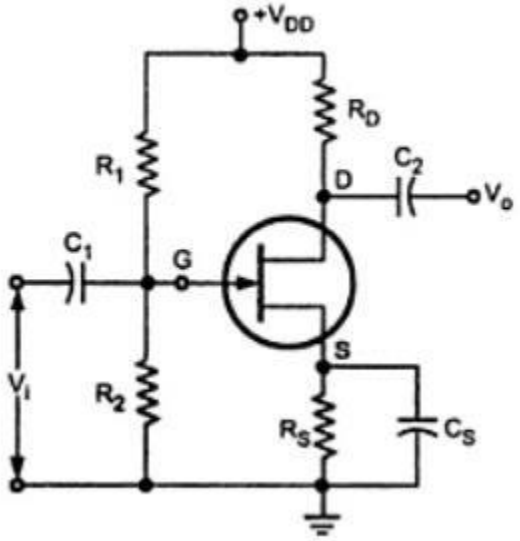

Figure 3.2.8 Common Source Amplifier With voltage divider Bias (Bypassede Rs)

Diagram Source Brain Kart

The following figure 3.2.9 shows the low frequency equivalent model for Common Source Amplifier With voltage divider Bias

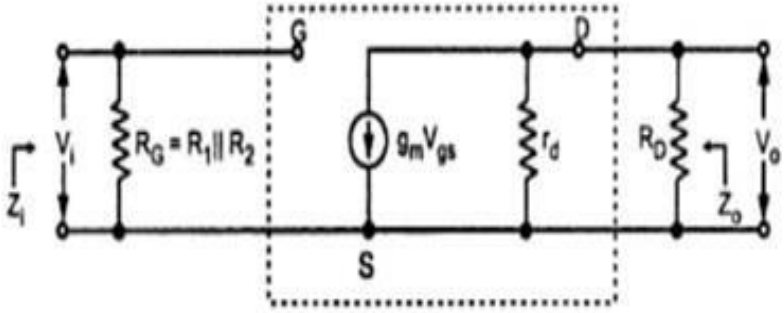

Figure 3.2.9 low frequency equivalent model for Common Source Amplifier With voltage divider Bias

Diagram Source Brain Kart

The parameters are given by

$$R_G = R_1 \| R_2$$

$$Z_i = R_G$$

$$= R_1 \| R_2$$

$$Z_o = r_d \| R_D$$

if $r_d >> R_D$ $\quad Z_o \approx R_D$

$$A_v = -g_m (r_d \| R_D)$$

If $r_d >> R_D$ $\quad A_v = -g_m R_D$

The negative sign in the voltage gain indicates there is a 180^o phase shift between input and output voltages.

Common source amplifier with Voltage divider bias (unbypassed R_s)

Figure 3.2.10 shows small signal model of Common source amplifier with Voltage divider bias(without Bypassed Rs.

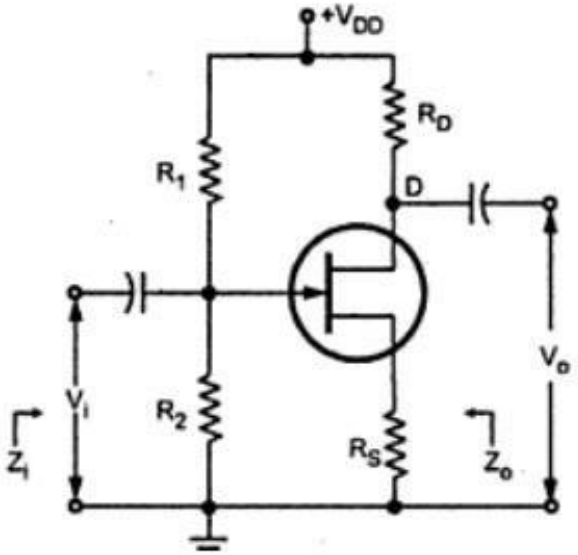

Figure 3.2.10 small model of Common source amplifier with Voltage divider bias(without Bypassed Rs

Diagram Source Brain Kart

Now Rs will be the part of low frequency equivalent model as shown in figure 3.2.11.

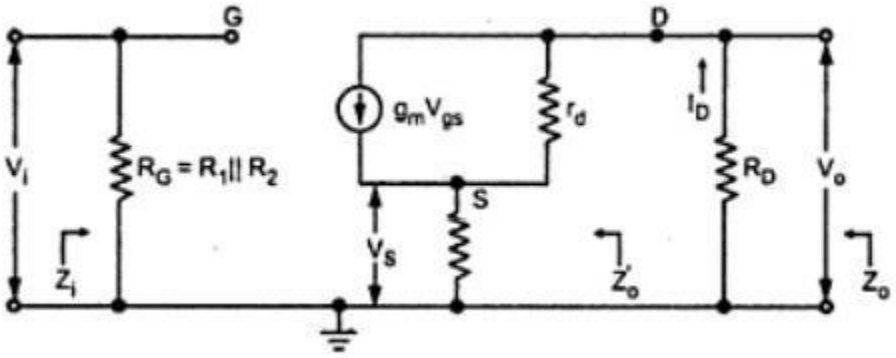

Figure 3.2.11 small model of Common source amplifier with Voltage divider bias(without Bypassed Rs

Diagram Source Brain Kart

It is important to note that, here, $R_G = R_1 \| R_2$.

$$Z_i = R_G = R_1 \| R_2$$

$$Z_o' = r_d + g_m R_s r_d + R_s$$

or $$Z_o' = r_d + R_s (\mu + 1)$$

$$Z_o = [\, r_d + g_m R_s r_d + R_s \,] \| R_D$$

or $$Z_o = [\, r_d + R_s (\mu + 1) \,] \| R_D$$

$$A_v = \frac{-g_m R_D}{1 + g_m R_s + \dfrac{R_s + R_D}{r_d}}$$

Where Av is the Voltage Gain.

Common Drain Amplifier

In this circuit shown in figure 3.3.1, input is applied between gate and source and output is taken between source and drain.

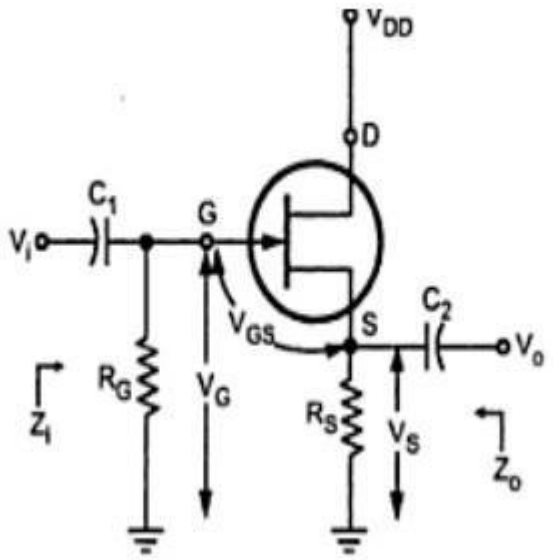

Figure 3.3.1 Common Drain Amplifier

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In this circuit, the source voltage is

$$V_s = V_G + V_{GS}$$

When a signal is applied to the JFET gate via C_1 ,VG varies with the signal. As VGS is fairly constant and $V_s = V_G + V_{GS}$, Vs varies with Vi. The following figure 3.3.2 shows the low frequency equivalent model for common drain circuit.

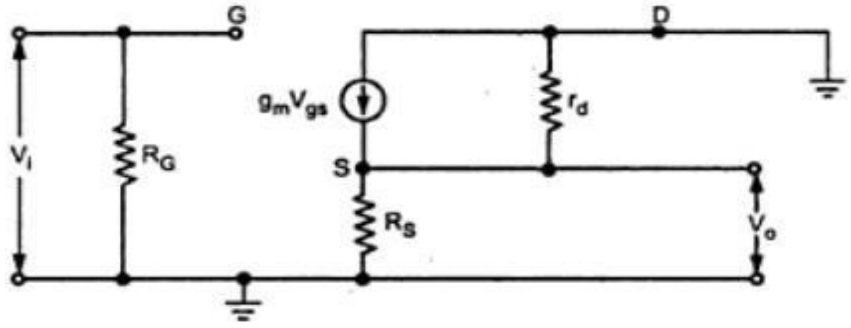

Figure 3.3.2 Small model of common Drain Amplifier

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Input Impedance Z_i

Figure 3.3.3 shows the simplified small model of common Drain Amplifier.

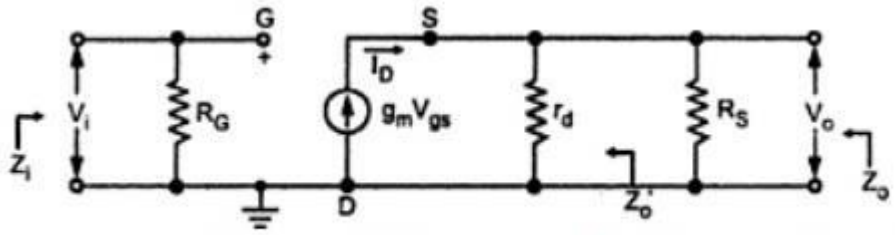

Figure 3.3.3 Simplified small model of common Drain Amplifier

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$$Zi = RG$$

Output Impedance Z_o

It is given by

$$Z_o = Z_o' || R_s$$

where $$Z_o' = \left.\frac{V_o}{I_d}\right|_{V_i = 0}$$

Applying KVL to the outer loop we can have,

$$V_i + V_{gs} - V_o = 0$$

As $$V_i = 0,$$

$$V_{gs} = V_o$$

Looking at Fig. we can write that,

$$g_m V_{gs} = I_d$$

But Vgs = Vo, so

$$g_m V_o = I_d$$

$$Z_o' = \frac{V_o}{I_d} = \frac{1}{g_m}$$

$$\therefore \quad Z_o = \frac{1}{g_m} || R_s$$

Voltage gain (A_v)

It is given by

$$A_v = \frac{V_o}{V_i}$$

Looking at Fig. we can write that,

$$V_o = - I_d (r_d || R_s)$$

and $$I_d = g_m V_{gs}$$

$$\therefore \quad V_o = - g_m V_{gs} (r_d || R_s)$$

But

$$V_i = - V_{gs} + V_o$$

$$= - V_{gs} + [- g_m V_{gs} (r_d || R_s)]$$

Substitute the value V_o and V_i. Then

$$A_v = \frac{-g_m V_{gs} (r_d \,||\, R_s)}{-V_{gs} (1 + g_m (r_d \,||\, R_s))}$$

$$= \frac{g_m (r_d \,||\, R_s)}{1 + g_m (r_d \,||\, R_s)}$$

if $r_d >> R_s$

$$A_v = \frac{g_m R_s}{1 + g_m R_s}$$

if $g_m R_s >> 1$

$A_v \approx 1$, but it is always less than one.

Common drain circuit does not provide voltage gain.& there is no phase shift between input and output voltages.

Table summarizes the performance of common drain amplifier

	Exact	$r_d >> R_D$
Z_i	R_G	R_G
Z_o	$\frac{1}{g_m} \,\|\|\, R_s$	$\frac{1}{g_m} \,\|\|\, R_s$
A_v	$\frac{g_m (r_d \,\|\| R_s)}{1 + g_m (r_d \,\|\| R_s)}$	$\frac{g_m R_s}{1 + g_m R_s}$

Common Gate Amplifier

In this circuit in figure 3.4.1, input is applied between source and gate and output is taken between drain and gate.

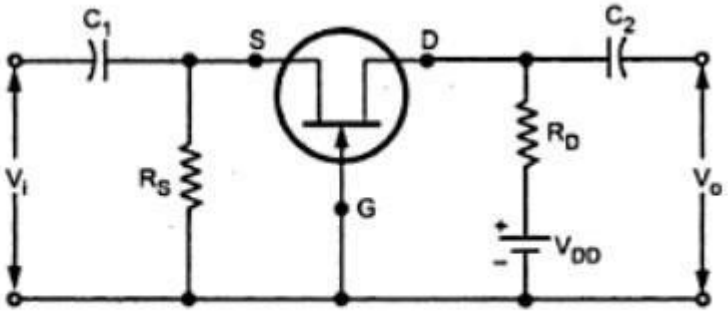

Fig3.14 **Circuit diagram of Common gate amplifier**

Figure 3.4.1 Common Gate Amplifier

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Figure 3.4.2 Small Signal for Common Gate Amplifier

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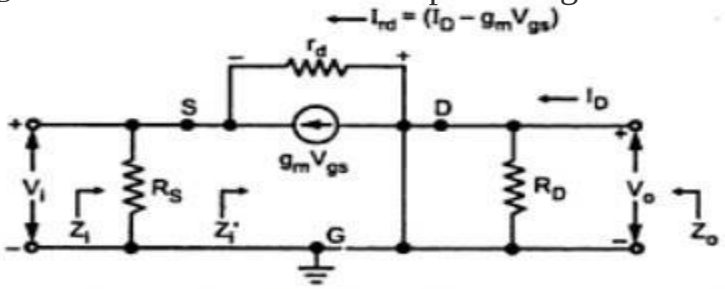
In CG Configuration, gate potential is at constant potential. so, increase in input voltage Vi in positive direction increase the negative gate source voltage sown in figure 3.4.2. Due to I_D reduces, reduces, reducing the drop I_DR_D. Since $V_D= V_{DD}-I_DR_D$, the reduction in I_D results in an increase in output voltage.

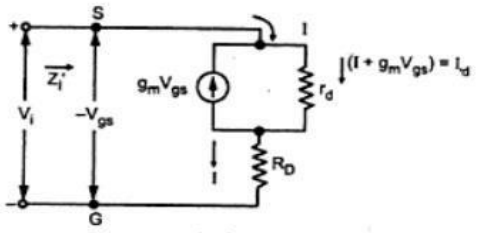


1. Input Impedance (Zi)

$$Z_i = R_s \parallel Z_i'$$

And

$$Z_i' = \frac{V_i}{I}$$



$$I_{rd} = I + g_m V_{gs}$$

$$\therefore \quad I = I_{rd}\ g_m V_{gs}$$

where $$I_{rd} = \frac{V_i - IR_D}{r_d}$$

Figure 3.4.3 Common Gate Amplifier for Zi Calculation

Diagram Source Brain Kart

After substituting and simplification,

$$\frac{V_i}{I} = \frac{1+\frac{R_D}{r_d}}{\frac{1}{r_d}+g_m} = \frac{r_d + R_D}{1+g_m r_d}$$

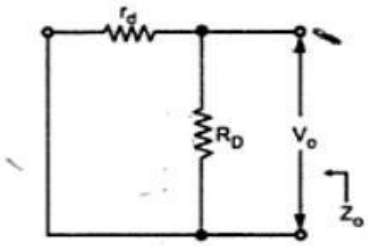
And

$$Z_i = R_s \parallel Z_i' = R_s \parallel \frac{r_d + R_D}{1+g_m r_d}$$

If $r_d >> R_D$ and $g_m r_d >> 1$ then we can write,

$$Z_i = R_s \parallel \frac{r_d}{g_m r_d} = R_s \parallel \frac{1}{g_m}$$

2. Output



It is given by

$$Z_o = r_d \parallel R_D$$

If $r_d >> R_D$

$$Z_o \approx R_D$$

3. Voltage gain (A_v)

$$A_v = \frac{V_o}{V_i}$$

$$V_o = -I_D R_D$$

$$V_i = -V_{gs}$$

Using KVL to the outer loop, after simplification

$$A_v = \frac{V_o}{V_i} = \frac{-I_d + R_D}{\frac{-I_d(r_d + R_D)}{1 + g_m r_d}}$$

$$= \frac{R_D(1 + g_m r_d)}{r_d + R_D}$$

If $r_d >> R_D$ and $g_m r_d >> 1$

$$A_v = \frac{R_D(g_m r_d)}{r_d} = R_D g_m$$

Table summarizes the performance of common gate amplifier

	Exact	$r_d >> R_{OD}$
Z_i	$R_s \parallel \left[\frac{r_d + R_D}{1 + g_m r_d}\right]$	$R_s \parallel \frac{1}{g_m}$
Z_o	$r_d \parallel R_D$	R_D
A_v	$\frac{R_D(1 + g_m r_d)}{r_d + R_D}$	$g_m R_D$

BI CMOS Inverter Circuit Diagram

BICMOS logic circuits are made by combining the CMOS and bipolar IC technologies. These ICs combine the advantages of BJT and CMOS transistors in them. We know that the speed of BJT is very high compared to CMOS. However, power dissipation in CMOS is extremely low compared to BJT. By combining such advantages, we construct the BICMOS circuits.

Figure 3.6.1 shows one configuration of the BICMOS inverter, and Fig. 3.43 shows its modified version. In Fig. 3.43, we see that MOS transistors T_3 and T_4 form the CMOS inverter logic circuit. We find that T_3 and T_4 are driven separately from $+V_{DD}/V_{CC}$ rail. With input voltage V_i = **0**, the PMOS will conduct and the NMOS will remain OFF. This drives a current through the base of the bipolar junction transistor T_1 and turns it ON. This in turn charges the parasitic load capacitance C_L at a very fast rate. Thus the output voltage V_o rises very fast, which is usually much faster than the charging of C_L by an MOS transistor by itself.

Now, let $V_i = +V_{DD}$ (≡ logic **1**). Then T_4 will turn ON and T_3 will turn OFF; this drives T_2 into the ON-state. Since T_3 is OFF, T_1 will also remain OFF. In this condition, C_L discharges very fast through T_{2ON}. Thus the charging and discharging of C_L is through BJTs and hence very fast.

The circuit shown in Fig. 3.6.1 has two major defects. The first of these is that whenever the input is at logic **1**, since T_3 is ON, there will be a continuous path from $+V_{DD}$ to ground. As a result, steady power drain will occur in this case. This is totally against the advantages of CMOS gates. The second defect is that there is no discharge path for the base currents of T_1 and T_2. This will therefore reduce the speed of the circuit

To overcome these problems, we modify the circuit, as shown in Fig. 3.44. In this case, NMOS transistor T_4 has its drain connected to the output terminal rather than to $+V_{DD}$. As before, when T_3 is turned ON, T_1 is also turned ON. Now, when T_4 is turned ON, we find T_2 also to turn ON.. However, since the collector and base of T_2 are shorted together through T_{4ON}, the output voltage V_o will now be equal V_{BES}, the saturation base-emitter voltage of T_2 (= 0.8 V). Thus in this case, the output swing is between V_{CC} and V_{BES}.

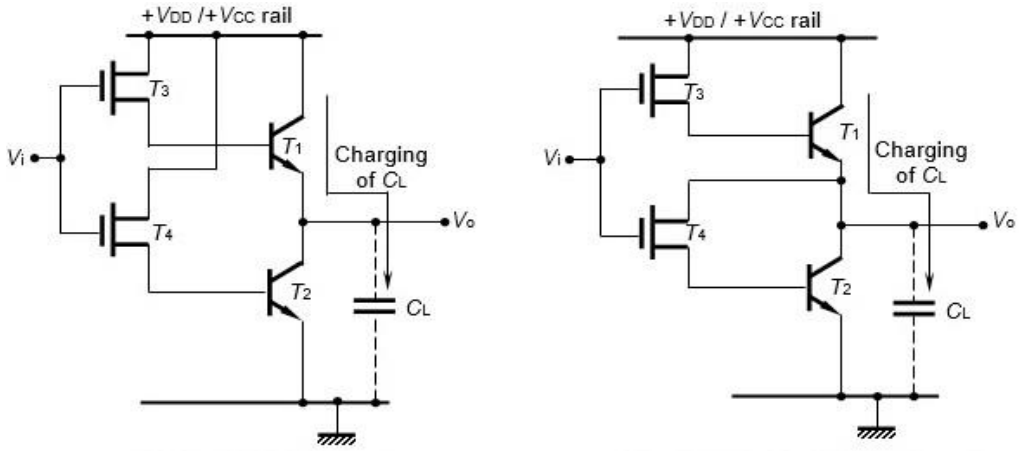


Figure 3.6.1 BI CMOS Inverter

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Features of BICMOS gates:

1. This has the advantages of both the BJTs and CMOS gates.
2. The power driver (BJT amplifier) in the output stage is capable of driving large loads.
3. The circuit, because of its CMOS input transistors, has high input impedance.
4. The output impedance of the circuit is low.
5. The noise margin is high because of the CMOS input stage.

6. The supply voltage VDD is 5 V.
7. The chip area is small.

JFET Amplifiers

It provides an excellent voltage gain with high input impedance. Due to these characteristics, it is often preferred over BJT.

Three basic FET configurations

Common source,

Common drain

Common gate

Figure 3.1.1 shows the small signal low frequency a.c Equivalent circuit for n-channel JFET.

JFET low frequency a.c Equivalent circuit

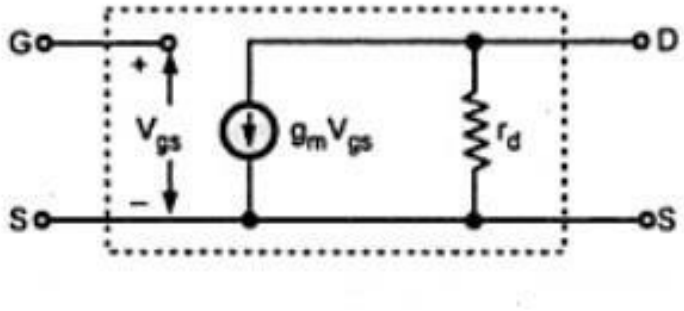


Figure 3.1.1 Small Signal Model of JFET

Diagram Source Brain Kart

JFET Low Frequency ac Equivalent Circuit:

Figure 3.1.1 shows the small signal low frequency ac equivalent circuit for n-channel JFET. The relation of I_D by V_{GS}, is included as a current source gm V_{GS} connected from drain to source. The input impedance is represented by the open circuit at its input terminals, since gate current I_G is zero. The output impedance is represented by rd from drain to source.

The JFET parameters are the major components of low frequency small signal model for JFET. We know that, drain to source current of JFET is controlled by gate to source voltage.

The change in the drain current due to change in gate to source voltage can be determined using the trans conductance factor gm. It is given as,

$$\Delta I_d = g_m \Delta V_{GS}$$

In BJT the relation between an output and input quantity is given by amplification factor β, whereas in JFET this relation is given by trans conductance factor gm. The another important parameter of JFET is drain resistance rd. It is given by

$$rd = \Delta V_{DS} / \Delta I_D |V_{GS} = \text{constant}.$$

It determines the output impedance Z_O of the JFET amplifier.

For the hybrid equivalent model, the parameters are defined at an operating point. The quantities hie, hre, hfe, and hoe are called hybrid parameters and are the components of a small – signal equivalent circuit in the figure 3.1.2.

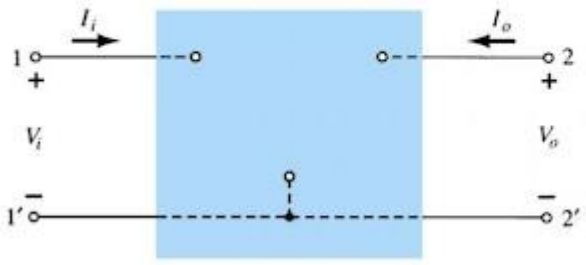


Figure 3.1.2 Description of the hybrid equivalent model of two port system

Diagram Source Brain Kart

• The description of the hybrid equivalent model will begin with the general two port system. The set of equations in which the four variables can be related are:

Vi = h11Ii + h12Vo

Io = h21Ii + h22Vo

The four variables h11, h12, h21 and h22 are called hybrid parameters (the mixtureof variables in each equation results in a " hybrid" set of units of measurement for the h parameters. Set Vo = 0, solving for h11, h11 = Vi / Ii Ohms This is the ratio of input voltage to the input current with the output terminals shorted. It is called Short circuit input impedance parameter. If Ii is set equal to zero by opening the input leads, we get expression for h12: h12 = Vi / Vo , This is called open circuit reverse voltage ratio.Again by setting Vo to zero by shorting the output terminals, we get h21 = Io / Ii known as short circuit forward transfer current ratio. Again by setting I1 = 0 by opening the input leads, h22 = Io / Vo . This is known as open circuit output admittance in figure 3.1.3 and 3.1.4. This is represented as resistor (1/h22)

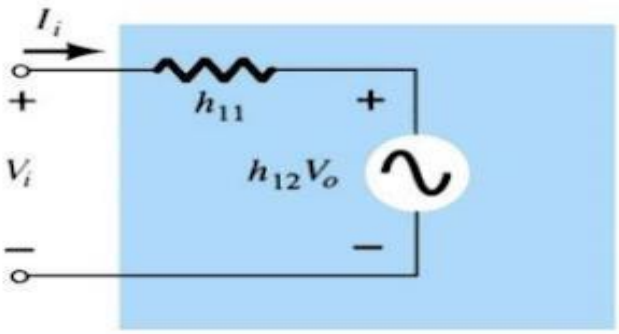
h11 = hi = input resistance

h12 = hr = reverse transfer voltage ratio

h21 = hf = forward transfer current ratio

h22 = ho = Output conductance

Hybrid Input equivalent circuit



Hybrid output equivalent circuit

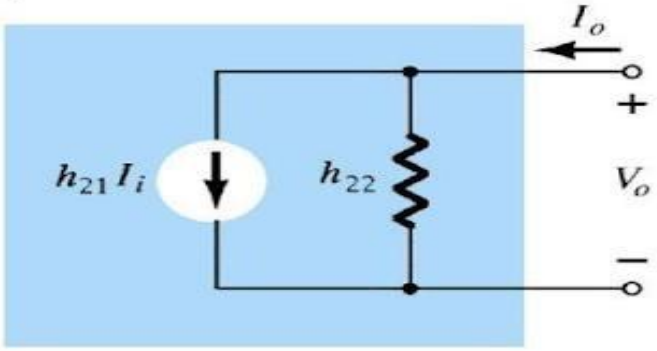
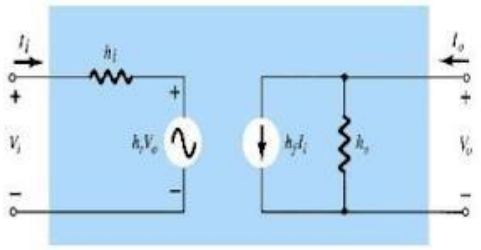


Figure 3.1.3 Hybrid input and Output equivalent Circuit

Diagram Source Brain Kart

Complete hybrid equivalent circuit



Common Emitter Configuration - hybrid equivalent circuit

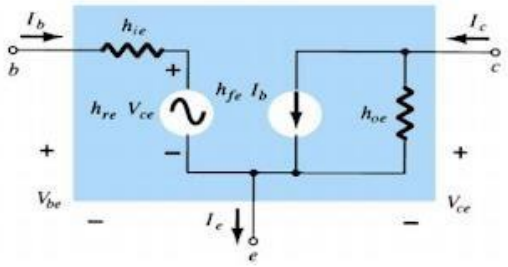


Figure 3.1.4 Hybrid input and Output equivalent Circuit

Diagram Source Brain Kart

Essentially, the transistor model is a three terminal two – port system. The h parameters, however, will change with each configuration. To distinguish which parameter has been used or which is available, a second subscript has been added to the h parameter notation. For the common – base configuration, the lowercase letter b is added, and for common emitter and common collector configurations, the letters e and c are used respectively.

Small signal Analysis of MOSFET

Common-Source Configuration

This configuration serves as the gain stage. The disadvantage is high output impedance. Capacitor C_S is included in figure 3.5.1 is a for current source biasing.

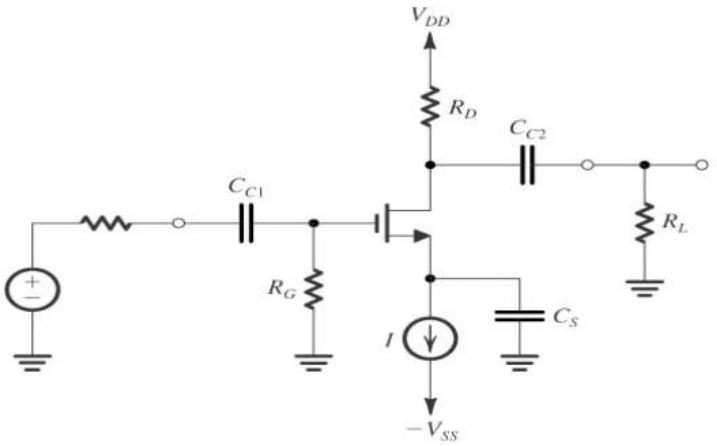


Figure 3.5.1 Common Source Configuration of MOSFET

Diagram Source Brain Kart

The figure 3.5.2 shows small Signal mode of Common Source Configuration of MOSFET.

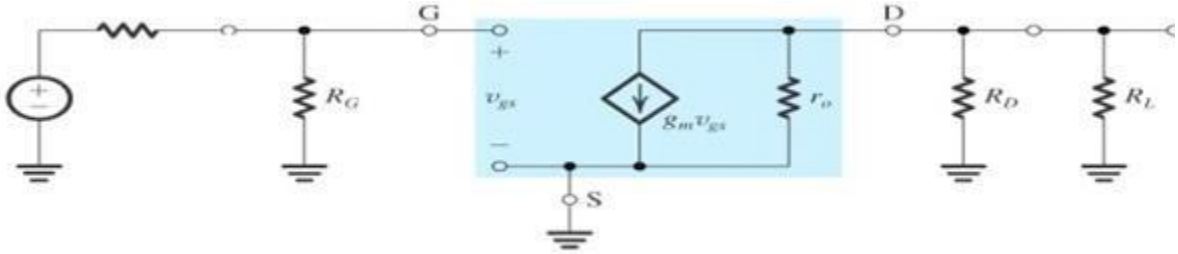


Figure 3.5.2 Small Signal mode of Common Source Configuration of MOSFET

Diagram Source Brain Kart

The input resistance , Output resistance and Voltage gain of MOSFET Common Source Circuit are as follows,

$$R_{in} = R_G$$

$$R_o = r_o \,//\, R_D$$

$$A_{vo} = -g_m \cdot (r_o \,//\, R_D)$$

Common-Gate Configuration

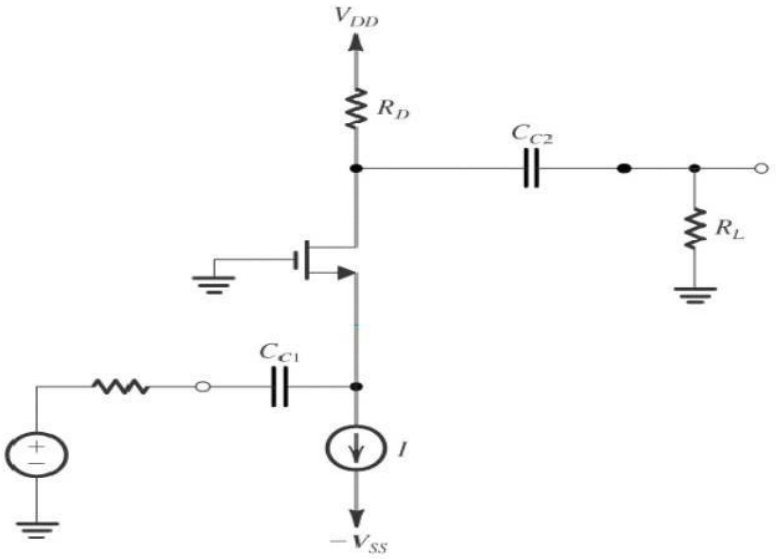


Figure 3.5.3 Common gate Configuration of MOSFET

Diagram Source Brain Kart

The figure3.5.3 & 3.5.4 shows small Signal mode of Common gate Configuration of MOSFET

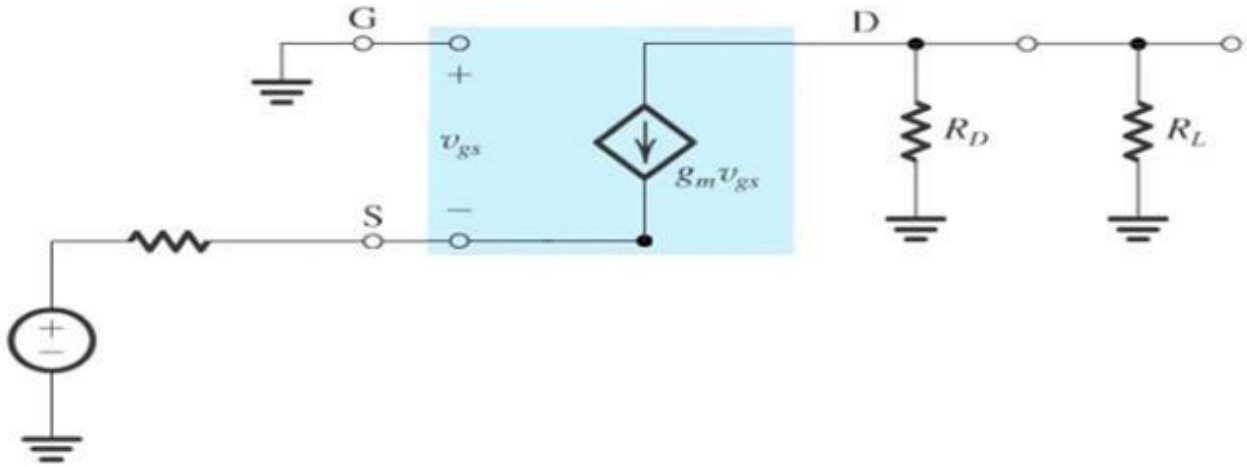


Figure 3.5.4 Small Signal mode of Common Gate Configuration of MOSFET

Diagram Source Brain Kart

The input resistance , Output resistance and Voltage gain of MOSFET Common Gate Circuit are as follows,

$$R_{in} = \frac{1}{g_m}$$

$$R_o = R_D$$

$$A_{vo} - g_m \cdot R_D$$

This amplifier provides gain and is useful when a specific (low) *Rin* is required.

This is, e.g., the case when the impedance needs to be matched, as with transmission lines (e.g. to 50 Ω). Another application of the CG configuration is that it acts as a current buffer (current gain close to unity, small *Rin*, large *Rout*).

Source Follower (Common-Drain Configuration)

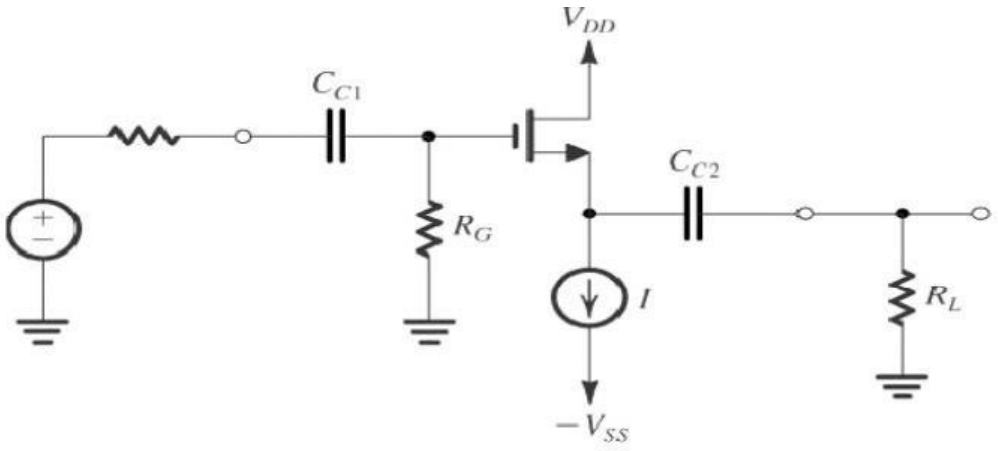


Figure 3.5.5 Common Drain Configuration of MOSFET

Diagram Source Brain Kart

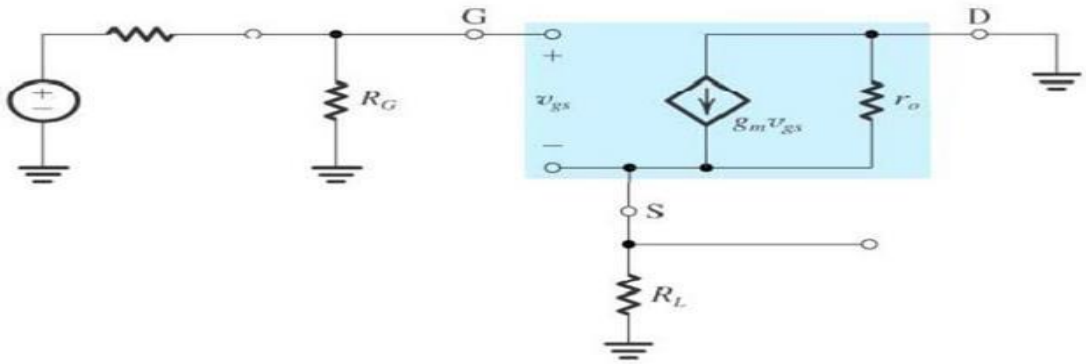


Figure 3.5.6 Small Signal mode of Common drain Configuration of MOSFET

Diagram Source Brain Kart

The figure 3.5.5 & 3.5.6 shows small Signal mode of Common drain Configuration of MOSFET

The input resistance , Output resistance and Voltage gain of MOSFET Common drain Circuit are as follows,

$$R_{in} = R_G$$

$$R_o = r_o // \frac{1}{g_m} \approx \frac{1}{g_m}$$

$$A_{vo} = \frac{g_m \cdot r_o}{1 + g_m \cdot r_o}$$