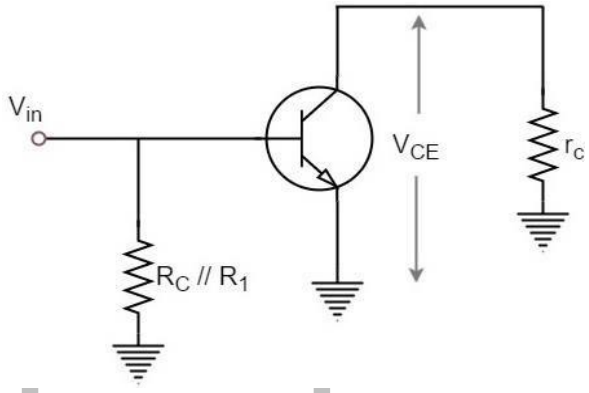
AC Load Line

The DC load line discussed previously, analyzes the variation of collector currents and voltages, when no AC voltage is applied. Whereas the AC load line gives the peak-to-peak voltage, or the maximum possible output swing for a given amplifier. We shall consider an AC equivalent circuit in figure 2.5.1 of a CE amplifier for our understanding.



www.binils.com

Figure 2.5.1 AC equivalent circuit of a CE amplifier

Diagram Source Electronic Tutorials

From the above figure 2.5.1

$$VCE=(RC//R1)\times IC$$

$$r_C=R_C//R_1$$

For a transistor to operate as an amplifier, it should stay in active region. The quiescent point is so chosen in such a way that the maximum input signal excursion is symmetrical on both negative and positive half cycles.

Hence,

$$V_{max}=V_{CEQ}$$

$V_{max}=V_{CEQ}$ and $V_{min}=-V_{CEQ}$

Where V_{CEQ} is the emitter-collector voltage at quiescent point

The following graph represents the AC load line which is drawn between saturation and cut off points.

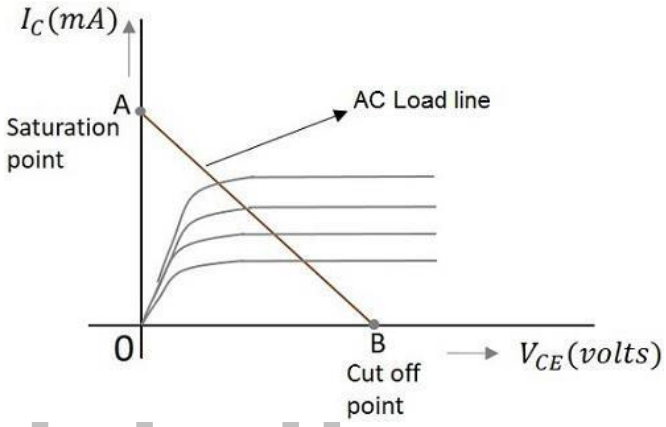


Figure 2.5.2 AC load line

Diagram Source Electronic Tutorials

www.binils.com

From the graph above figure 2.5.2 , the current IC at the saturation point is

$$I_C(sat)=I_{CQ}+(V_{CEQ}/r_C)$$

The voltage V_{CE} at the cutoff point is

$$VCE(off)=V_{CEQ} + I_{CQ}r_C$$

Hence the maximum current for that corresponding $V_{CEQ} = V_{CEQ} / (R_C // R_1)$ is

$$I_{CQ}=I_{CQ'}(R_C//R_1)$$

Hence by adding quiescent currents the end points of AC load line are

$$IC(sat)=I_{CQ}+V_{CEQ}/(R_C//R_1)$$

$$V_{CE(off)}=V_{CEQ}+I_{CQ}(R_C//R_1)$$

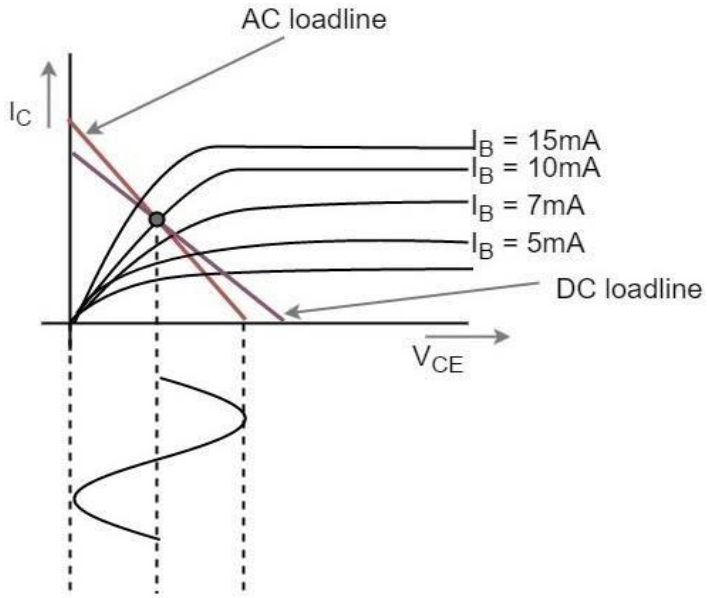
AC and DC Load Line

When AC and DC Load lines are represented in a graph, it can be understood that they are not identical. Both of these lines intersect at the **Q-point** or **quiescent point**. The endpoints of AC load line are saturation and cut off points. This is understood from the figure 2.5.3 below.

Figure 2.5.3 AC & DC equivalent DC load line

Diagram Source Electronic Tutorials

www.binils.com



From the above figure 2.5.3 , it is understood that the quiescent point (the dark dot) is obtained when the value of base current IB is 10mA. This is the point where both the AC and DC load lines intersect.

www.binils.com

Analysis of CB amplifiers using Hybrid π equivalent circuits

In Common Base circuit, the signal source is coupled to the emitter of the transistor through C_1. The load resistance R_L is coupled to the collector of the transistor through C_2. The positive going pulse of input source increases the emitter voltage. As base voltage is constant, forward bias of emitter-base junction reduces. This reduces I_b, I_c and drop across R_c.

$$V_o = V_{CC} - I_C R_C$$

Reduction in I_C results in an increase in V_o. Positive going input produces positive going output and vice versa. So there is no phase shift between input and output in common base amplifier.

An Amplifier circuit is used to increase the strength of the signal. The amplifier circuit uses the power supply to increase the signal strength. The amplification provided by the amplifier circuit is measured in terms of Gain of an amplifier. The gain of the amplifier is the ratio of output to input, which is always greater than one. Amplification does not alter frequency and waveform shape.

www.binils.com

Gain of the Amplifier (A) = Output/(Input)

Symbol

Below figure 2.4.1 illustration gives the amplifier symbol.

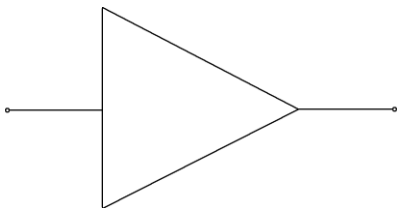


Figure 2.4.1 Symbol of Amplifier

Diagram Source Elprocus

Amplifier Module

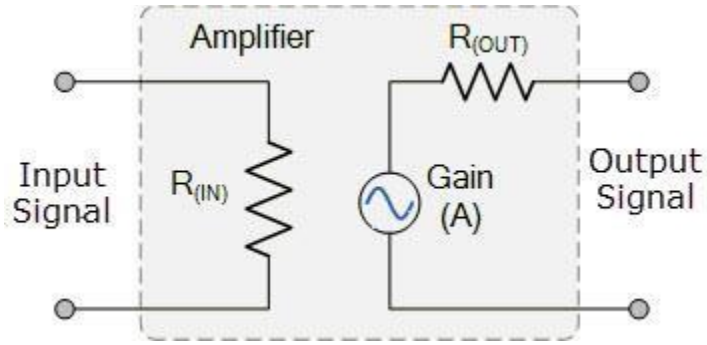


Figure 2.4.2 Amplifier Module

Diagram Source Elprocus

The ideal amplifier module has three important properties, namely, input impedance (Rin), output impedance (Rout) and of course amplification called as Gain(A) in figure 2.4.2. The amplifier module explains the general system of amplification with input and output signal. The impedance Rin increases the signal strength at gain A to produce the desired signal strength. Rin should be infinite and Rout should be zero.

www.binils.com

Types of Amplifiers

The below table explains the configuration, classification, and frequency of operation for different signals.

Type of Signal	Configuration	Classification	Operational Frequency
Small Signals	Common Emitter (CE)	Class A Amplifier	Direct Current (DC)
Large Signals	Common Base (CB)	Class B Amplifier	Audio Frequency (AF)
	Common Collector (CC)	Class AB Amplifier	Radio Frequency (RF)
		Class C Amplifier	VHF, UHF and SHF Frequencies

Different Amplifier Configurations

Transistors are used in amplifiers in three different configurations, namely,

Common Base (CB)
Common Collector (CC)
Common Emitter (CE).

The Common Emitter circuit is most widely used configuration. This circuit has grounded emitter. This circuit gives a medium level input impedance and output impedance. Voltage gain and current gain are medium, and the output reverses the input.

The Common collector circuit is widely used as a buffer. It is called as Emitter-follower. The emitter voltage follows that of the base. This gives a high input impedance and low output impedance. It has grounded collector.

www.binils.com

The Common base circuit provides low input impedance and high output impedance. The base of the transistor in this configuration is grounded. Input and output are in phase.

Common Base Amplifier Circuit

NPN and PNP transistors are used in Amplifier circuits. Both NPN and PNP have input provided at the emitter of the transistor and the output is taken at the collector of the transistor in figure 2.4.3 .

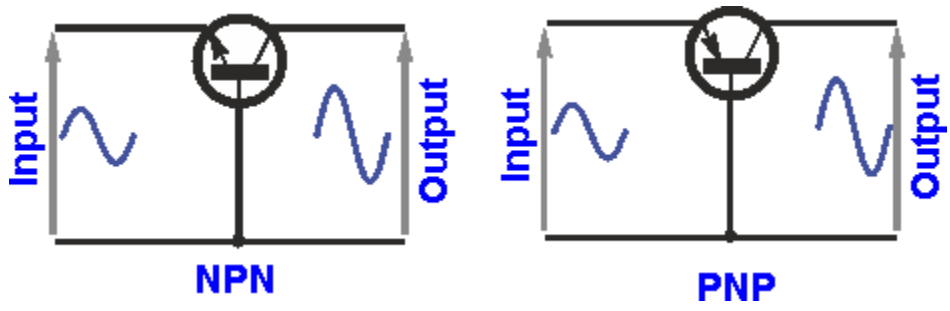


Figure 2.4.3 Common Base Amplifier Configuration

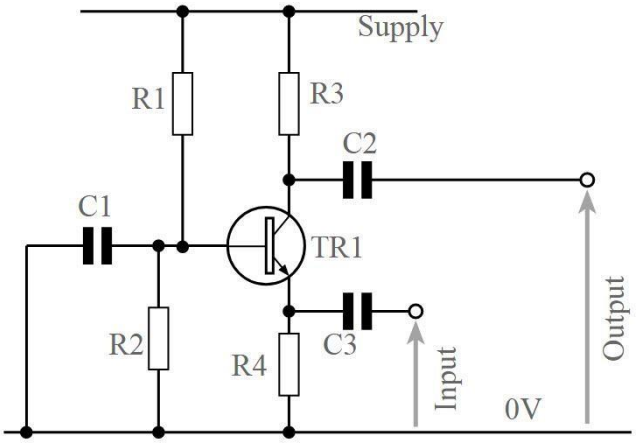
Diagram Source Elprocus

The below figure 2.4.4 shows how common base amplifier circuit is implemented.

Figure 2.4.4 Common Base Amplifier Circuit

Diagram Source Elprocus

www.binils.com



The biasing constraints are same, but the applications of the signals are different. In this circuit, care has to be taken such that correct impedance match is provided to the input signal.

Download Binils Android App in playstore Download Photoplex

Characteristics of Common Base Amplifier Circuit

The following are the characteristics of the Common Base amplifier circuit.

- High voltage gain
- Low current gain
- Low power gain
- Input and output phase relation is 0o
- It has low input impedance
- It has high output impedance

Applications

The common base amplifier circuit is used, where the low input impedance is required.

The following are the applications of the common base amplifier circuit.

www.binils.com

- It is used in moving coil microphones Preamplifiers.
- It is used in UHF and VHF RF amplifiers.

Analysis of CC amplifiers using Hybrid π equivalent circuits

The amplifier is an electronic circuit that is used for amplifying a voltage or current signal. The input for the transistor will be a voltage or current and the output will be an amplified form of that input signal. An amplifier circuit is generally designed with one or more transistors is called a transistor amplifier. The transistor (BJT, FET) is a major component in an amplifier system. In this article, we will discuss the common-collector amplifier circuit. The Transistor amplifiers are most commonly using in our day to day life applications like an audio amplifier, Radio Frequency, audio tuners, Optical fiber communication, etc.

Common Collector/ Emitter Follower Transistor Amplifier Basics

There are three transistor configurations that are used commonly for signal amplification i.e. common base (CB), common collector (CC) and common emitter (CE). Good transistor amplifiers essentially have the following parameters high gain, high input impedance, high bandwidth, high slew rate, high linearity, high efficiency, high stability, etc. In the Common Collector transistor configuration, we use the collector terminal as common for both input and output signals. This configuration is also known as emitter follower configuration because the emitter voltage follows the base voltage. The emitter follower configuration is mostly used as a voltage buffer. These configurations are widely used in impedance matching applications because of their high input impedance.

www.binils.com

Common collector amplifiers have the following circuit configurations.

- The input signal enters the transistor at the base terminal
- The input signal exits the transistor at the emitter terminal
- The collector is connected to a constant voltage, i.e. ground, sometimes with an intervening resistor

A simple common-collector amplifier circuit is shown in the figure 2.3.1 below. The collector resistor Rc is unnecessary in many applications. In order to work transistor as an amplifier, it should be in the active region of its configuration.

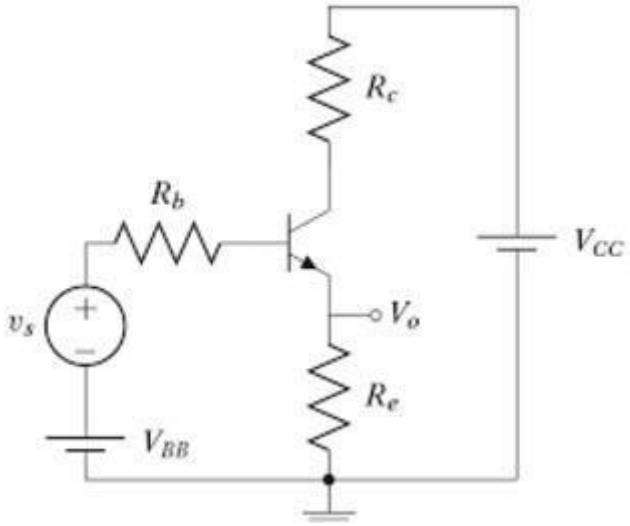


Figure 2.3.1 Common Collector Amplifier or Emitter Follower Circuit

Diagram Source Elprocus

www.binils.com

For that we set the quiescent point need to be set with the circuitry external to the transistor, the values of resistors Rc and Rb, and the DC voltage sources, Vcc and Vbb, have chosen accordingly.

Once the circuit quiescent conditions have been calculated and it has been determined that the BJT is in the forward- active region of operation, the h-parameters are calculated below to form the small-signal model of the transistor.

$$h_{fe} = \beta_F \qquad h_{oe} = \frac{I_C}{V_A} \approx 0.$$

$$h_{ie} = (\beta_F + 1)\left|\frac{\eta V_t}{I_C}\right|.$$

Common Collector Transistor Amplifier Characteristics

The load resistor in the common collector amplifier being placed in series with the emitter circuit receives both the base current and collector currents. Since the emitter of a transistor is the sum of base and collector currents, since base and collector

currents always add together to form the emitter current, it would be reasonable to assume that this amplifier will have a very large current gain. The common-collector amplifier has quite large current gain, larger than any other transistor amplifier configuration. The characteristics of cc amplifier as mentioned below.

Parameter	**Characteristics**
Voltage gain	Zero
Current gain	High
Power gain	Medium
Input or output phase relationship	Zero degree
Input resistance	High
Output resistance	Low

www.binils.com

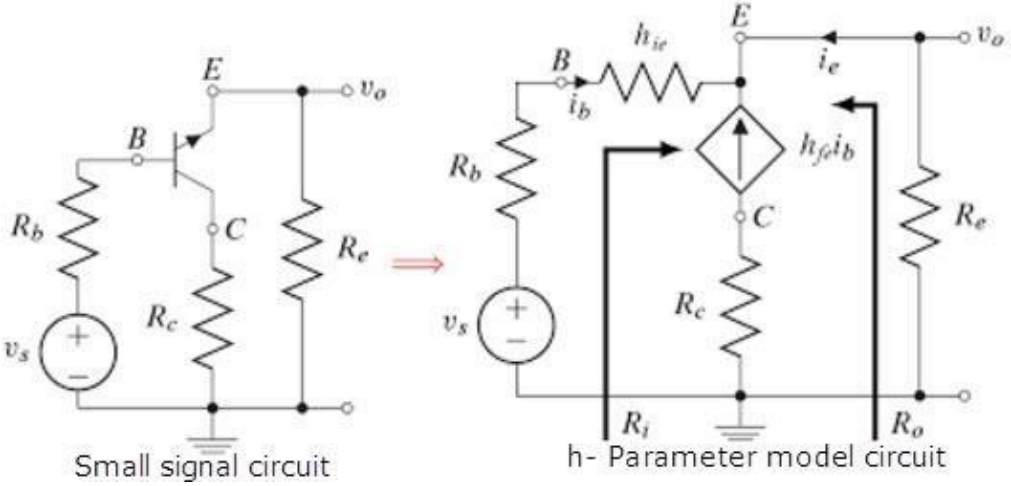


Figure 2.3.2 AC Modeling of Common Collector Amplifier

Diagram Source Elprocus

Current gain

The current gain is defined as the ratio of the load current to the input current.

$$Ai = i_l/i_b = -ie/ib$$

From the h-parameter circuit, it can be determined that the emitter and base currents are related through the dependent current source by the constant hfe+1. The current gain is dependent only on the BJT characteristics and independent of any other circuit element values. Its value is given by

This result is identical to that for a common emitter amplifier with an emitter resistor. The input resistance to a common collector amplifier is large for typical values of the load resistance Re.

Voltage Gain

The voltage gain is the ratio of output voltage to input voltage. If the input voltage is again taken to be the voltage at the input to the transistor, Vb.

www.binils.com

Input Resistance

The input resistance is given by

$$Av = Vo/Vb$$

$$R_i \equiv \frac{v_b}{i_b} = \frac{h_{ie}i_b + R_e(i_b + h_{fe}i_b)}{i_b} = h_{ie} + (h_{fe} + 1)R_e \quad {}_{7b})$$

Replacing each term with its equivalent expression

$$Av = (Re)(Ai)(1/Ri)$$

$$A_V = (R_e)(A_I)\left(\frac{1}{R_i}\right) = \frac{(h_{fe} + 1)R_e}{h_{ie} + (h_{fe} + 1)R_e}.$$

The above equation is somewhat less than unity. The approximation equation of voltage gain is given by

The overall voltage gain can be defined as

Output Resistance

The output resistance is defined as the Thevenin resistance at the output of the amplifier looking back into the amplifier. The circuit is shown below FIGURE 2.3.3, the AC equivalent circuit to calculate the output resistance.

$$A_{vs} = Vo/Vs$$

This ratio can be directly derived from the voltage gain Av, and a voltage division between the source resistance Rs and the amplifier input resistance Ri

$$A_{VS} = \frac{v_o}{v_s} = \left(\frac{v_o}{v_b}\right)\left(\frac{v_b}{v_s}\right) = A_V\left(\frac{R_i}{R_i + R_b}\right)$$

After substitutions of appropriate equations, the overall voltage gain is given by

$$A_{vs} = 1 - (h_{ie}+R_b)/(R_i+R_b)$$

www.binils.com

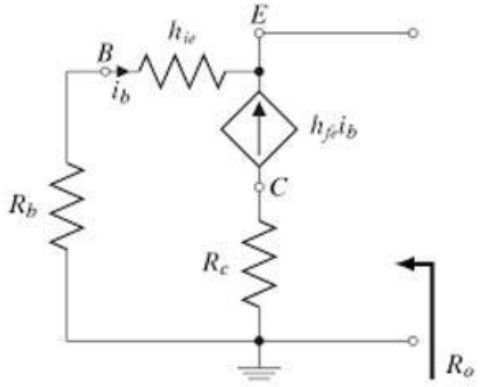


Figure 2.3.3 Common Collector Amplifier Output Resistance AC Equivalent Circuit

Diagram Source Elprocus

If a voltage v is applied to the output terminals, the base current is found to be

$$ib = -v/(Rb+hie)$$

The total current flowing into the BJT is given by

$$i = -ib-hfe.ib$$

the output resistance is calculated as

$$Ro = v/i = (Rb+hie)/(hfe+1)$$

The output resistance for a common collector transistor amplifier is typically small.

Applications

This amplifier is used as an impedance matching circuit.

It is used as a switching circuit.

The high current gain combined with near-unity voltage gain makes this circuit a great voltage buffer

It is also used for circuit isolation.

www.binils.com

Common Emitter Amplifier Circuit

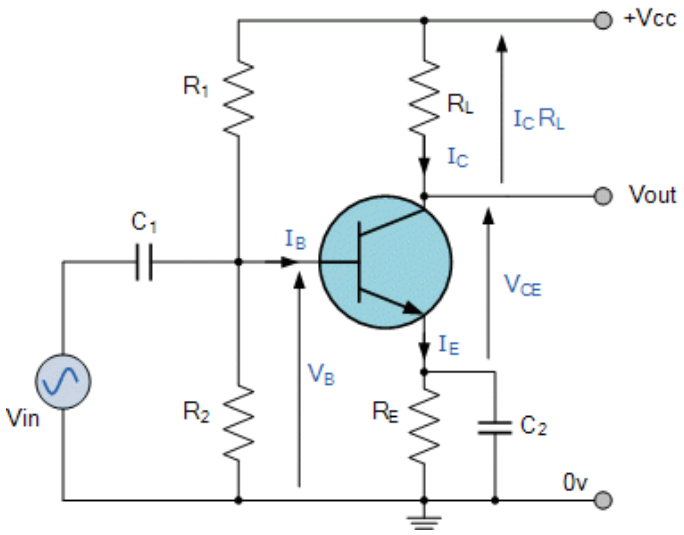


Figure 2.2.1 Practical common-emitter amplifier circuit

Diagram Source Electronic Tutorials

From above circuit, it consists of different circuit components. The functions of these components in figure 2.2.1 are as follows:

www.binils.com

1. Biasing Circuit:

Resistors R_1, R_2 and R_E forms the voltage divider biasing circuit for CE amplifier and it sets the proper operating point for CE amplifier.

2. Input Capacitor C_1:

C_1 couples the signal to base of the transistor. It blocks any D.C. component present in the signal and passes only A.C. signal for amplification.

3. Emitter Bypass Capacitor C_E:

C_E is connected in parallel with emitter resistance R_E to provide a low reactance path to the amplified A.C. This will reduce the output voltage and reducing the gain value.

4. Output Coupling Capacitor C_2:

C_2 couples the output of the amplifier to the load or to the next stage of the amplifier. It blocks D.C. and passes only A.C. part of the amplified signal.

Need for C_1, C_2, and C_E:

The impedance of the capacitor is given by,

$$X_C = 1/ (2\prod f_c)$$

Phase reversal:

The phase relationship between the input and output voltages can be determined by considering the effect of positive and negative half cycle separately. The collector current is β times the base current, so the collector current will also increases. This increases the voltage drop across R_C.

$$V_C = V_{CC} - I_C R_C$$

Increase in I_C results in a drop in collector voltage V_C, as V_{CC} is constant. V_i increases in a positive direction, V_o goes in negative direction and negative half cycle of output voltage can be obtained for positive half cycle at the input.

www.binils.com

In negative half cycle of input, A.C. and D.C. voltage will oppose each other. This will reduce the base current. Accordingly collector current and drop across R_C both will reduce and it increases the output voltage. So positive half cycle at the output for negative half cycle at the input can be obtained. So there is a phase shift of 180º between input and output voltages for a common emitter amplifier.

Common Emitter Voltage Gain

The Voltage Gain of the common emitter amplifier is equal to the ratio of the change in the input voltage to the change in the amplifiers output voltage. Then ΔV_L is Vout and ΔV_B is Vin. But voltage gain is also equal to the ratio of the signal resistance in the Collector to the signal resistance in the Emitter and is given as:

$$\text{Voltage Gain} = \frac{\text{Vout}}{\text{Vin}} = \frac{\Delta V_L}{\Delta V_B} = -\frac{R_L}{R_E}$$

Common Emitter Amplifier analysis

The first step in AC analysis of Common Emitter amplifier circuit is to draw the AC equivalent circuit by reducing all DC sources to zero and shorting all the capacitors. The below figure2.2.2 shows the AC equivalent circuit.

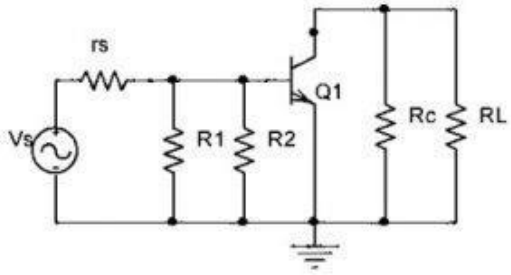


Figure 2.2.2 AC Equivalent Circuit for CE Amplifier

Diagram Source Electronic Tutorials

www.binils.com

The next step in the AC analysis is to draw an h-parameter circuit by replacing the transistor in the AC equivalent circuit with its h-parameter model. The below figure 2.2.3 shows the h-parameter equivalent circuit for the CE circuit.

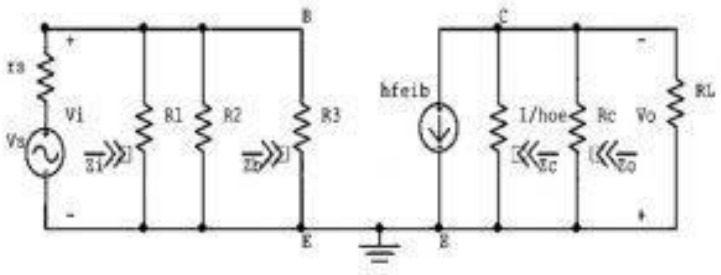


Figure 2.2.3 h**-Parameter Equivalent Circuit for Common Emitter Amplifier**

Diagram Source Electronic Tutorials

The typical CE circuit performance is summarised below:

Device input impedance, Zb = hie

Circuit input impedance, Zi = R1 || R2 || Zb

Device output impedance, Zc= 1/hoe

Circuit output impedance, Zo = RC || ZC ≈ RC

Circuit voltage gain, Av = -hfe/hie*(Rc|| RL)

Circuit current gain, AI = hfe. RC. Rb/ (Rc+RL) (Rc+hie)

Circuit power gain, Ap = Av * Ai

CE Amplifier Frequency Response

The voltage gain of a CE amplifier varies with signal frequency. It is because the reactance of the capacitors in the circuit changes with signal frequency and hence affects the output voltage. The curve drawn between voltage gain and the signal frequency of an amplifier is known as frequency response. The below figure shows the frequency response of a typical CE amplifier.

www.binils.com

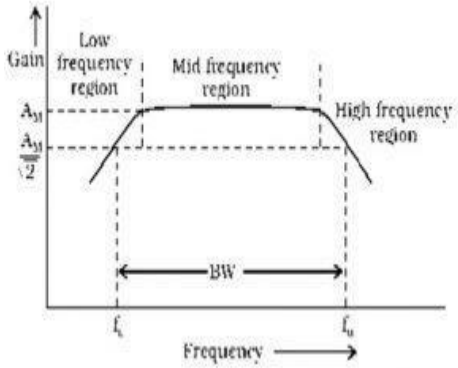


Figure 2.2.4 Frequency Response

Diagram Source Electronic Tutorials

From the above figure 2.2.4, we observe that the voltage gain drops off at low (< FL) and high (> FH) frequencies, whereas it is constant over the mid-frequency range (FL to FH).

At Low Frequencies (< FL)

The reactance of coupling capacitor C2 is relatively high and hence very small part of the signal will pass from the amplifier stage to the load. Moreover, CE cannot

shunt the RE effectively because of its large reactance at low frequencies. These two factors cause a drops off of voltage gain at low frequencies.

At High Frequencies (> FH)

The reactance of coupling capacitor C2 is very small and it behaves as a short circuit. This increases the loading effect of the amplifier stage and serves to reduce the voltage gain. Moreover, at high frequencies, the capacitive reactance of base-emitters junction is low which increases the base current. This frequency reduces the current amplification factor β. Due to these two reasons, the voltage gain drops off at a high frequency.

At Mid Frequencies (FL to FH)

The voltage gain of the amplifier is constant. The effect of the coupling capacitor C2 in this frequency range is such as to maintain a constant voltage gain. Thus, as the frequency increases in this range, the reactance of CC decreases, which tends to increase the gain.

www.binils.com

However, at the same time, lower reactance means higher almost cancel each other, resulting in a uniform fair at mid-frequency.

We can observe the frequency response of any amplifier circuit is the difference in its performance through changes within the input signal's frequency because it shows the frequency bands where the output remains fairly stable. The circuit bandwidth can be defined as the frequency range either small or big among fH & fL. So from this, we can decide the voltage gain for any sinusoidal input in a given range of frequency. The frequency response of a logarithmic presentation is the Bode diagram. Most of the audio amplifiers have a flat frequency response that ranges from 20 Hz – 20 kHz. For an audio amplifier, the frequency range is known as Bandwidth. Frequency points like fL & fH are related to the lower corner & the upper corner of the amplifier which are the gain falls of the circuits at high as well as low frequencies.

These frequency points are also known as decibel points. So the BW can be defined as

$$\mathbf{BW = f_H - f_L}$$

The dB (decibel) is 1/10th of a B (bel), is a familiar non-linear unit to measure gain & is defined like 20log10(A). Here 'A' is the decimal gain which is plotted over the y-axis.The maximum output can be obtained through the zero decibels which communicate toward a magnitude function of unity otherwise it occurs once Vout = Vin when there is no reduction at this frequency level, so

$$\mathbf{V_{OUT}/V_{IN} = 1,}$$

$$\mathbf{so\ 20log(1) = 0dB}$$

We can notice from the above graph, the output at the two cut-off frequency points will decrease from 0dB to -3dB & continues to drop at a fixed rate. This reduction within gain is known commonly as the roll-off section of the frequency response curve. In all basic filter and amplifier circuits, this roll-off rate can be defined as 20dB/decade, which is equal to a 6dB/octave rate. So, the order of the circuit is multiplied with these values.

www.binils.com

These -3dB cut-off frequency points will describe the frequency where the o/p gain can be decreased to 70 % of its utmost value. After that, we can properly say that the frequency point is also the frequency at which the gain of the system has reduced to 0.7 of its utmost value.

Common Emitter Transistor Amplifier

The circuit diagram of the common emitter transistor amplifier has a common configuration and it is a standard format of transistor circuit whereas voltage gain is desired. The common emitter amplifier is also converted as an inverting amplifier. The different types of configurations in transistor amplifiers are common base and the common collector transistor and the figure are shown in the following circuits.

Common Emitter Transistor Amplifier

Characteristics of Common Emitter Amplifier

The voltage gain of a common emitter amplifier is medium

The power gain is high in the common emitter amplifier

There is a phase relationship of 180 degrees in input and output

In the common emitter amplifier, the input and output resistors are medium.

The characteristics graph between the bias and the gain is shown in figure 2.2.5 below.

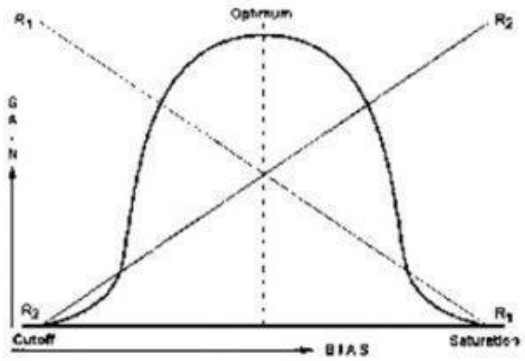


Figure 2.2.5 Characteristics Transistor Bias Voltage

Diagram Source Electronic Tutorials

www.binils.com

The Vcc (supply voltage) will determine the utmost Ic (collector current) once the transistor is activated. The Ib (base current) for the transistor can be found from the Ic (collector current) & the DC current gain β (Beta) of the transistor.

VB = VCC R2/R1+R2

Sometimes, 'β' is referred to as 'hFE' which is the forward current gain of the transistor within the CE configuration. Beta (β) is a fixed ratio of the two currents like Ic and Ib, so it doesn't contain units. So a small change within the base current will make a huge change within the collector current.

The same type of transistors as well as their part number will contain huge changes within their 'β' values. For instance, the NPN transistor like BC107 includes a Beta value (DC current gain in between 110 – 450 based on the datasheet. So one transistor may include a 110 Beta value whereas another may include of 450 Beta

value, however, both the transistors are NPN BC107 transistors because Beta is a feature of the structure of the transistor but not of its function.

When the base or emitter junction of the transistor is connected forward bias, then the emitter voltage 'Ve' will be a single junction where voltage drop is dissimilar to the voltage of the Base terminal. The emitter current (Ie) is nothing but the voltage across the emitter resistor. This can be calculated simply through Ohm's Law. The 'Ic' (collector current) can be approximated, as it is approximately a similar value to the emitter current.

Input and Output Impedance of Common Emitter Amplifier

In any electronic circuit design, impedance levels are one of the main attributes that need to consider. The value of input impedance is normally in the region of 1kΩ, while this can differ significantly based on the conditions as well as values of the circuit. The less input impedance will result from the truth that the input is given across the two terminals of the transistor-like base & emitter because there is a forward-biased junction.

www.binils.com

Also, the o/p impedance is comparatively high because it varies significantly again on the values of selected electronic component values & allowed current levels. The o/p impedance is a minimum of 10kΩ otherwise possibly high. But if the current drain permits high levels of current to be drawn, then the o/p impedance will be decreased significantly. The impedance or resistance level comes from the truth that the output is used from the collector terminal because there is a reverse-biased junction.

Basic BJT differential pair

Transistorized Differential Amplifier

The transistorised differential amplifier basically uses the emitter biased circuits which are identical in characteristics. Such two identical emitter biased circuits are

Figure 2.10.1 Emitter Biased Circuits

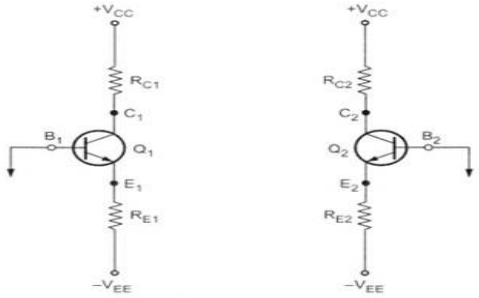


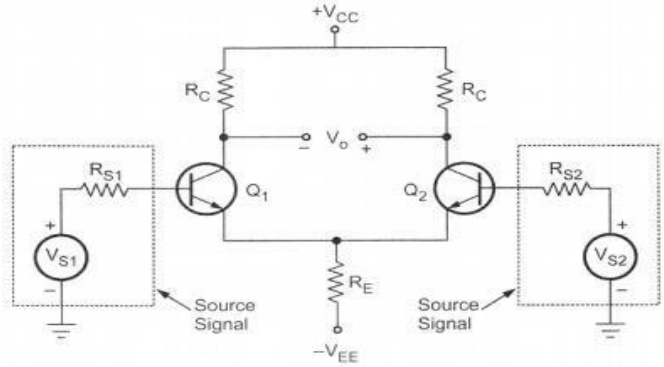
Diagram Source Electronic Tutorials

www.binils.com

The magnitudes of + Vcc and – V_{EE} are also same. The differential amplifier can be obtained by using such two emitter biased circuits. This is achieved by connecting emitter E1 of Q1 to the emitter E2 of Q2. Due to this, R_{E1} appears in parallel with R_{E2} and the combination can be replaced by a single resistance denoted as R_E. The base B_1 of Q1 is connected to the input 1 which is V_{S1} while the base B_2 of Q_2 is connected to the input 2 which is Vs2. The supply voltages are measured with respect to ground. The balanced output is taken between the collector C1 of Q1

and the collector C2 of Q_2. Such an amplifier is called emitter coupled differential amplifier. The two collector resistances are same hence can be denoted as R_C.

The output can be taken between two collectors or in between one of the two collectors and the ground. When the output is taken between the two collectors, none of them is grounded then it is called balanced output, double ended output or floating output. When the output is taken between any of the collectors and the ground, it is called unbalanced output or single ended output. The complete circuit diagram of such a



Dual input, balanced output differential amplifier

www.binils.com

Figure 2.9.2 Differential Amplifier Dual Input balanced differential Amplifier

Diagram Source Electronic Tutorials

As the output is taken between two output terminals, none of them is grounded, it is called balanced output differential amplifier. Let us study the circuit operation in the two modes namely

- Differential mode operation
- Common mode operation

1. Differential Mode Operation

In the differential mode, the two input signals are different from each other. Consider the two input signals which are same in magnitude but 180" out of phase. These signals, with opposite phase can be obtained from the center tap transformer. The circuit used in differential mode operation is shown in the Figure 2.9.3

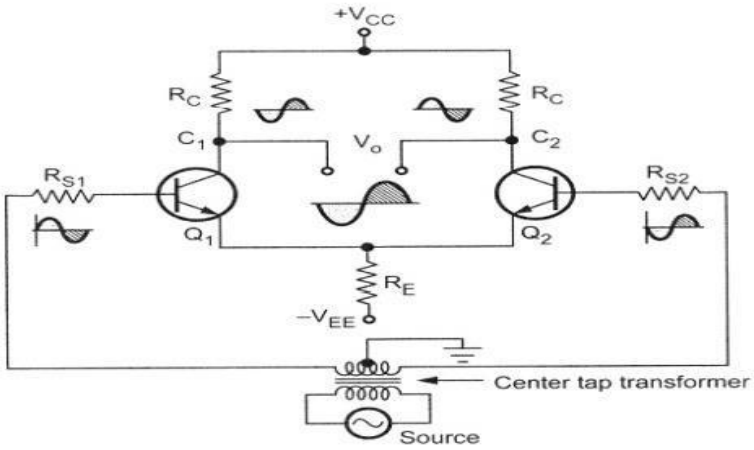


Figure 2.9.3 Differential Mode Operation

Diagram Source Electronic Tutorials

www.binils.com

Assume that the sine wave on the base of Q_1 is positive going while on the base of Q_2 is negative going. With a positive going signal on the base of Q_1, m amplified negative going signal develops on the collector of Q1. Due to positive going signal, current through R_E also increases and hence a positive going wave is developed across R_E. Due to negative going signal on the base of Q2, an amplified positive going signal develops on the collector of Q_2. And a negative going signal develops across R_E, because of emitter follower action of Q_2. So signal voltages across R_E, due to the effect of Q1 and Q2 are equal in magnitude and 180o out of phase, due to matched

pair of transistors. Hence these two signals cancel each other and there is no signal across the emitter resistance. Hence there is no a.c. signal current flowing through the emitter resistance. Hence R_E in this case does not introduce negative feedback. While Vo is the output taken across collector of Q1 and collector of Q_2.

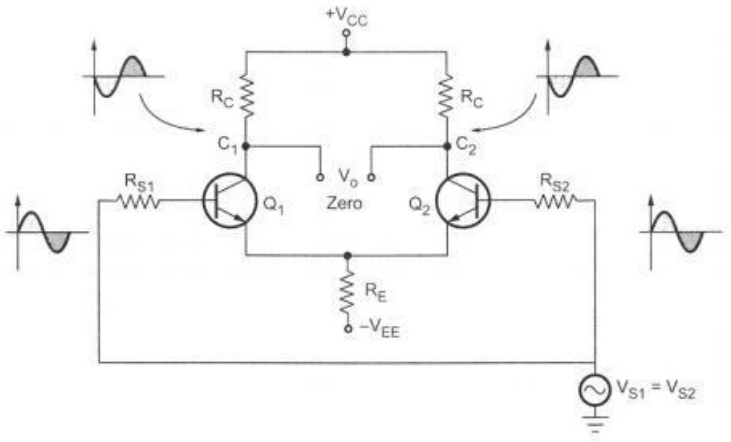
Hence the difference output Vo is twice as large as the signal voltage from either collector to ground

2. Common Mode Operation

In this mode, the signals applied to the base of Q1 and Q2 are derived from the same source. So the two signals are equal in magnitude as well as in phase. The circuit diagram is shown in the Figure 2.9.4. In phase signal voltages at the bases of Q1 and Q2 causes in phase signal voltages to appear across R_E, which add together. Hence R_E carries a signal current and provides a negative feedback. This feedback reduces the common mode gain of differential amplifier.

www.binils.com

Figure 2.9.4 Common Mode Operation



While the two signals causes in phase signal voltages of equal magnitude to appear across the two collectors of Q_1 and Q2. Now the output voltage is the difference between the two collector voltages, which are equal and also same in phase

Eg. (20) - (20) = 0. Thus the difference output Vo is almost zero, negligibly small. ideally it should be zero.

www.binils.com

Download Binils Android App in playstore

Download Photoplex

Cascaded Amplifiers

A cascade amplifier is a two-port network designed with amplifiers which are connected in series when every amplifier transmits its o/p to the second amplifiers input in a daisy chain. The problem in measuring the gain of the cascaded stage is the non-perfect coupling among two stages because of loading.

The two stages of cascaded CE (common-emitter) are shown in the following circuit. Here the voltage divider can be formed by using the input and output resistances of the first and next stage. The complete gain cannot be the result of the individual stages in Figure 2.7.1.

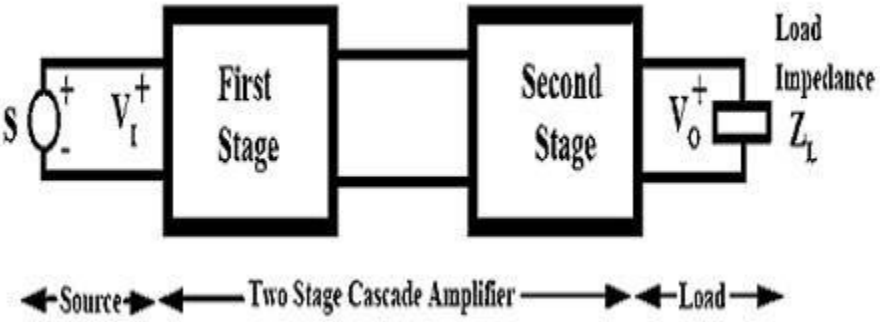


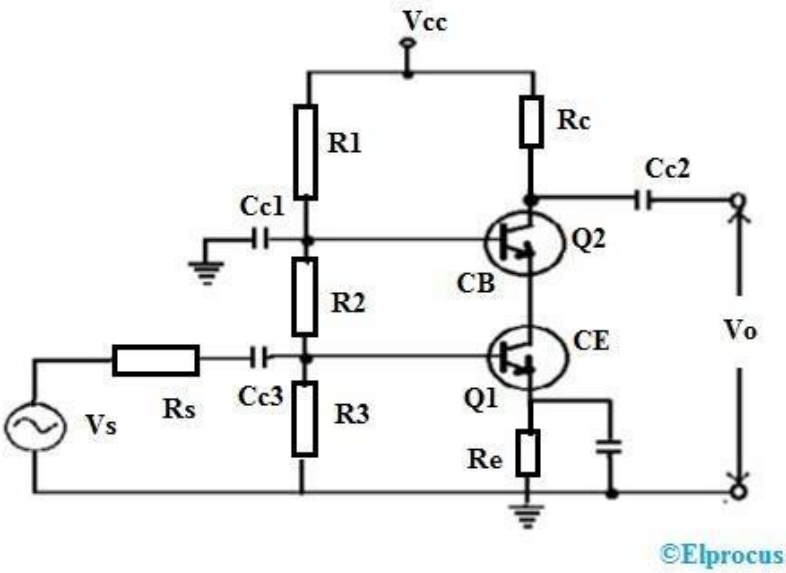
Figure 2.7.1 Two Stage Cascade Amplifier

Diagram Source Electronic Tutorials

Cascade Amplifier Circuit

The circuit diagram of cascade amplifier is shown below figure 2.7.2. The circuit can be designed with two configurations of a transistor namely CE (common-

emitter) and CB (common base). The CB (common base) configuration provides a good high-frequency operation.



cascade-amplifier-circuit

www.binils.com

Figure 2.7.2 Two Stage Cascade Amplifier

Diagram Source Electronic Tutorials

The current gain, as well as the i/p resistance of the cascade arrangement, is equivalent to the related value of a common emitter single-stage amplifier. The o/p resistance can be equivalent to the common base configuration in figure 2.7.2. The miller's capacitor shunting the common emitter input stage is extremely small.

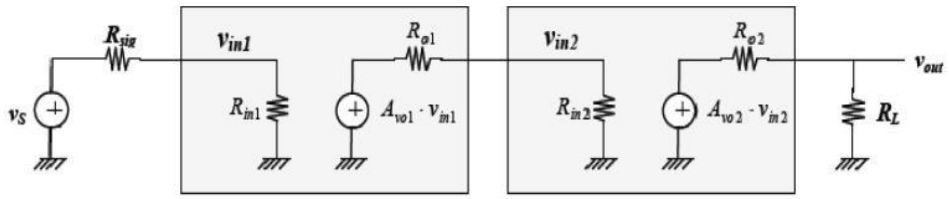


Fig3.20 small signal model of Cascaded ***Configuration of MOSFET***

Figure 2.7.3 Small Signal Model of Cascaded Configuration

Diagram Source Electronic Tutorials

$$A_{vo1} = -\frac{g_{m1} \cdot R_2}{1 + g_{m1} \cdot R_3}$$
$$A_{vo2} = g_{m2} \cdot R_4$$
$$R_{o1} = R_2$$
$$R_{o2} = R_4$$
$$R_{in1} = R_1$$
$$R_{in2} = \frac{1}{g_{m2}}$$

By grouping the different factors in this expression, we can find a physical interpretation for the cascading in figure 2.7.3. This physical interpretation can be used to guide simulation or analysis of the different stages separately, before combining them into a cascaded amplifier.

www.binils.com

$$\frac{v_{out}}{v_S} = \frac{v_1}{v_S} \cdot \frac{v_{out}}{v_2} = \underbrace{\left[\frac{R_{in1}}{R_{in1} + R_S} \cdot A_{vo1} \cdot \frac{R_{in2}}{R_{in2} + R_{o1}}\right]}_{\text{Gain of stage 1 with actual source and loaded by stage 2}} \cdot \underbrace{\left[A_{vo2} \cdot \frac{R_L}{R_L + R_{o2}}\right]}_{\text{Gain of stage 2 with ideal source and loaded by } R_L}$$

This amplifier is used to enhance the strength of a signal in a TV receiver. In this amplifier, the primary stage of the amplifier can be connected to the secondary stage of the amplifier. To build a practical electronic system, a single-stage amplifier is not enough. Even though the amplifier's gain mainly depends on parameters of the device as well as components of the circuit, there exists a higher limit of gain which can be attained from a single-stage amplifier. Therefore, the gain of this amplifier cannot be sufficient in practical application.

To conquer this trouble, we require this amplifier's two or more stages to amplify the overall amplifier's voltage gain. As above one stage is used within series it is named as a multi-stage amplifier. The main drawback of the cascade amplifier is when several stages increases then the bandwidth will decrease.

The applications of the cascade amplifier include the following.

www.binils.com

- This amplifier is used in tuned RF amplifiers within television circuits.
- This amplifier can also be used as a wideband amplifier.
- The isolation offered among input & output with these amplifiers is extremely high.

Configurations of Differential Amplifier

The differential amplifier, in the difference amplifier stage in the op-amp, can be used in four configurations :

- Dual input balanced output differential amplifier.
- Dual input, unbalanced output differential amplifier.
- Single input, balanced output differential amplifier.
- Single input, unbalanced output differential amplifier.

The differential amplifier uses two transistors in common emitter configuration. If output is taken between the two collectors it is called balanced output or double ended output. While if the output is taken between one collector with respect to ground it is called unbalanced output or single ended output. If the signal is given to both the input terminals it is called dual input, while if the signal is given to only one input terminal and other terminal is grounded it is called single input or single ended input. Out of these four configurations the dual input, balanced output is the basic differential amplifier configuration. This is shown in the Figure 2.11.1. (a). The dual input, unbalanced output differential amplifier is shown in the Figure 2.11.1.(b). The single input, balanced output differential amplifier is shown in the Figure 2.11.1 (c) and the single input, unbalanced output differential amplifier is shown in the Figure 2.11.1. (d).

www.binils.com

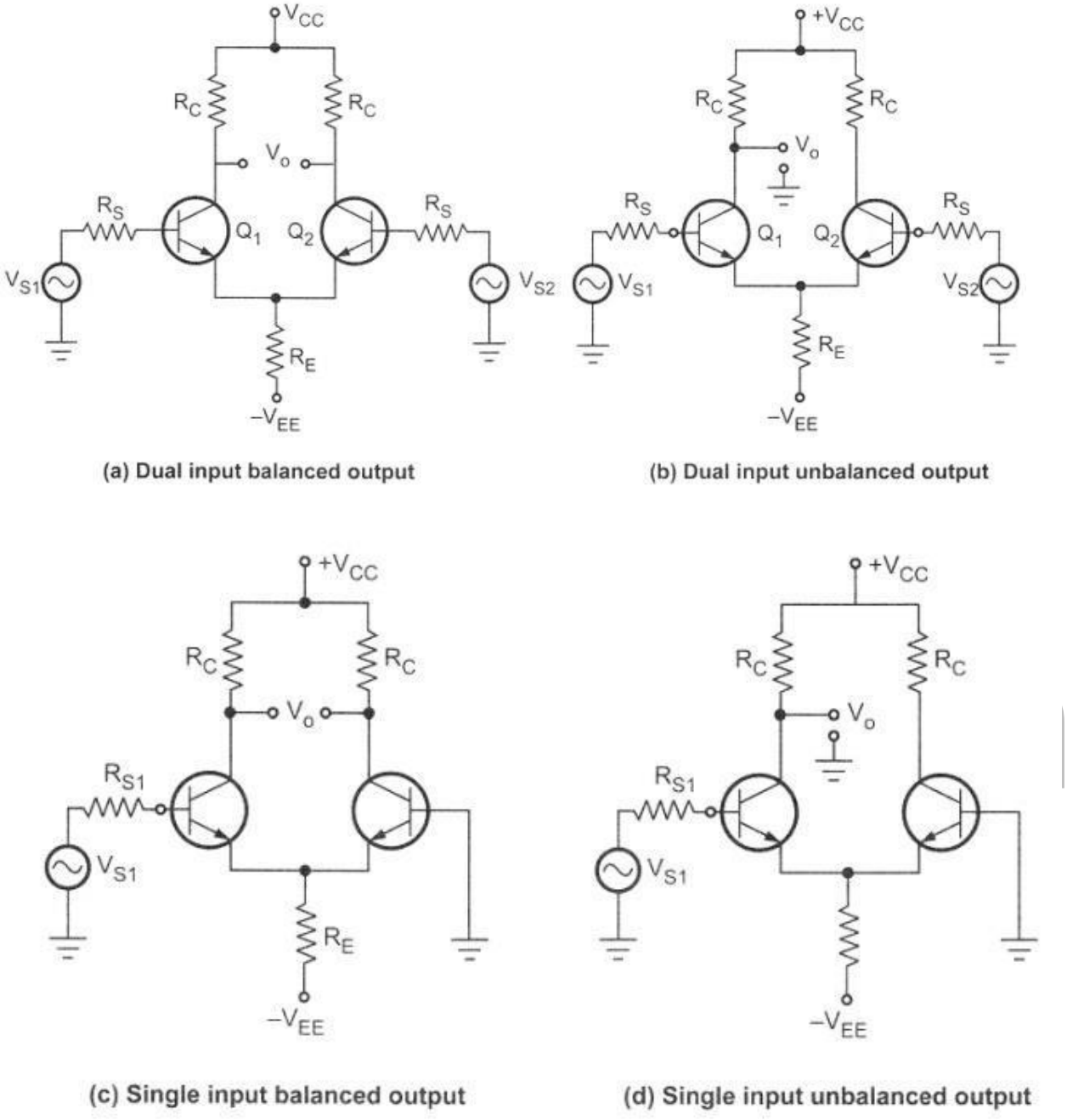


Figure 2.11.1 The dual input, unbalanced output differential amplifier is shown in the Fig.(b). The single input, balanced output differential amplifier is shown in the Fig (c) and the single input, unbalanced output differential amplifier is shown in the Fig. (d).

Diagram Source Electronic Tutorials

A.C. Analysis of Differential Amplifier using h-Parameters

In the a.c. analysis, we will calculate the differential gain A_d, common mode gain A_C, input resistance Ri and the output resistance R_0 of the differential amplifier circuit, using the h-parameters.

1. Differential Gain (A_d)

For the differential gain calculation, the two input signals must be different from each other. Let the two a.c. input signals be equal in magnitude but having 180" phase difference in between them. The magnitude of each a.c. input voltage V_{S1} and V_{S2}beVs /2. The two a.c. emitter currents I e_1 and I e_2 are equal in magnitude and 180' out of phase. Hence they cancel each other to get resultant a.c. current through the emitter as zero. For the a.c. purposes emitter terminal can be grounded.

The a.c. small signal differential amplifier circuit with grounded emitter terminal is shown in the Figure 2.11.2 As the two transistors are matched, the a.c. equivalent circuit for the other transistor is identical to the one shown in the Fig..1. Thus the circuit can be analyzed by considering only one transistor. This is called as half circuit concept of analysis. The approximate hybrid model for the above circuit can be shown as in the Fig.2, neglecting ho_e,

www.binils.com

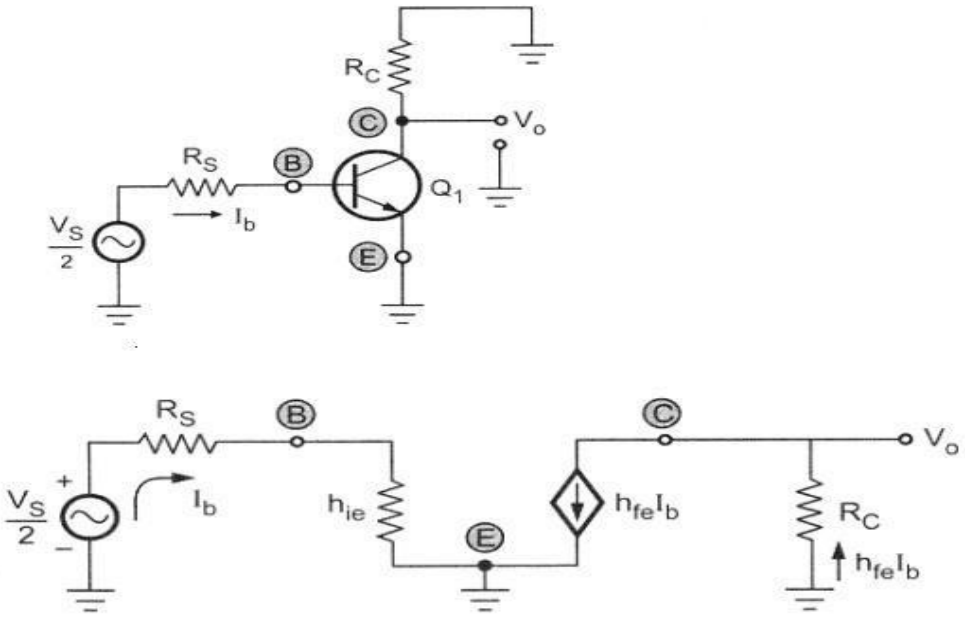


Figure 2.11.2 AC Equivalent for differential Operation and its hybrid

Diagram Source Electronic Tutorials

www.binils.com

Applying KVL to the input loop,

$$-I_b R_S - I_b h_{ie} + \frac{V_S}{2} = 0 \qquad \ldots(1)$$

$$-I_b(R_S + h_{ie}) = -\frac{V_S}{2}$$

$$I_b = \frac{V_S}{2(R_S + h_{ie})} \qquad \ldots(2)$$

Applying KVL to the output loop,

$$V_o = -h_{fe} I_b R_C \qquad \ldots(3)$$

Substituting equation (2) in equation (3),

$$V_o = -h_{fe} R_C \frac{V_S}{2(R_S + h_{ie})}$$

$$\boxed{\frac{V_o}{V_S} = \frac{-h_{fe} R_C}{2(R_S + h_{ie})}} \qquad \ldots(4)$$

The negative sign indicates the phase difference between input and output. Now two input signal magnitudes are V_S /2 but they are opposite in polarity, as 180" out of phase.

$$V_d = V_1 - V_2 = \frac{V_S}{2} - \left(-\frac{V_S}{2}\right) = V_S$$

The **magnitude** of the differential gain A_d is

$$\boxed{A_d = \frac{V_o}{V_S} = \frac{h_{fe} R_C}{2(R_S + h_{ie})}} \quad \text{(For unbalanced output)} \qquad \ldots(5)$$

where V_S = Differential input

the expression for A_d with balanced output changes as

$$A_d = 2 \times \frac{h_{fe} R_C}{2(R_S + h_{ie})}$$

$$A_d = \frac{h_{fe} R_C}{(R_S + h_{ie})} \text{ (magnitude)} \quad \ldots 6)$$

This is the differential gain for balanced output dual input differential amplifier circuit.

2. Common Mode Gain (A_C)

Let the magnitude of both the a.c. input signals be VS and are in phase with each other. Hence the differential input Vd = 0 while the common mode input Vc is the average value of the two.

$$V_c = \frac{V_1 + V_2}{2} = \frac{V_S + V_S}{2} \quad \ldots(7)$$

$$= V_S$$

the output can be expressed as

$$V_o = A_c V_S \quad \ldots (8)$$

$$A_c = \frac{V_o}{V_S} \quad \ldots(8\,(a))$$

But now both the emitter currents flows through R_E in the Same direction. Hence the total current flowing through R_E is $2I_e$. considering only one transistor, as in the figure 2.11.3

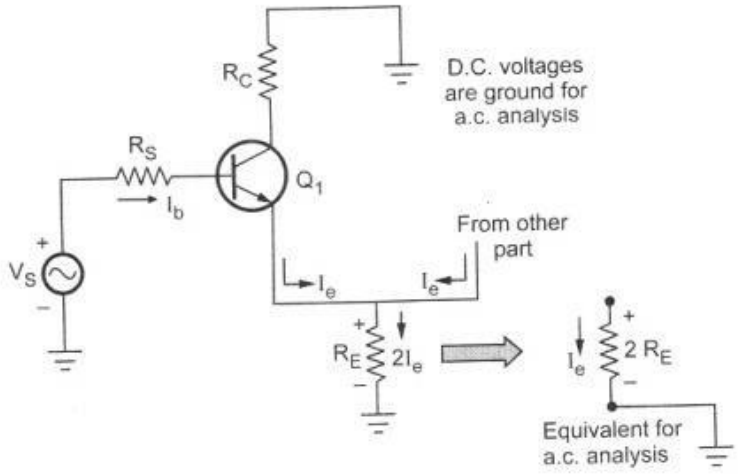


Figure 2.11.3 AC Equvalent for differential Operation and its hybrid model

Diagram Source Electronic Tutorials

www.binils.com

$$\therefore \quad -\frac{I_L}{h_{oe}} + \frac{h_{fe}}{h_{oe}} I_b - 2R_E I_L - 2R_E I_b - I_L R_C = 0$$

$$I_b \left[\frac{h_{fe}}{h_{oe}} - 2R_E\right] = I_L \left[\frac{1}{h_{oe}} + 2R_E + R_C\right]$$

$$I_b [h_{fe} - 2R_E h_{oe}] = I_L [1 + h_{oe} (2R_E + R_C)]$$

$$\frac{I_L}{I_b} = \frac{[h_{fe} - 2R_E h_{oe}]}{[1 + h_{oe} (2R_E + R_C)]} \qquad \ldots (10)$$

Substituting value of I_b, into the equation (8(b)), we get

$$V_S = \frac{I_L [1 + h_{oe} (2R_E + R_C)] (R_S + h_{ie} + 2R_E)}{[h_{fe} - 2R_E h_{oe}]} + I_L (2R_E)$$

$$\therefore \quad \frac{V_S}{I_L} = \frac{[1 + h_{oe} (2R_E + R_C)] (R_S + h_{ie} + 2R_E)}{[h_{fe} - 2R_E h_{oe}]} + (2R_E)$$

Download Binils Android App in playstore Download Photoplex

Finding L.C.M. and adjusting the terms, we get

$$\therefore \quad \frac{V_S}{I_L} = \frac{2R_E(1+h_{fe}) + R_S(1+2R_E h_{oe}) + h_{ie}(1+2R_E h_{oe}) + h_{oe} R_C [2R_E + R_S + h_{ie}]}{[h_{fe} - 2R_E h_{oe}]}$$

$$\therefore \quad \frac{V_S}{I_L} = \frac{2R_E(1+h_{fe}) + (R_S + h_{ie})(1+2R_E h_{oe}) + h_{oe} R_C [2R_E + R_S + h_{ie}]}{[h_{fe} - 2R_E h_{oe}]} \quad \ldots (11)$$

Neglecting the terms of $h_{oe} R_C$ as practically $h_{oe} R_C << 1$.

$$\therefore \quad \frac{V_S}{I_L} = \frac{2R_E(1+h_{fe}) + (R_S + h_{ie})(1+2R_E h_{oe})}{[h_{fe} - 2R_E h_{oe}]} \quad \ldots (12)$$

Substituting the value of I_L, in the equation (9)

$$V_o = \frac{-V_S(h_{fe} - 2R_E h_{oe}) R_C}{2R_E(1+h_{fe}) + (R_S + h_{ie})(1+2R_E h_{oe})}$$

Hence the common mode gain can be written as (absorbing negative sign),

$$A_c = \frac{V_o}{V_S} = \frac{(2R_E h_{oe} - h_{fe}) R_C}{2R_E(1+h_{fe}) + (R_S + h_{ie})(1+2R_E h_{oe})} \quad \ldots (13)$$

In practice h_{oe} is generally neglected hence the expression for A_c can be further modified as

$$\therefore \quad \boxed{A_c = \frac{-h_{fe} R_C}{R_S + h_{ie} + 2R_E(1+h_{fe})}} \quad \ldots (14)$$

Common Mode rejection Ratio (CMRR)

Once the differential and common mode gains are obtained, the expression for the CMRR can be obtained as,

$$\text{CMRR} = \left|\frac{A_d}{A_c}\right|$$

$$\therefore \quad \boxed{\text{CMRR} = \frac{R_S + h_{ie} + 2R_E(1 + h_{fe})}{(R_S + h_{ie})}} \qquad \ldots(15)$$

This is CMRR for ***dual input balanced output*** differential amplifier circuit.

www.binils.com

A Darlington transistor

If the Darlington pair consists of both PNP transistors, it makes PNP Darlington Transistor. And if the Darlington pair consists of both NPN transistors, it makes NPN Darlington Transistor.

A Darlington transistor (also known as a Darlington pair**)** is an electronics component made via the combination of two BJTs (Bipolar Junction Transistor) connected in such a way that it allows a very high amount of current gain. This is achieved through a compounding amplification, whereby the current is amplified by the first transistor and then further amplified by the second transistor. As this compound structure is designed from two BJTs, this transistor is also known as "Darlington Pair". This transistor behaves as a single unit transistor as it has only one emitter, collector, and base. The Darlington transistor was invented by Sidney Darlington in 1953.

www.binils.com

If the current gain of a transistor is β1 and β2, the overall current gain of Darlington pair is β1β2. The current gain of this transistor is very high compared to the normal transistor. Therefore, this transistor is also known as "Super Beta Transistor".

Darlington Transistor Circuit. The Darlington Transistor consists of two PNP transistors or NPN transistors connected back to back. It is a single package with a common collector terminal for both transistors. The Emitter terminal of the first transistor is connected with the base terminal of the second transistor.

Hence, the base supply is given only to the first transistor, and the output current is taken only from the second transistor. Therefore, it consists of only one base, emitter, and collector as shown in the below figure 2.6.1.

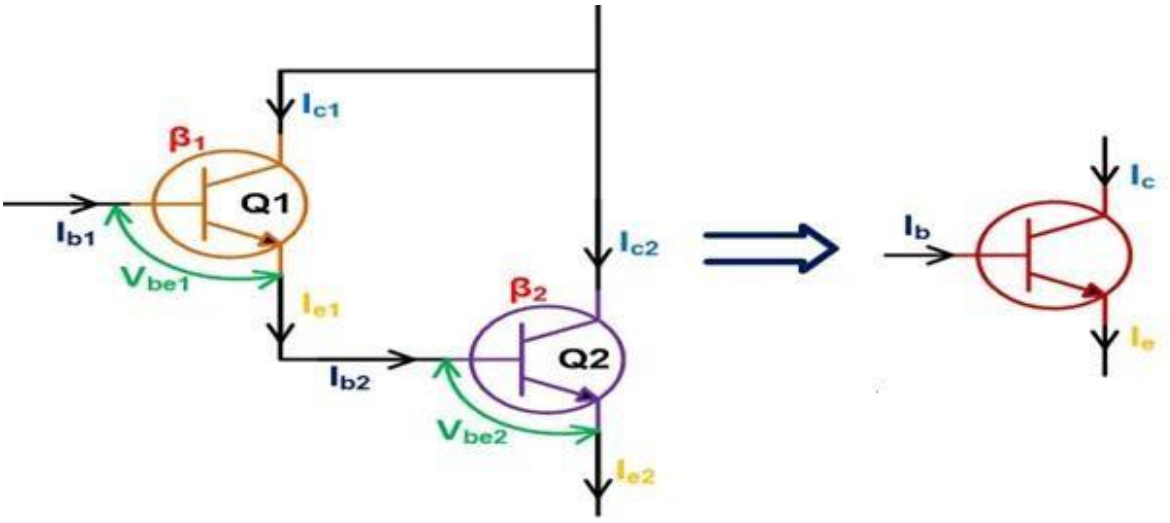


Figure 2.6.1 Darlington pair

Diagram Source Electronic Tutorials

There are two transistors Q1 and Q2.

I_{b1} = Base current of transistor Q1

I_{e1} = Emitter current of transistor Q1

I_{b2} = Base current of transistor Q2

I_{e2} = Emitter current of transistor Q2

In the above figure, two transistors are shown in one package. And from these two figures, the total base current (total input current) of the transistor package is equal to the base current of transistor Q1.

$$I_{b1} = I_b$$

Similarly, the total emitter current (total output current) of the package is equal to the emitter current of transistor Q2.

$$I_{C2} = I_C$$

www.binils.com

V_{be1} = base-emitter voltage of transistor Q1

V_{be2} = base-emitter voltage of transistor Q2

Total base-emitter voltage is a summation of the base-emitter voltage of both transistors.

$$V_{be}=V_{b1}+V_{b2}$$

www.binils.com

β_1 = Current gain of transistor Q1

β_2 = Current gain of transistor Q2

The total current gain of the Darlington Transistor is β_D. The total current gain of a transistor is the ratio of output current to the input current.

$$Current\ gain\ \beta_D = \frac{Output\ Current}{Input\ Current}$$

$$\beta_D = \frac{i_e}{i_b} = \frac{i_{e2}}{i_{b1}} \quad (1)$$

In transistor, the Emitter current is summation of base current and collector current. And the collector current is β times of base current. Hence, in general form of transistor,

$$i_e = i_c + i_b$$

$$i_e = \beta i_b + i_b$$

$$i_e = (\beta + 1) i_b \quad (2)$$

For transistor Q2,

$$i_{e2} = (\beta_2 + 1) i_{b2}$$

From equation-(1),

$$\beta_D = \frac{(\beta_2 + 1) i_{b2}}{i_{b1}}$$

From the circuit diagram, the emitter current of transistor Q1 is equal to the base current of transistor Q2.

$$i_{e1} = i_{b2}$$

$$\beta_D = \frac{(\beta_2 + 1) i_{e1}}{i_{b1}}$$

For transistor Q1,

$$i_{e1} = (\beta_1 + 1) i_{b1}$$

$$\beta_D = \frac{(\beta_2 + 1)(\beta_1 + 1) i_{b1}}{i_{b1}}$$

$$\beta_D = (\beta_2 + 1)(\beta_1 + 1)$$

$$\beta_D = \beta_1 \beta_2 + \beta_1 + \beta_2$$

In the above equation, the value of $\beta_1\beta_2$ is very large compared to the value of $\beta_1 + \beta_2$. Let's take an example in which, the β_1=100 and β_2=100.

In this condition, $\beta_1\beta_2$ = 10000 and $\beta_1+\beta_2$ = 200. Therefore, we can neglect the value of $\beta_1+\beta_2$. And the gain of Darlington Transistor is,

$$\beta_D = \beta_1 \beta_2$$

Advantages of Darlington Transistor

A Darlington transistor (i.e. a Darlington pair) has several advantages compared to the normal transistor. They have been summarized in the list below:

- The main advantage of a Darlington transistor is the high current gain. So, a small amount of base current can trigger the transistor.
- It offers high input impedance which translates into an equal decrease in output impedance.
- It is a single package. So, it is easy to configure on a circuit board or PCB compared to connect two different transistors.

Disadvantages of Darlington Transistor

The disadvantages of a Darlington transistor (i.e. a Darlington pair) have been summarized in the list below:

- It has a slow switching speed.
- The base-emitter voltage is almost two times compared to a normal transistor.
- Due to high saturation voltage, in such an application, it dissipates high power.
- The bandwidth is limited.
- The Darlington transistor introduces a phase shift at a certain frequency in the negative feedback circuit.

www.binils.com

Differential Amplifier

Introduction

A device which accepts an input signal and produces an output signal proportional to the input, is called an amplifier. An amplifier which amplifies the difference between.the two input signals is called differential amplifier. The differential amplifier configuration is used in variety of analog circuits. The.differential amplifier is an essential and basic building block in modern IC amplifier .The Integrated Circuit (IC) technology is well known now a days, due to which the design of complex circuits become very simple. The IC version of operational amplifier is inexpensive, takes up less space and consumes less power. The.differential amplifier is the basic building block of such IC operational amplifier.

Basics of Differential Amplifier

www.binils.com

The Differential Amplifier amplifies the difference between two input voltage signal. Hence it is also called as difference amplifier.

Consider an ideal differential amplifier shown in the Figure 2.9.1

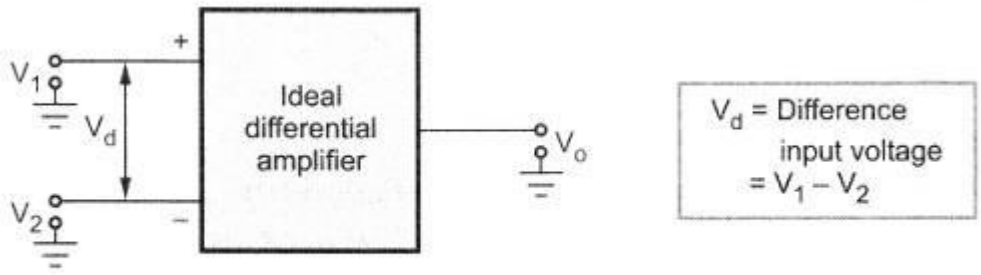


Fig. Ideal differential amplifier

Figure 2.9.1 Ideal Differential Amplifier

Diagram Source Electronic Tutorials

V_1 and V_2 are the two input signals while Vo is the output. Each signal is measured with respect to the ground.

In an ideal differential amplifier, the output voltage Vo is proportional to the difference between the two input signals. Hence we can write,

$$V_o \propto (V_1 - V_2) \quad \ldots(1)$$

Differential Gain A_d

From Equation 1 we can write,

$$\therefore \quad \boxed{V_o = A_d (V_1 - V_2)} \quad \ldots(2)$$

where A_D is the constant of proportionality. The A_D is the gain with which differential amplifier amplifies the difference between two input signals. Thus it is called differential gain of the differential amplifier.

Thus, Ad = Differential gain

www.binils.com

The difference between the two inputs (V_1 - V_2) is generally called difference voltage and denoted as Vd.

$$\boxed{V_o = A_d V_d} \quad \ldots(3)$$

Hence the differential gain can be expressed as,

$$A_d = \frac{V_o}{V_d} \quad \ldots(4)$$

Generally the differential gain is expressed in its decibel (dB) value as,

$$A_d = 20 \text{ Log}_{10} (A_d) \text{ in dB} \quad \ldots(5)$$

Common Mode Gain Ac

If we apply two input voltages which are equal in all the respects to the differential amplifier i.e. V1 = Vz then ideally the output voltage Vo = (V_1 - V_2) A_d, must be zero.But the output voltage of the practical differential amplifier not only depends on thedifference voltage but also depends on the average common level of the two inputs.

Such an average level of the two input signals is called common mode signal denoted as V_C

$$V_c = \frac{V_1 + V_2}{2} \quad ...(6)$$

` 1Practically, the differential amplifier produces the output voltage proportional to such common mode signal, also. The gain with which it amplifies the common mode signal to produce the output is called common mode gain of the differential amplifier $A_{C.\backslash}$

$$V_o = A_c V_c \quad ..(7)$$

Thus there exists some finite output for V1 = V2 due to such common mode gain $A_{C,}$ in case of practical differential amplifiers. So the total output of any differential amplifier can be expressed as,

$$V_o = A_d V_d + A_c V_c \quad ..(8)$$

For an ideal differential amplifier, the differential gain A_d, must be infinite while the common mode gain must be zero. But due to mismatch in the internal circuitry, there is some output available for $V_1 = V_2$ and gain A_C is not practically zero. The value of such common mode gain A_C very small while the value of the differential gain A_d is

www.binils.com

always very large.

www.binils.com

Common Mode Rejection Ratio (CMRR)

When the same voltage is applied to both the inputs, the differential amplifier is said to be operated in a common mode configuration. Many disturbance signals, noise signal appear as a common input signal to both the input terminals of the differential amplifier. Such a common signal should be rejected by the differential amplifier. The ability of a differential amplifier to reject a common mode signal is expressed by a ratio called common mode rejection ratio denoted as CMRR. It is defined as the ratio of the differential voltage gain A_d to common mode voltage gain A_C

$$\text{CMRR} = \rho = \left|\frac{A_d}{A_c}\right| \quad \ldots.(9)$$

$$\text{CMRR in dB} = 20 \log \left|\frac{A_d}{A_c}\right| \text{dB} \quad \ldots.(10)$$

www.binils.com

D.C. Analysis of Differential Amplifier

The d.c. analysis means to obtain the operating point values i.e. I_{CQ} and V_{CEQ} for the transistors used. The supply voltages are d.c. while the input signals are a.c., so d.c equivalent circuit can be obtained simply by reducing the input a.c. signals to zero. The d.c. equivalent circuit thus obtained is shown in the Figure 2.9.2. Assuming $Rs_1 = R_{S2}$, the source resistance is simply denoted by Rs ,

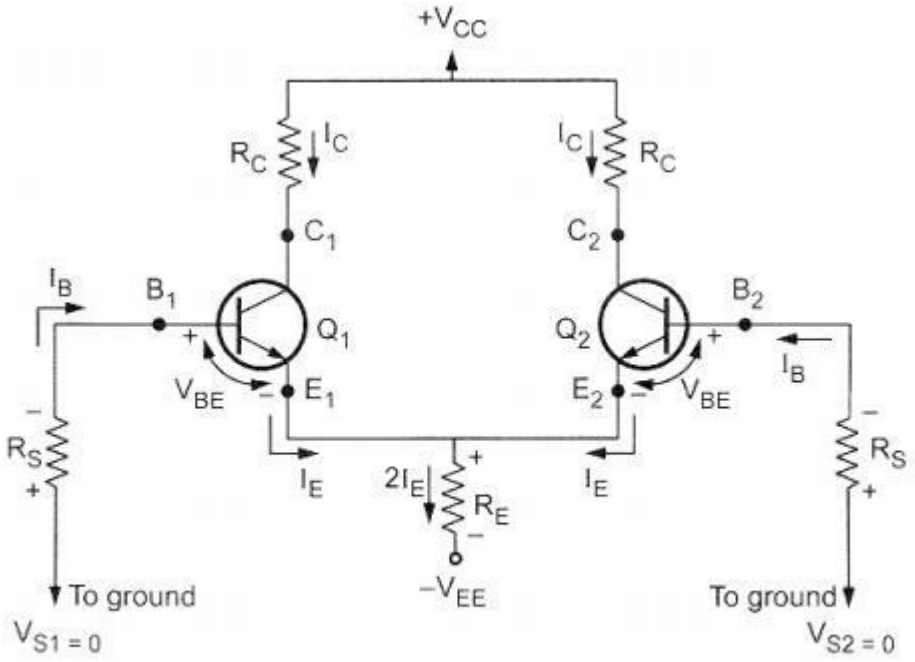


Fig. D.C. equivalent circuit

www.binils.com

Figure 2.9.2 DC Equivalent Circuit

Diagram Source Electronic Tutorials

The transistors Q1 and Q_2 are matched transistors and hence for such a matched pair we can assume :

i) Both the transistors have the same characteristics.

ii) $R_{E1} = R_{E2}$ hence $R_E = R_{E1} \| R_{E2}$.

iii) $R_{C1} = R_{c2}$ hence denoted as R_C.

iv) $|V_{CC}| = |V_{EE}|$ and both are measured with respect to ground.

As the two transistors are matched and circuit is symmetrical, it is enough to find out operating point I_{CQ} and V_{CEQ}, for any one of the two transistors. The same is applicable for the other transistor.

Apply-g KVL to base-emitter loop of the transistor Q1

$$-I_B R_S - V_{BE} - 2I_E R_E + V_{EE} = 0 \quad \ldots(1)$$

$I_C = \beta I_B$ and $I_C \cong I_E$

$$I_B = \frac{I_E}{\beta} \quad \ldots(2)$$

Substituting in equation (1), we get

$$\frac{-I_E R_S}{\beta} - V_{BE} - 2I_E R_E + V_{EE} = 0 \quad \ldots(3)$$

$$I_E \left[\frac{-R_S}{\beta} - 2R_E\right] + V_{EE} - V_{BE} = 0 \quad \ldots(4)$$

www.binils.com

$$I_E = \frac{V_{EE} - V_{BE}}{\frac{R_S}{\beta} + 2R_E} \quad \ldots(5)$$

V_{BE} = 0.6 to 0.7 V for silicon

= 0.2 V for germanium transistors.

In practice, generally $\frac{R_S}{\beta} << 2R_E$

$$I_E = \frac{V_{EE} - V_{BE}}{2R_E} \quad \ldots(6)$$

Now let us determine V_{CE}. As I_E is known and $I_E \cong I_C$, we can determine the collector voltage of Q_1 as

$$V_C = V_{CC} - I_C R_C \quad \ldots(7)$$

Neglecting the drop across R_S, we can say that the voltage at the emitter of Q_1 is approximately equal to $-V_{BE}$. Hence the collector to emitter voltage is

$$V_{CE} = V_C - V_E = (V_{CC} - I_C R_C) - (-V_{BE})$$

$$V_{CE} = V_{CC} + V_{BE} - I_C R_C \quad \ldots(8)$$

Hence $I_E = I_C = I_{CQ}$ while $V_{CE} = V_{CEQ}$ for given values of V_{CC} and V_{EE}.

Thus for both the transistors, we can determine operating point values, using equations (6) and (8) With the same biasing arrangement, the d.c. analysis remains same for all the four possible configurations of differential amplifier.

$$I_E = \frac{V_{EE} - V_{BE}}{\frac{R_s}{\beta} + 2R_E} \approx \frac{V_{EE} - V_{BE}}{2R_E} \approx I_{CQ}$$

$$V_{CEQ} = V_{CC} + V_{BE} - I_{CQ}R_C$$

www.binils.com

UNIT II

BJT AMPLIFIERS

Small Signal Hybrid π equivalent circuit of BJT

BJT circuit models

- Small signal model (hybrid pi model)
- Large signal model (Charge control model)
- SPICE model

A large variety of bipolar junction transistor models have been developed. One distinguishes between small signal and large signal models. We will discuss here first the hybrid pi model, a small signal model, which lends itself well to small signal design and analysis. The next model is the charge control model, which is particularly well suited to analyze the large-signal transient behavior of a bipolar transistor. And we conclude with the derivation of the SPICE model parameters.

www.binils.com

Small signal model (hybrid pi model)

The hybrid pi model of a BJT is a small signal model, named after the "p"-like equivalent circuit for a bipolar junction transistor. The model is shown in Figure 2.1.1. It consists of an input impedance, r_p, an output impedance r_0, and a voltage controlled current source described by the transconductance, g_m. In addition it contains the base-emitter capacitances, the junction capacitance, $C_{j,BE}$, and the diffusion capacitance, $C_{d,BE}$, and the base-collector junction capacitance, $C_{j,BC}$, also referred to as the Miller capacitance

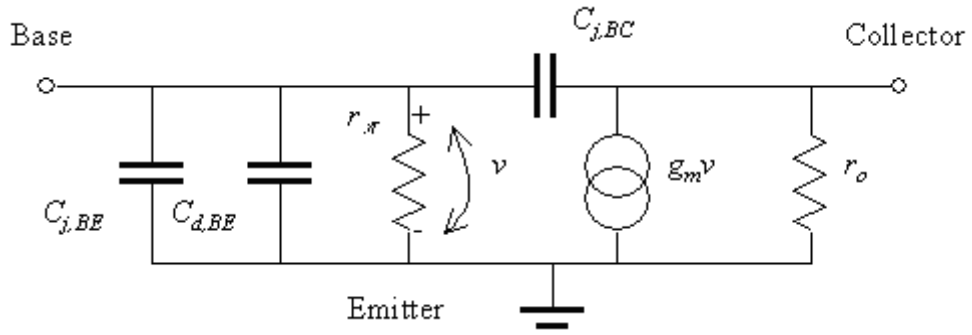


Figure 2.1.1 Small signal model (hybrid pi model) of a bipolar junction transistor.

Diagram Source Electronic Tutorials

The transconductance, g_m, of a bipolar transistor is defined as the change in the collector current divided by the change of the base-emitter voltage.

$$g_m \triangleq \frac{\partial I_C}{\partial V_{BE}} = \frac{I_C}{nV_t}$$

The base input resistance, r_p, is defined as the change of the emitter-base voltage divided by the change of the base current.

$$r_\pi \triangleq \frac{\partial V_{BE}}{\partial I_B} = \beta \frac{\partial V_{BE}}{\partial I_C} = \frac{\beta}{g_m} = \frac{nV_t}{I_B}$$

The output resistance, r_o, is defined as:

$$r_o \triangleq \frac{\partial V_{CE}}{\partial I_C} \cong \frac{\partial V_{CB}}{\partial I_C} = \frac{|V_A|}{I_C}$$

Introduction BJT Amplifiers

An amplifier is used to increase the signal level. It is used to get a larger signal output from a small signal input. Assume a sinusoidal signal at the input of the amplifier. At the output, signal must remain sinusoidal in waveform with frequency same as that of input. To make the transistor work as an amplifier, it is to be biased to

operate in active region. It means base-emitter junction is forward biased and base-collector junction is reverse biased. Let us consider the common emitter amplifier circuit using voltage divider bias.

In the absence of input signal, only D.C. voltage is present in the circuit. It is known as zero signal or no signal condition or quiescent condition. D.C. collector-emitter voltage V_{CE}, D.C. collector current I_C and base current I_B is the quiescent operating point for the amplifier. Due to this base current varies sinusoidaly , I_{BQ} is quiescent DC base current If the transistor is biased to operate in active region, output is linearly proportional to the input.

The collector current is β times larger than the input base current in CE configuration. The collector current will also vary sinusoidal about its quiescent value I_{CQ}. The output voltage will also vary sinusoidal.

EARLY Effect (Base-width modulation)

www.binils.com

As the voltages applied to the base-emitter and base-collector junctions are changed, the depletion layer widths and the quasi-neutral regions vary as well. This causes the collector current to vary with the collector-emitter voltage as illustrated in Figure 2.1.2

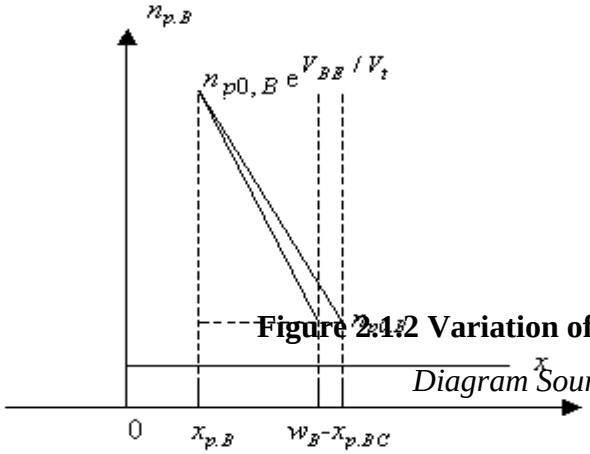


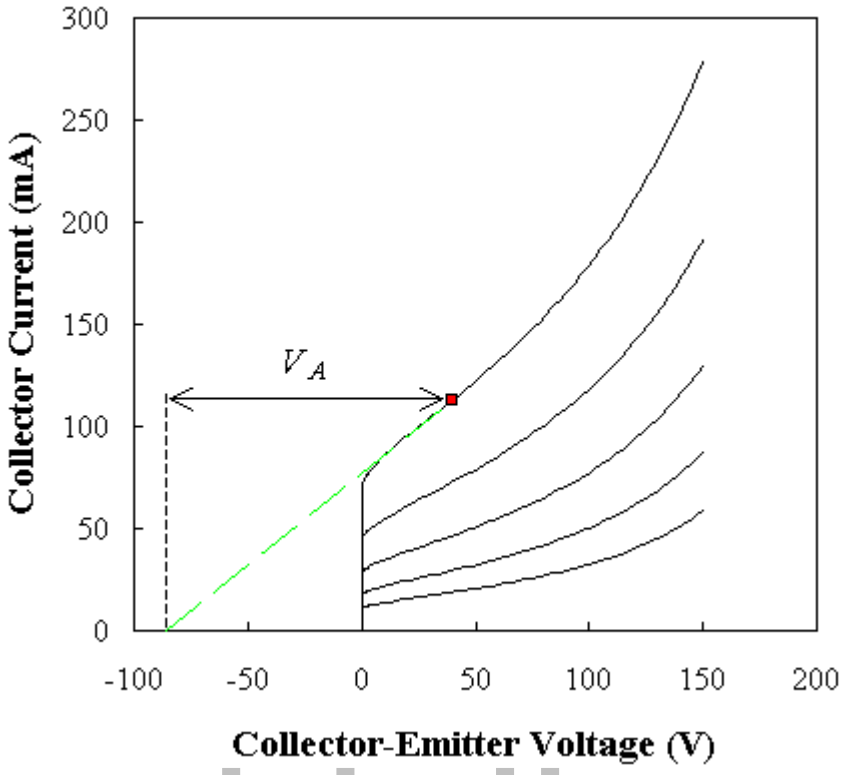
Figure 2.1.2 Variation of the minority-carrier distribution

Diagram Source Electronic Tutorials

A variation of the base-collector voltage results in a variation of the quasi-neutral width in the base. The gradient of the minority-carrier density in the base therefore changes, yielding an increased collector current as the collector-base current is increased. This effect is referred to as the Early effect. The Early effect is observed as an increase in the collector current with increasing collector-emitter voltage .The Early voltage, VA, is obtained by drawing a line tangential to the transistor I-V characteristic at the point of interest. The Early voltage equals the horizontal distance between the point chosen on the I-V characteristics in the figure 2.1.3.

A variation of the base-collector voltage results in a variation of the quasi-neutral width in the base. The gradient of the minority-carrier density in the base therefore changes, yielding an increased collector current as the collector-base current is increased. This effect is referred to as the Early effect. The Early effect is observed as an increase in the collector current with increasing collector-emitter voltage as illustrated with Figure 2.1.3. The Early voltage, VA, is obtained by drawing a line tangential to the transistor I-V characteristic at the point of interest. The Early voltage equals the horizontal distance between the point chosen on the I-V characteristics and the intersection between the tangential line and the horizontal axis. It is indicated on the figure by the horizontal arrow.

www.binils.com



www.binils.com

Figure 2.1.3 Collector current increase with an increase of the collector-emitter voltage

Diagram Source Electronic Tutorials

The change of the collector current when changing the collector-emitter voltage is primarily due to the variation of the base-collector voltage, since the base-emitter junction is forward biased and a constant base current is applied. The collector current depends on the base-collector voltage since the base-collector depletion layer width varies, which also causes the quasi-neutral width, wB', in the base to vary in te figure 2.1.3 .

. The collector current depends on the base-collector voltage since the base-collector depletion layer width varies, which also causes the quasi-neutral width, w_B', in the base to vary. This variation can be calculated for a piece-wise uniformly-doped transistor using the ideal transistor mode as described by equations given below.

$$\frac{dI_C}{dV_{CE}} \cong -\frac{dI_C}{dV_{BC}} = \frac{I_C}{w_B'}\frac{dw_B'}{dV_{BC}}$$

The change of the collector current when changing the collector-emitter voltage is primarily due to the variation of the base-collector voltage, since the base-emitter junction is forward biased and a constant base current is applied.

www.binils.com