Requirements of a biasing circuit

Emitter base junction must be forward biased and collector base junction must be reverse biased. That means the transistor should be operated in the middle of the active region or Q point should be fixed at the centre of the active region. Circuit design should provide a degree of temperature stability. Q point should be made independent of the transistor parameters such as β. To maintain the Q point stable by keeping I_C and V_{CE} constant so that the transistor will always work in active region, the following techniques are normally used,

1. Stabilization technique
2. Compensation technique

Method of stabilizing the Q point

Stabilization technique:

It refers to the use of resistive biasing circuits which allow I_B to vary so as to keep I_C relatively constant with variations in I_{CO}, β and V_{BE}.

Compensation technique:

It refers to the use of temperature sensitive devices such as diodes, transistors, thermistors which provide compensating voltage and current to maintain Q point stable.

Diode Compensation for Instability

These are the circuits that implement compensation techniques using diodes to deal with biasing instability. The stabilization techniques refer to the use of resistive biasing circuits which permit I_B to vary so as to keep I_C relatively constant.

There are two types of diode compensation methods. They are −

- Diode compensation for instability due to V_{BE} variation
- Diode compensation for instability due to I_{CO} variation

Let us understand these two compensation methods in detail.

Diode Compensation for Instability due to V_{BE} Variation

In a Silicon transistor, the changes in the value of V_{BE} results in the changes in I_C. A diode can be employed in the emitter circuit in order to compensate the variations in V_{BE} or I_{CO}. As the diode and transistor used are of same material, the voltage V_D across the diode has same temperature coefficient as V_{BE} of the transistor.

The following figure 1.5.1 shows self-bias with stabilization and compensation.

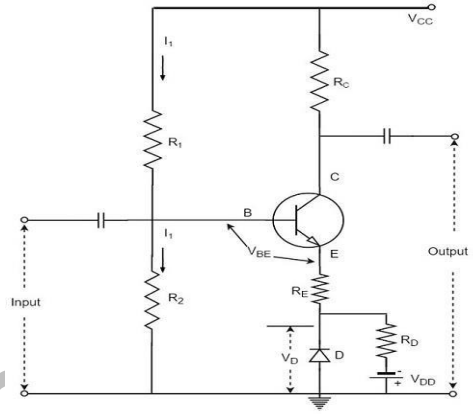


Figure 1.5.1 self-bias with stabilization and compensation

Diagram Source Brain Kart

The diode D is forward biased by the source V_{DD} and the resistor R_D. The variation in V_{BE} with temperature is same as the variation in V_D with temperature, hence the quantity ($V_{BE} – V_D$) remains constant. So the current I_C remains constant in spite of the variation in V_{BE}.

Diode Compensation for Instability due to I_{CO} Variation

The following figure 1.5.2 shows the circuit diagram of a transistor amplifier with diode D used for compensation of variation in I_{CO}.

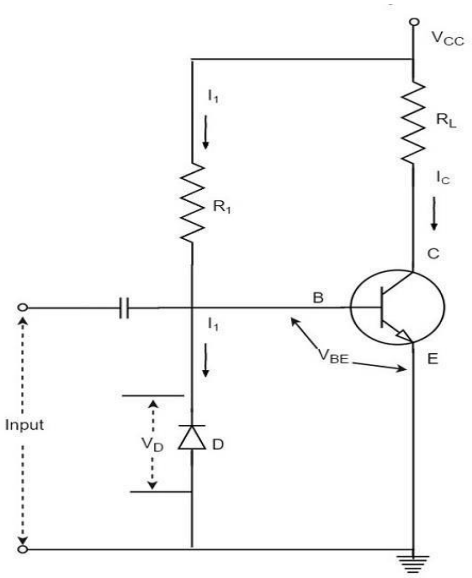


Figure 1.5.2 Transistor amplifier with diode D used for compensation of variation in I_{CO}

Diagram Source Brain Kart

So, the reverse saturation current I_O of the diode will increase with temperature at the same rate as the transistor collector saturation current I_{CO}.

$$I=(VCC-VBE) / R \cong VCC/ R=Constant$$

he diode D is reverse biased by V_{BE} and the current through it is the reverse saturation current I_O.

Now the base current is,

$$IB=I-IO$$

Substituting the above value in the expression for collector current.

$$IC=\beta(I-IO)+(1+\beta)ICOIC=\beta(I-IO)+(1+\beta)ICO$$

If $\beta \gg 1$,

$$IC=\beta I-\beta IO+\beta ICO$$

Other Compensations

There are other compensation techniques which refer to the use of temperature sensitive devices such as diodes, transistors, thermistors, Sensistors, etc. to compensate for the variation in currents.

There are two popular types of circuits in this method, one using a thermistor and the other using a Sensistor. Let us have a look at them.

Thermistor Compensation

Thermistor is a temperature sensitive device. It has negative temperature coefficient. The resistance of a thermistor increases when the temperature decreases and it decreases when the temperature increases. The below figure 1.5.3 shows a self-bias amplifier with thermistor compensation.

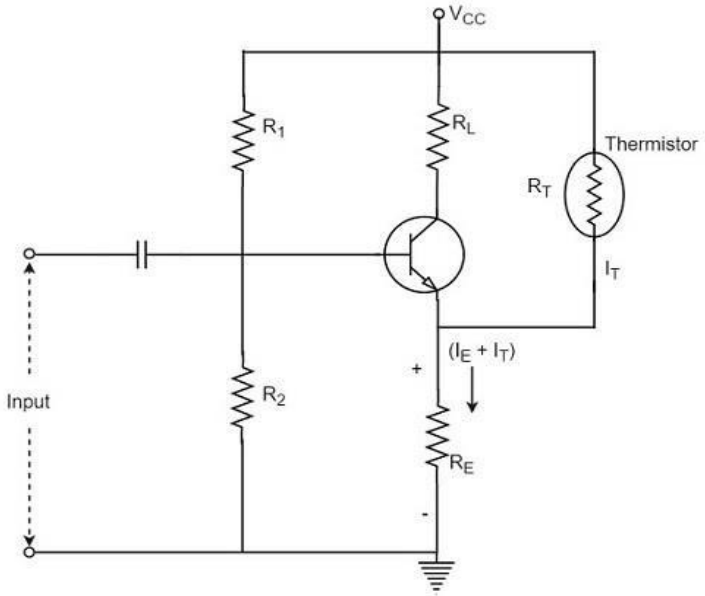


Figure 1.5.3 A self-bias amplifier with thermistor compensation.

Diagram Source Brain Kart

In an amplifier circuit, the changes that occur in I_{CO}, V_{BE} and β with temperature, increases the collector current. Thermistor is employed to minimize the increase in collector current. As the temperature increases, the resistance R_T of thermistor decreases, which increases the current through it and the resistor R_E. Now, the voltage developed across R_E increases, which reverse biases the emitter junction. This reverse bias is so high that the effect of resistors R_1 and R_2 providing forward bias also gets reduced. This action reduces the rise in collector current.

Thus the temperature sensitivity of thermistor compensates the increase in collector current, occurred due to temperature.

Sensistor Compensation

A Sensistor is a heavily doped semiconductor that has positive temperature coefficient. The resistance of a Sensistor increases with the increase in temperature and decreases with the decrease in temperature. The figure 1.5.4 below shows a self-bias amplifier with Sensistor compensation.

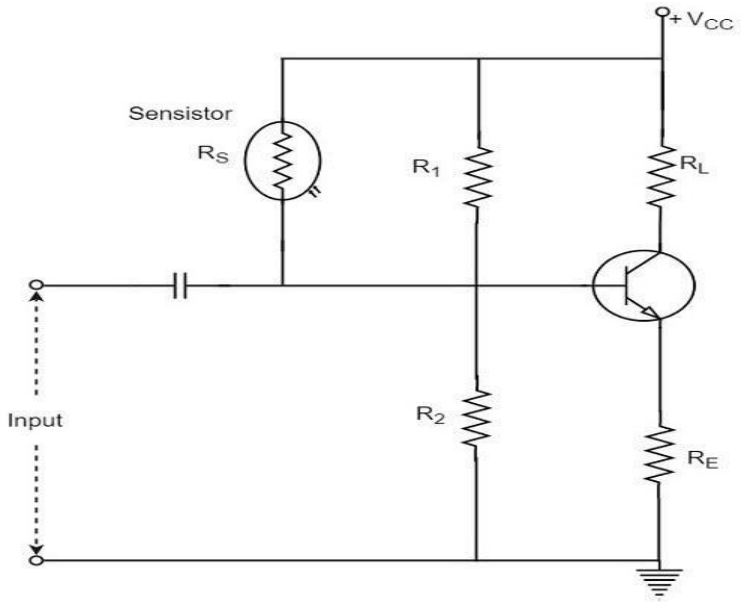


Figure 1.5.4 A self-bias amplifier with Sensistor compensation.

Diagram Source Brain Kart

In the above figure 1.5.3 , the Sensistor may be placed in parallel with R_1 or in parallel with R_E. As the temperature increases, the resistance of the parallel combination, thermistor and R_1 increases and their voltage drop also increases. This decreases the voltage drop across R_2. Due to the decrease of this voltage, the net forward emitter bias decreases. As a result of this, I_C decreases.

Hence by employing the Sensistor, the rise in the collector current which is caused by the increase of I_{CO}, V_{BE} and β due to temperature, gets controlled.

Thermal Resistance

The transistor is a temperature dependent device. When the transistor is operated, the collector junction gets heavy flow of electrons and hence has much heat generated. This heat if increased further beyond the permissible limit, damages the junction and thus the transistor.

In order to protect itself from damage, the transistor dissipates heat from the junction to the transistor case and from there to the open air surrounding it.

Let, the ambient temperature or the temperature of surrounding air = $T_A{}^oC$

And, the temperature of collector-base junction of the transistor = $T_J{}^oC$

As $T_J > T_A$, the difference $T_J - T_A$ is greater than the power dissipated in the transistor P_D will be greater. Thus,

$$TJ-TA \propto PD$$

$$TJ-TA=HPD$$

Where H is the constant of proportionality, and is called as **Thermal resistance**.

Thermal resistance is the resistance to heat flow from junction to surrounding air. It is denoted by H.

$$H=TJ-TA \ / \ PD$$

The unit of H is ^oC/watt.

If the thermal resistance is low, the transfer of heat from the transistor into the air, will be easy. If the transistor case is larger, the heat dissipation will be better. This is achieved by the use of Heat sink.

Heat Sink

The transistor that handle larger powers, dissipates more heat during operation. This heat if not dissipated properly, could damage the transistor. Hence the power transistors are generally mounted on large metal cases to provide a larger area to get the heat radiated that is generated during its operation.

The metal sheet that helps to dissipate the additional heat from the transistor is known as the **heat sink**.

The ability of a heat sink depends upon its material, volume, area, shape, contact between case and sink, and the movement of air around the sink. The heat sink is selected after considering all these factors. The image shows a power transistor with a heat sink.

A tiny transistor in the above image is fixed to a larger metal sheet in order to dissipate its heat, so that the transistor doesn't get damaged.

Thermal Runaway

The use of heat sink avoids the problem of **Thermal Runaway**. It is a situation where an increase in temperature leads to the condition that further increase in temperature, leads to the destruction of the device itself. This is a kind of uncontrollable positive feedback.

Heat sink is not the only consideration; other factors such as operating point, ambient temperature, and the type of transistor used can also cause thermal runaway.

Biasing FET Switching Circuits:

JFET Switching

A Biasing FET Switching Circuits is normally in an off state with zero drain current, or in an on state with a very small drain-source voltage. When the FET is off, there is a drain-source leakage current so small that it can almost always be neglected. When the device is on, the drain-source voltage drop depends on the channel resistance ($r_{DS(on)}$) and the drain current (I_D).

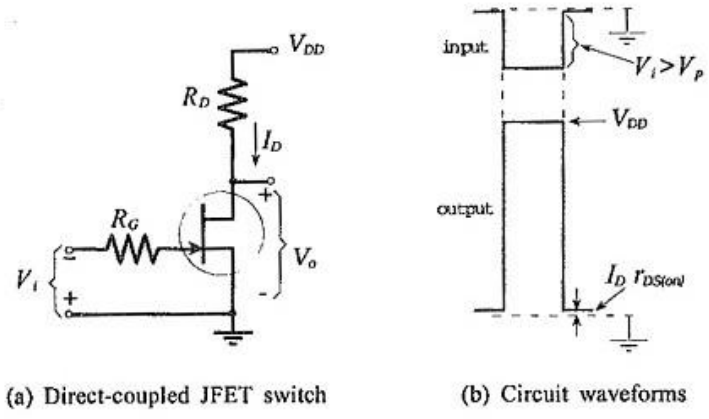
$$V_{DS(on)} = I_D \, r_{DS(on)} \qquad (1)$$

Field effect transistors designed specifically for switching applications have very low channel resistances. For example, the 2N4856 has $r_{DS(on)} = 25\ \Omega$. With low I_D levels, $r_{DS(on)}$ can be much smaller than the 0.2 V typical $V_{CE(sat)}$ for a BJT. This is an important advantage of a FET switch over a BJT switch.

Direct-Coupled JFET Switching Circuit:

A direct-coupled Biasing FET Switching Circuits is shown in Figure 1.9.1 (a) and the circuit wave forms are illustrated in Figure 1.9.1 (b)

When $V_i = 0$, the FET gate and source voltages are equal and there is no depletion region penetration into the channel. The output voltage is now $V_o = V_{DS(on)}$, as expressed by Equation(1). When V_i exceeds the FET pinch-off voltage, the device is switched off, and the output voltage goes to V_{DD}, as illustrated.



(a) Direct-coupled JFET switch (b) Circuit waveforms

Figure 1.9.1 Direct Couples JFET Switching Circuit and waveforms of the circuit input and output values

Assuming that $V_{DS(on)}$ is very small, the drain current level is determined

$$V_{DD} \approx I_D R_D \tag{2}$$

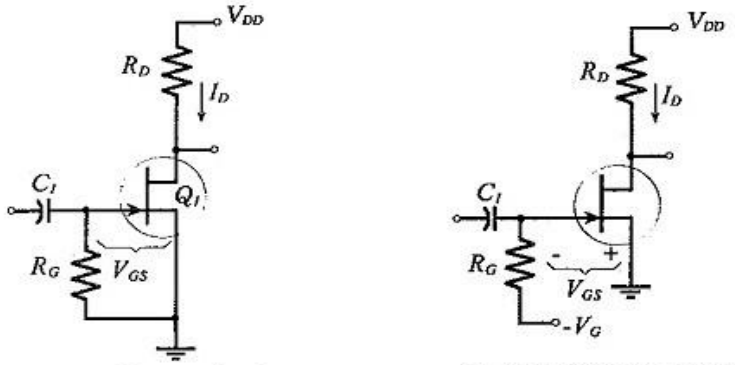
Equation (2) can be used to determine R_D when V_{DD} and I_D are specified, or to calculate I_D when R_D is known. The I_D level can then be employed to determine $V_{DS(on)}$. The lowest drain current that can be used must be very much greater than the specified drain-source leakage current for the device. To switch the FET off, V_i should exceed the maximum pinch-off voltage. However, V_i must not be so large that the drain-gate voltage ($V_{DG} = V_{DD} + V_i$) approaches the breakdown voltage. A rule-of-thumb is to select the input voltage 1 V larger than $V_{P(max)}$.

The gate resistor (R_G) in the circuit in Figure 1.9.1 is provided solely to limit any gate current in the event that the gate-source junctions become forward biased. The circuit might operate satisfactorily with R_G selected as 1 MΩ, however, high-

value resistors can slow the switching speed of the circuit, so, quite small resistance values are often used for R_G.

Capacitor-Coupled JFET Switching Circuits:

Two capacitor-coupled Biasing FET Switching Circuits are shown in Figure for the direct coupled Biasing FET Switching



1.9.2 . The FET in Figure 1.9.2 (a) is normally-on because it has $V_{GS} = 0$, and the device in Figure 1.9.2 (b) is normally-off with $-V_{GS}$ greater than the pinch-off voltage. In both circuits, the FET is switched on or off by a capacitor-coupled input pulse. The design procedure for these circuits uses the equations already discussed

Figure 1.9.2 Normally ON and Normally OFF capacitor coupled JFET Switching Circuits

Diagram Source Brain Kart

MOSFET Switching:

Figure 1.9.3(a) and 1.9.3 (b) shows two capacitor-coupled MOSFET switching circuits. The FET is biased off because $V_{GS} = 0$. A positive-going input signal is required to turn the device on. The FET is biased on by the positive V_{GS} provided by R_1 and R_2. In this case, a negative-going input voltage must be applied to turn the FET off Equations 10-20 and 10-21 can be applied to these

circuits to calculate I_D and $V_{DS(on)}$. To turn the device on to a desired level of drain current, the transfer characteristics can be employed if they are available.

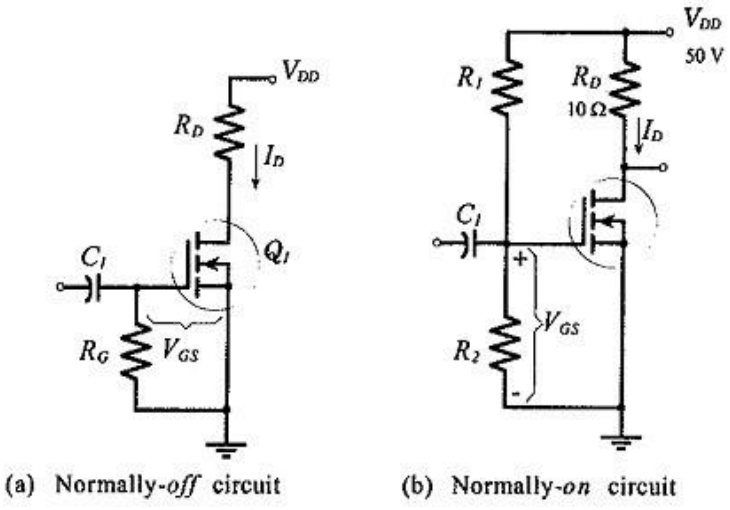


Figure 1.9.3 MOSFET Normally ON and Normally off capacitor coupled

P-channel MOSFET Switch

The N-channel MOSFET as a switch were the MOSFET is placed between the load and the ground. This also allows for the MOSFET's gate drive or switching signal to be referenced to ground (low-side switching) shown in the figure 1.9.4.

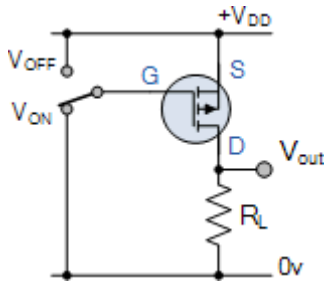


Figure 1.9.4 P-channel MOSFET Switch

Diagram Source Brain Kart

But in some applications we require the use of P-channel enhancement-mode MOSFET were the load is connected directly to ground. In this instance the MOSFET switch is connected between the load and the positive supply rail (high-side switching) as we do with PNP transistors.

In a P-channel device the conventional flow of drain current is in the negative direction so a negative gate-source voltage is applied to switch the transistor "ON".

This is achieved because the P-channel MOSFET is "upside down" with its source terminal tied to the positive supply $+V_{DD}$. Then when the switch goes LOW, the MOSFET turns "ON" and when the switch goes HIGH the MOSFET turns "OFF".

This upside down connection of a P-channel enhancement mode MOSFET switch allows us to connect it in series with a N-channel enhancement mode MOSFET to produce a complementary or CMOS switching device as shown across a dual supply.

Bipolar Junction Transistor (BJT)

Introduction

BJT consists of 2 PN junctions shown in the figure 1.1.1. It has three terminals: emitter, base and collector. Transistorcan be operated in three regions, namely cut-off, active and saturation by applying proper biasing conditions.

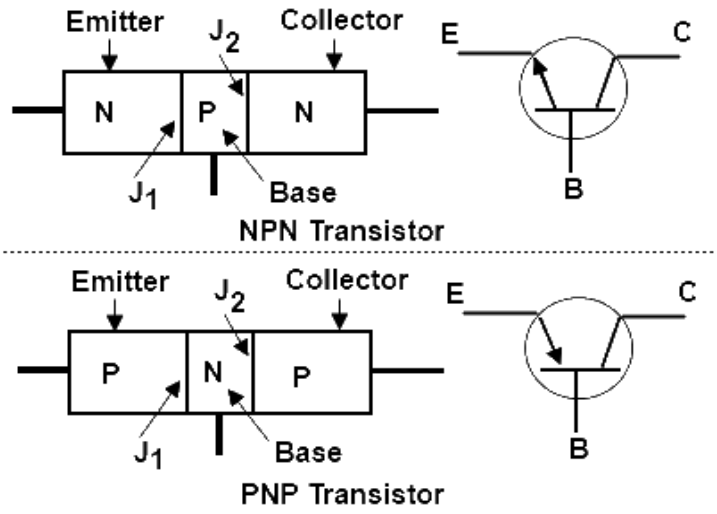


Figure 1.1.1 PN Junctions of BJT

Active Reion:

– Most important mode, e.g. for amplifier operation and switching application

– The region where current curves are practically flat.

Saturation:

– Barrier potential of the junctions cancels each other out causing a virtual short.

– Ideal transistor behaves like a closed switch.

Cutoff:

– Current reduced to zero

– Ideal transistor behaves like an open switch.

In order to operate transistor in the desired region we have to apply external d.c. voltages of correct polarity and magnitude to the two junctions of the transistor. This is nothing but the biasing of the transistor.

When we bias a transistor we establish a certain current and voltage conditions for the transistor. These conditions are known as operating conditions or d.c. operating point or quiescent point. The operating point must be stable for proper operation of the transistor. However, the operating point shifts with changes in transistor parameters such as β, Ico and V_{BE}. As transistor parameters are temperature dependent, the operating point also varies with changes in temperature.

Bipolar Transistor Configurations

As the **Bipolar Transistor** is a three terminal device, there are basically three possible ways to connect it within an electronic circuit with one terminal being common to both the input and output. Each method of connection responding differently to its input signal within a circuit as the static characteristics of the transistor vary with each circuit arrangement.

- Common Base Configuration – has Voltage Gain but no Current Gain.
- Common Emitter Configuration – has both Current and Voltage Gain.
- Common Collector Configuration – has Current Gain but no Voltage Gain.

The Common Base (CB) Configuration

As its name suggests, in the **Common Base** or grounded base configuration, the BASE connection is common to both the input signal AND the output signal. The input signal is applied between the transistors base and the emitter terminals, while the corresponding output signal is taken from between the base and the

collector terminals as shown. The base terminal is grounded or can be connected to some fixed reference voltage point.

The input current flowing into the emitter is quite large as its the sum of both the base current and collector current respectively therefore, the collector current output is less than the emitter current input resulting in a current gain for this type of circuit of “1” (unity) or less, in other words the common base configuration “attenuates” the input signal.

The Common Base Transistor Circuit sown in the figure 1.1.2

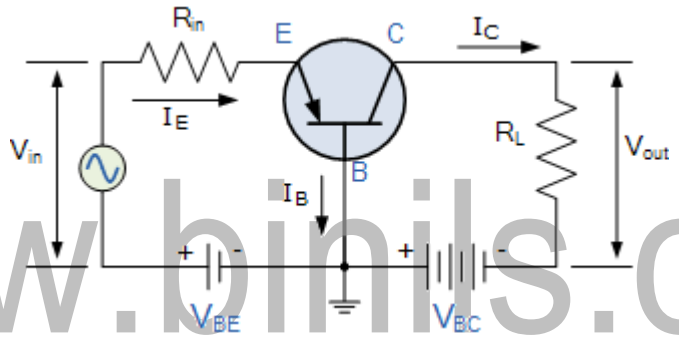


Figure 1.1.2 Common Base Transistor Circuit

Diagram Source electronic Tutorials

This type of amplifier configuration is a non-inverting voltage amplifier circuit, in that the signal voltages Vin and Vout are “in-phase”. This type of transistor arrangement is not very common due to its unusually high voltage gain characteristics. Its input characteristics represent that of a forward biased diode while the output characteristics represent that of an illuminated photo-diode.

Also this type of bipolar transistor configuration has a high ratio of output to input resistance or more importantly “load” resistance (RL) to “input” resistance (Rin) giving it a value of “Resistance Gain”. Then the voltage gain (Av) for a common base configuration is therefore given as:

Common Base Voltage Gain

$$A_V = \frac{Vout}{Vin} = \frac{I_C \times R_L}{I_E \times R_{IN}}$$

Where: Ic/Ie is the current gain, alpha (α) and RL/Rin is the resistance gain.

The common base circuit is generally only used in single stage amplifier circuits such as microphone pre-amplifier or radio frequency (R*f*) amplifiers due to its very good high frequency response.

The Common Emitter (CE) Configuration

In the **Common Emitter** or grounded emitter configuration, the input signal is applied between the base and the emitter, while the output is taken from between the collector and the emitter as shown. This type of configuration is the most commonly used circuit for transistor based amplifiers and which represents the "normal" method of bipolar transistor connection.

The common emitter amplifier configuration produces the highest current and power gain of all the three bipolar transistor configurations. This is mainly because the input impedance is LOW as it is connected to a forward biased PN-junction, while the output impedance is HIGH as it is taken from a reverse biased PN-junction.

The Common Emitter Amplifier Circuit shown in the figure 1.1.3

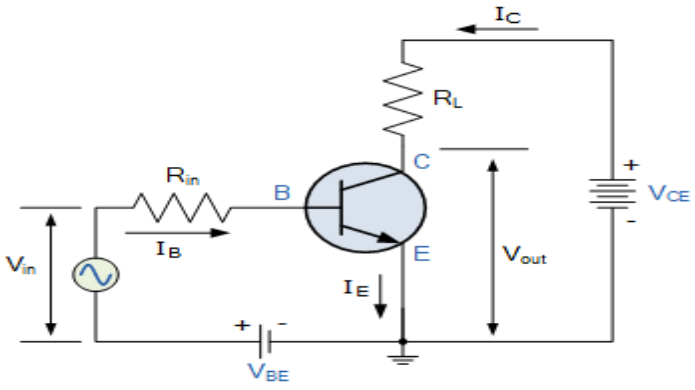


Figure 1.1.3 Common Emitter Transistor Circuit

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In this type of configuration, the current flowing out of the transistor must be equal to the currents flowing into the transistor as the emitter current is given as Ie = Ic + Ib.

As the load resistance (R_L) is connected in series with the collector, the current gain of the common emitter transistor configuration is quite large as it is the ratio of Ic/Ib. A transistors current gain is given the Greek symbol of Beta, (β).

As the emitter current for a common emitter configuration is defined as Ie = Ic + Ib, the ratio of Ic/Ie is called Alpha, given the Greek symbol of α. Note: that the value of Alpha will always be less than unity.

Since the electrical relationship between these three currents, Ib, Ic and Ie is determined by the physical construction of the transistor itself, any small change in the base current (Ib), will result in a much larger change in the collector current (Ic).

Then, small changes in current flowing in the base will thus control the current in the emitter-collector circuit. Typically, Beta has a value between 20 and 200 for most general purpose transistors. So if a transistor has a Beta value of say 100, then one electron will flow from the base terminal for every 100 electrons flowing between the emitter-collector terminal.

By combining the expressions for both Alpha, α and Beta, β the mathematical relationship between these parameters and therefore the current gain of the transistor can be given as:

$$\text{Alpha},(\alpha) = \frac{I_C}{I_E} \quad \text{and} \quad \text{Beta},(\beta) = \frac{I_C}{I_B}$$

$$\therefore I_C = \alpha.I_E = \beta.I_B$$

$$\text{as: } \alpha = \frac{\beta}{\beta + 1} \qquad \beta = \frac{\alpha}{1 - \alpha} \qquad I_E = I_C + I_B$$

Where: “Ic” is the current flowing into the collector terminal, “Ib” is the current flowing into the base terminal and “Ie” is the current flowing out of the emitter terminal.

Then to summarise a little. This type of bipolar transistor configuration has a greater input impedance, current and power gain than that of the common base configuration but its voltage gain is much lower. The common emitter configuration is an inverting amplifier circuit. This means that the resulting output signal has a 180° phase-shift with regards to the input voltage signal.

The Common Collector (CC) Configuration

In the **Common Collector** or grounded collector configuration, the collector is connected to ground through the supply, thus the collector terminal is common to both the input and the output. The input signal is connected directly to the base terminal, while the output signal is taken from across the emitter load resistor as shown. This type of configuration is commonly known as a **Voltage Follower** or **Emitter Follower** circuit.

The common collector, or emitter follower configuration is very useful for impedance matching applications because of its very high input impedance, in the region of hundreds of thousands of Ohms while having a relatively low output impedance.

The Common Collector Transistor Circuit shown in the figure 1.1.4

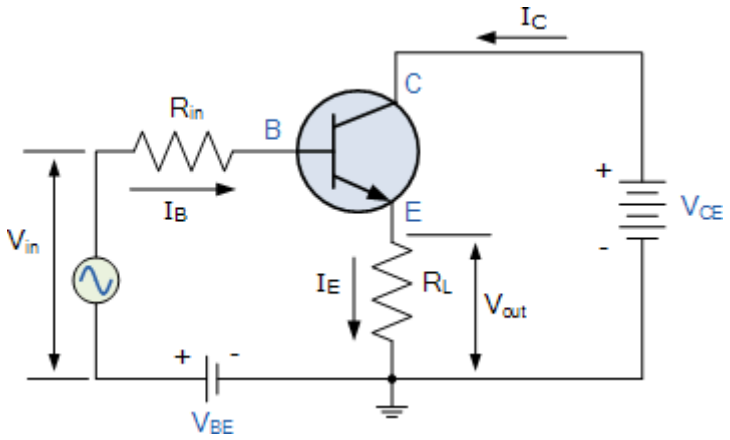


Figure 1.1.4 Common Collector Transistor Circuit

Diagram Source electronic Tutorials

The common emitter configuration has a current gain approximately equal to the β value of the transistor itself. However in the common collector configuration, the load resistance is connected in series with the emitter terminal so its current is equal to that of the emitter current. As the emitter current is the combination of the collector AND the base current combined, the load resistance in this type of transistor configuration also has both the collector current and the input current of the base flowing through it. Then the current gain of the circuit is given as:

The Common Collector Current Gain

$$I_E = I_C + I_B$$

$$A_i = \frac{I_E}{I_B} = \frac{I_C + I_B}{I_B}$$

$$A_i = \frac{I_C}{I_B} + 1 \qquad A_i = \beta + 1$$

This type of bipolar transistor configuration is a non-inverting circuit in that the signal voltages of Vin and Vout are "in-phase". The common collector

configuration has a voltage gain of about “1” (unity gain). Thus it can considered as a voltage-buffer since the voltage gain is unity.

The load resistance of the common collector transistor receives both the base and collector currents giving a large current gain (as with the common emitter configuration) therefore, providing good current amplification with very little voltage gain.

Having looked at the three different types of bipolar transistor configurations, we can now summarise the various relationships between the transistors individual DC currents flowing through each leg and its DC current gains given above in the following table.

Relationship between DC Currents and Gains

$I_E = I_B + I_C$ $I_C = I_E - I_B$ $I_B = I_E - I_C$	$\alpha = \frac{I_C}{I_E} = \frac{\beta}{1+\beta}$ $\beta = \frac{I_C}{I_B} = \frac{\alpha}{1-\alpha}$
$I_B = \frac{I_C}{\beta} = \frac{I_E}{1+\beta} = I_E(1-\alpha)$	
$I_C = \beta.I_B = \alpha.I_E$	$I_E = \frac{I_C}{\alpha} = I_B(1+\beta)$

Note that although we have looked at *NPN Bipolar Transistor* configurations here, PNP transistors are just as valid to use in each configuration as the calculations will all be the same, as for the non-inverting of the amplified signal. The only difference will be in the voltage polarities and current directions.

DC Load Line and Bias Point – DC analysis of Transistor circuits

Biasing is the application of dc voltages to establish a fixed level of current and voltage. For transistor amplifiers the resulting dc current and voltage establish an operating point on the characteristics that define the region that will be employed for amplification of the applied signal. Since the operating point is a fixed point on the characteristics, it is also called the quiescent point (abbreviated Q-point). The operating point of a device, also known as bias point, quiescent point, or Q-point, is the point on the output characteristics that shows the DC collector–emitter voltage

(V_{ce}) and the collector current (I_c) with no input signal applied shown in figure 1.3.1.

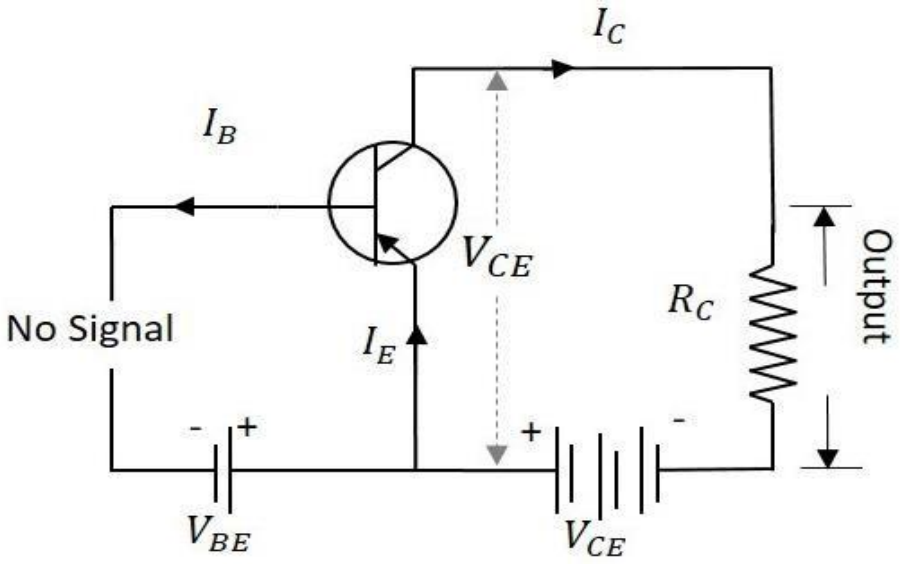


Figure 1.3.4 DC condition to draw dc load line

Diagram Source Brain Kart

We can draw a straight line on the graph of I_C versus V_{CE} which is having slope -1/Rc.To determine the two points on the line we assume $V_{CE} = V_{CC}$ and $V_{CE} = 0$

a) When $V_{CE} = V_{CC}$; $I_C = 0$ and we get a point A

b) When $V_{CE} = 0$; $I_C = V_{CC}/R_C$ and we get a point B

The figure below shows the output characteristic curves for the transistor in CE mode. The DC load line is drawn on the output characteristic curves. **Load line -** To draw load line, we have to find saturation current and the cutoff voltage.

Saturation point

The point at which the load line intersects the characteristic curve near thecollector current axis is referred to as the **saturation point** . At this point of time, the current through the transistor is maximum and the voltage across collector is minimum for a given value of load. So, saturation current for the fixed bias circuit, **Ic (sat) =Vcc/Rc** .

Cutoff point

The point where the load line intersects the cutoff region of the collector curvesis referred as the cutoff point (i.e. end of load line). At this point, collector current is approximately zero and emitter is grounded for fixed bias circuit. so, **Vce (cut) = Vc = VccOperating point** - The **"Q point"** for a transistor amplifier circuit is the point along itsoperating region in a "quiescent ", where no input signal gets amplified.

The figure below shows the output characteristic curves for the transistor in CE mode with points A and B, and line drawn between them. The line drawn between points A and B is called d.c load line. The d.c word indicates that only d.c conditions are considered, i.e input signal is assumed to be zero. The d.c load line is a plot of I_C versus V_{CE}. For a given value of Rc and a given value of Vcc. So, it represents all

collector current levels and corresponding collector emitter voltages that can exist in the circuit. Knowing any one of Ic, I_B, or V_{CE} , it is easy to determine the other two from the load line. The slope of the d.c load line depends on the value of R_C. It is the negative and equal to reciprocal of the R_C.

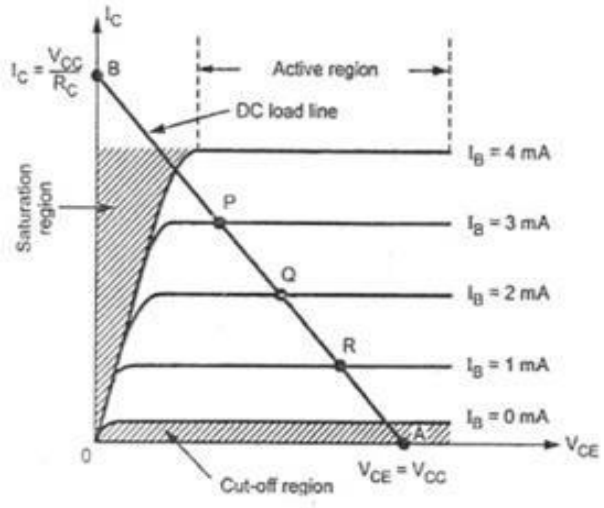


Figure 1.3.2 The output characteristic curves for the transistor in CE mode with points A and B

Diagram Source Brain Kart

Applying KVL to the base circuit, we get

$$V_{CC} - I_B R_B - V_{BE} = 0$$
$$I_B R_B = V_{CC} - V_{BE}$$
$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

The intersection of curves of different values I_B of with d.c load line gives different operating points. For different values of I_B, we have different intersection points such as P, Q and R.

Selection of operating point

The operating point can be selected at different positions on the d.c load line, near saturation region, near cut-off region or at the centre, i.e in the active region. The selection of operating point will depend on its application. When transistor is used as an amplifier, the Q point should be selected at the center of the d.c. load line to prevent any possible distortion in the amplified output signal.

Output Characteristics

When the output characteristics of a transistor are considered, the curve looks as below for different input values. In the figure 1.3.2 , the output characteristics are drawn between collector current $\mathbf{I_C}$ and collector voltage $\mathbf{V_{CE}}$ for different values of base current $\mathbf{I_B}$. These are considered here for different input values to obtain different output curves.

Operating point

When a value for the maximum possible collector current is considered, that point will be present on the Y-axis, which is nothing but the **saturation point**. As well, when a value for the maximum possible collector emitter voltage is considered, that point will be present on the X-axis, which is the **cutoff point**.

When a line is drawn joining these two points, such a line can be called as **Load line**. This is called so as it symbolizes the output at the load. This line, when drawn over the output characteristic curve, makes contact at a point called as **Operating point**.

This operating point is also called as **quiescent point** or simply **Q-point**. There can be many such intersecting points, but the Q-point is selected in such a way that irrespective of AC signal swing, the transistor remains in active region. This can be better understood through the figure 1.3.3 below.

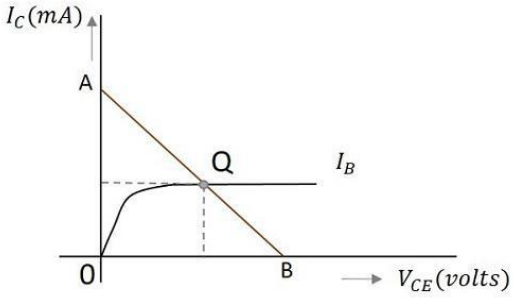


Figure 1.3.3 The Q Point or Operating Point

Diagram Source Brain Kart

The load line has to be drawn in order to obtain the Q-point. A transistor acts as a good amplifier when it is in active region and when it is made to operate at Q-point, faithful amplification is achieved.

Faithful amplification is the process of obtaining complete portions of input signal by increasing the signal strength. This is done when AC signal is applied at its input. This is discussed in AMPLIFIERS tutorial.

DC Load line

When the transistor is given the bias and no signal is applied at its input, the load line drawn at such condition, can be understood as **DC** condition. Here there will be no amplification as the signal is absent. The circuit will be as shown below figure 1.3.4.

The value of collector emitter voltage at any given time will be

$$VCE=VCC-ICRCVCE=VCC-ICRC$$

As V_{CC} and R_C are fixed values, the above one is a first degree equation and hence will be a straight line on the output characteristics. This line is called as **D.C. Load line**. The figure 1.3.5 below shows the DC load line.

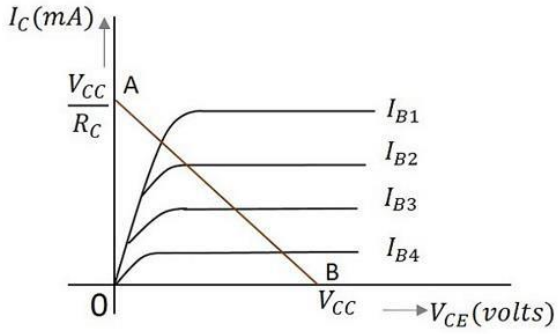


Figure 1.3.5 DC load line

Diagram Source Brain Kart

To obtain the load line, the two end points of the straight line are to be determined. Let those two points be A and B.

To obtain A

When collector emitter voltage V_{CE} = 0, the collector current is maximum and is equal to V_{CC}/R_C. This gives the maximum value of V_{CE}. This is shown as

$$VCE=VCC−ICRCVCE=VCC−ICRC$$

$$0=VCC−ICRC0=VCC−ICRC$$

$$IC=VCCRCIC=VCCRC$$

This gives the point A ($OA = V_{CC}/R_C$) on collector current axis, shown in the above figure 1.3.5.

To obtain B

When the collector current IC = 0, then collector emitter voltage is maximum and will be equal to the VCC. This gives the maximum value of IC. This is shown as

$$VCE=VCC−ICRCVCE=VCC−ICRC$$

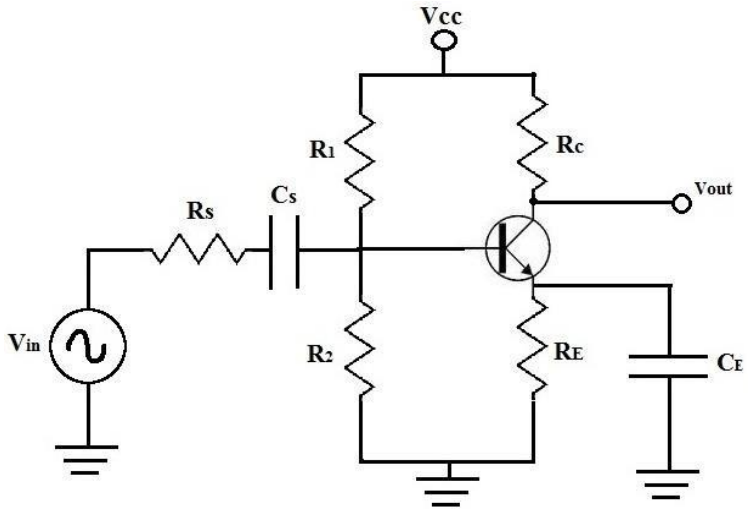
$$=VCC=VCC$$

(As $I_C = 0$)

This gives the point B, which means ($OB = V_{CC}$) on the collector emitter voltage axis shown in the above figure 1.3.5.

Hence we got both the saturation and cutoff point determined and learnt that the load line is a straight line. So, a DC load line can be drawn as shown in the figure 1.3.5.

DC Analysis of a Bipolar Junction Transistor Circuit



DC Analysis

When doing DC analysis, all AC voltage sources are taken out of the circuit because they're AC sources. DC analysis is concerned only with DC sources. We also take out all capacitors because in DC, capacitors function as open circuits. For this reason, everything before and after capacitors are removed, which in this circuit includes resistor, Rs , Below figure 1.3.1 is the schematic of the circuit above with respective to DC analysis:

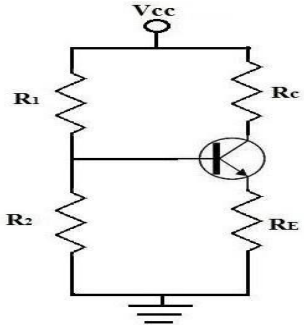


Figure 1.3.1 Circuit for DC analysis

Diagram Source Brain Kart

Now let's do the calculations to find the Vbb, Rb, Ieq, and Vceq. From this then, we can find the quiescient or just simply Q-point of this transistor circuit.

$$V_{bb} = V_{cc}\left(\frac{R_2}{R_1 + R_2}\right)$$

$$R_B = R_1 \,||\, R_2 = \frac{(R_1)(R_2)}{R_1 + R_2}$$

$$I_{EQ} = \frac{V_{BB} - V_{BE}}{\frac{R_B}{(\beta+1)} + R_E}$$

$$V_{CEQ} = V_{cc} - I_{EQ}(R_C + R_E)$$

$$\text{Q-point} = (V_{CEQ}, I_{EQ})$$

Biasing of JFET

Different types of techniques are used to bias the JFET in a proper manner. From various techniques, below three are widely used:

- ✓ Fixed DC Biasing Technique
- ✓ Self-Biasing Technique
- ✓ Potential (Voltage)Divider Biasing

Fixed DC Biasing Technique

This is done by inserting a battery in the gate circuit. The negative terminal of the battery is connected to the gate terminal. As the gate current in JFET is almost zero, there would be no voltage drop across the input gate resistance. Hence the negative potential of the battery directly reaches to gate terminal. The corresponding drain current and drain to source voltage would be the output operating point of the transistor.

As, in JFET there is no gate current, We can find the value of drain current I_D from the relation given below as I_{DSS} and $V_{GS(off)}$ (= – V_P) are given in transistor data sheet. The value of V_{DS} can be found by applying KVL at output circuit The operating point of the JFET is located at the coordinate (V_{DS}, I_D) on the characteristic graph.

$$V_{GS} = V_{GG}$$

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2$$

$$\Rightarrow I_D = I_{DSS}\left(1 - \frac{V_{GG}}{V_{GS(off)}}\right)^2$$

Diagram Source Brain Kart

In fixed DC biasing technique of an N channel JFET, the gate of the JFET is connected in such a way that the V_{GS} of the JFET remains negative all the time. As the input impedance of a JFET is very high there are no loading effects observed in the input signal. The current flow through the resistor R1 remains zero. When we apply an AC signal across the input capacitor C1, the signal appears across the gate. Now, if we calculate the voltage drop across the R1, as per the Ohms law it will be V = I x R or V_{drop} = Gate current x R1. As the current flowing to the gate is 0 the Voltage drop across the gate remains zero. So, by this biasing technique, we can control the JFET drain current by just changing the fixed voltage thus changing the V_{GS}.

Self-Biasing Technique

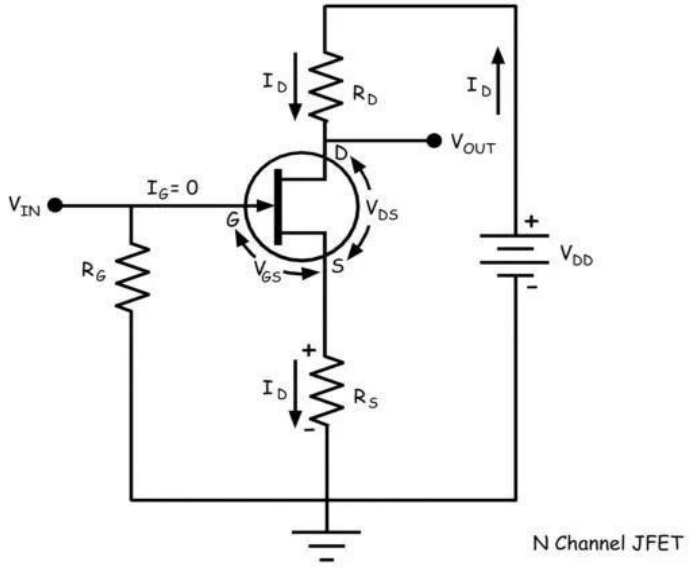


Figure 1.7.2 Self bias JFET Circuit

Diagram Source Brain Kart

In self-biasing technique in figure 1.7.2, a single resistor is added across the source pin. The voltage drop across the source resistor R2 creates the V_{GS} to bias the voltage. In this technique, the gate current is zero again. The source voltage is

determined by the same ohms law V = I x R. Therefore source voltage = Drain current x source resistor. Now, the gate to source voltage can be determined by the differences between gate voltage and source voltage.

Since the gate voltage is 0 (as the gate current flow is 0, as per V = IR, gate voltage = Gate current x gate resistor = 0) the V_{GS} = 0 – Gate current x Source resistance. Thus there is no external biasing source is needed. The biasing is created by self, using the voltage drop across source resistor.

The voltage across R_S would be

$$V_S = I_D R_S$$

Here the gate terminal is also grounded through a resistance R_G. As there is no gate current, zero ground potential appears at the gate terminal.

$$V_G = 0$$

The voltage between the gate and source is V_{GS}.

$$V_{GS} = V_G - V_S = 0 - I_D R_S$$
$$\Rightarrow V_{GS} = -I_D R_S$$

This equation tells us that here the gate terminal always gets negative potential than the source terminal.

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2$$

$$V_{DS} = V_{DD} - I_D(R_D + R_S)$$

After determining the value of I_D, and V_{DS} from above relation, we can put the operating point on the characteristic graph at the coordinate (V_{DS}, I_D).

Potential (Voltage) Divider Biasing

In this technique, an additional resistor is used and the circuit is slightly modified from the self-biasing technique, a potential voltage divider using R1 and R2 provide the required DC biasing for the JFET. The voltage drop across the source resistor is needed to be larger than the resistor divider gate voltage.

In such a way the V_{GS} remain negative. Two series connected resistors form a voltage divider circuit. The voltage at the gate terminal can be calculated by voltage division rule. In this way, the applied drain voltage is utilized to get the gate terminal voltage. A resistance is inserted into source terminal in series. The device current

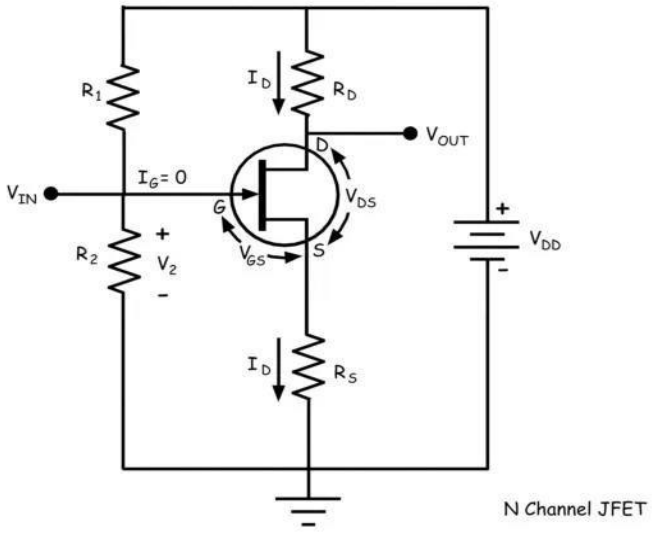


Figure 1.7.1 Voltage Divider bias JFET Circuit

Diagram Source Brain Kart

$$V_2 = V_G = \frac{V_{DD} R_2}{R_1 + R_2}$$

$$Again,\ V_2 = V_{GS} + I_D R_S \Rightarrow V_{GS} = V_2 - I_D R_S$$

$$I_D = \frac{V_2 - V_{GS}}{R_S}$$

$$And,\ V_{DS} = V_{DD} - I_D(R_D + R_S)$$

flows through the resistance and causes a voltage drop. If this source voltage drop is greater than voltage appears at the gate terminal, the gate to source voltage has a negative value which is desired for JFET operation. Let us consider the following circuit.

JFET - DC Load Line and Bias Point

When we apply an alternating signal to the gate terminal of a JFET, that would be amplified in the drain circuit. The proper amplification of a gate signal depends on proper biasing of both gate and drain section of the JFET. Proper biasing ensures that the JFET is being operated in the active or saturation zone during its amplification action.

To identify proper biasing voltages in input as well as in output circuit we need load line analysis and a properly located Q point on the characteristic curve of the device.

Q point is the intersection between DC load line and the characteristic curve of the JFET. The DC Load Line for FET circuit is drawn on the device output characteristics (or drain characteristics) in exactly the same way as for a BJT circuit. Refer to the n-channel FET circuit in figure 1.6.1 . The source terminal is grounded, the gate is biased via resistor R_G to a negative voltage ($-V_G$), and the drain terminal is supplied from $+V_{DD}$ via resistor R_D. The dc load line for this circuit is a graph of drain current (I_D) versus drain-source voltage (V_{DS}), for a given value of drain resistance and a given supply voltage.

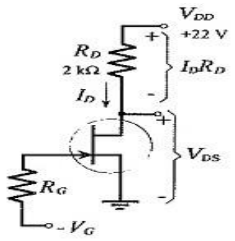


Figure 1.6.1 , FET Circuit with dc load resistor

Diagram Source Brain Kart

The drain-source voltage is,

V_{DS} = (supply voltage) – (voltage drop across R_D)

Substituting V_{DD}, R_D, and convenient levels of I_D into Eq. 10-1, produces corresponding V_{DS} and I_D values. These values are then plotted on the device characteristics, and the dc load line is drawn through them in the figure 1.6.2.

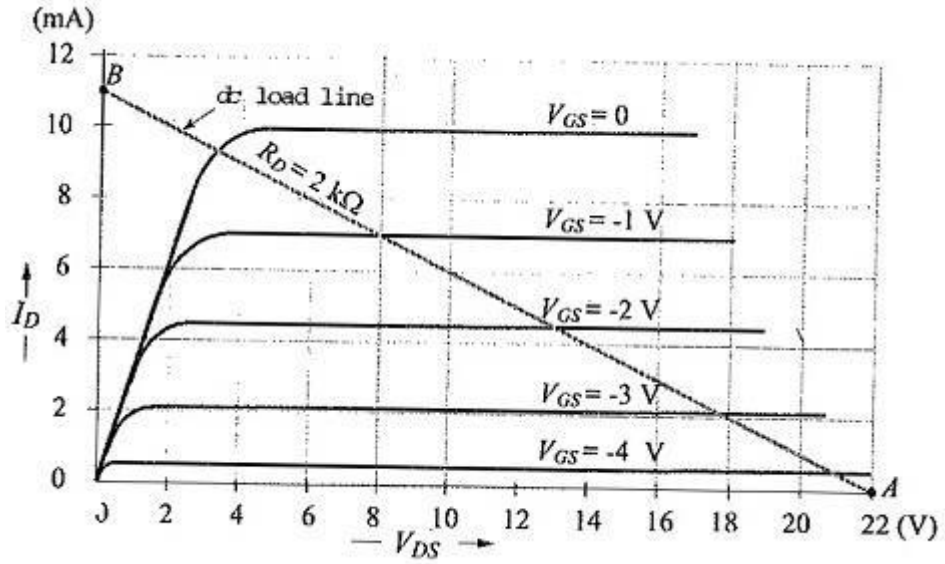


Figure 1.6.2 DC load line drawn upon FET Characteristics

Diagram Source Brain Kart

As already explained, the dc load line represents all corresponding I_D and V_{DS} levels that can exist in a FET circuit, as represented by Eq. 10-1. A point plotted at V_{DS} = 16 V and I_D = 10 mA does not appear on the load line, and so this combination of voltage and current cannot exist in this particular circuit (Figure. 1.6.2).

Bias Point (Q-Point):

Just as in the case of a BJT circuit, the dc bias point, or quiescent point (Q-point), identifies the device current and terminal voltages when there is no at input signal. When a signal is applied to the gate, I_D varies according to the instantaneous amplitude of the signal, producing a variation in V_{DS}.

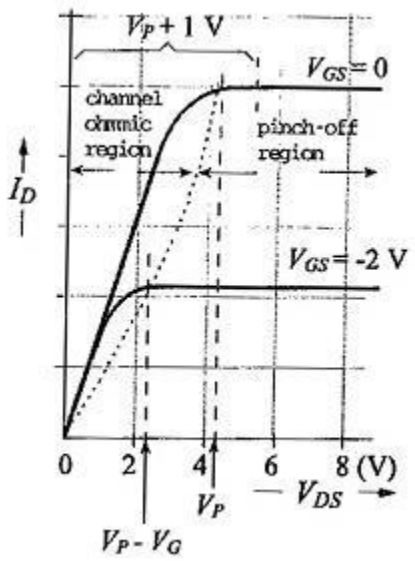


Figure 1.6.2 FET Amplifier circuit Characteristics curve between Vp and ID

Diagram Source Brain Kart

For a FET amplifier circuit, V_{DS} must remain in the pinch-off region of the characteristics. This means that it must not be allowed to fall below the the device pinch-off voltage to avoid going into the channel ohmic region. Therefore, in a FET bias circuit the drain-source voltage should always be a minimum of (V_p + 1 V), as illustrated.

Where an external bias voltage (V_G) is included (as in Figure 1.6.2), the pinch-off voltage for that bias level on the device characteristics is (V_p – V_G).The bias point for a BJT can be selected half-way along the load line, to give the maximum possible

symmetrical output voltage variation. To achieve the same result with a FET, the bias point must be half way between $V_{DS} = V_{DD}$ and $V_{DS} = V_p$. This is illustrated at Q_1 . When maximum V_{DS} variations are not required, the FET bias point can be selected at any convenient point on the dc load line just as in the case of a BJT amplifier.

$$V_{DS} = V_{DD} - I_D R_S$$

In Figure 1.6.2 drain and source resistors R_D and R_S are both present, and the total

dc load in series with the FET is $(R_D + R_S)$. For drawing the dc load line, Eq.

$$V_{DS} = V_{DD} - I_D (R_D + R_S)$$

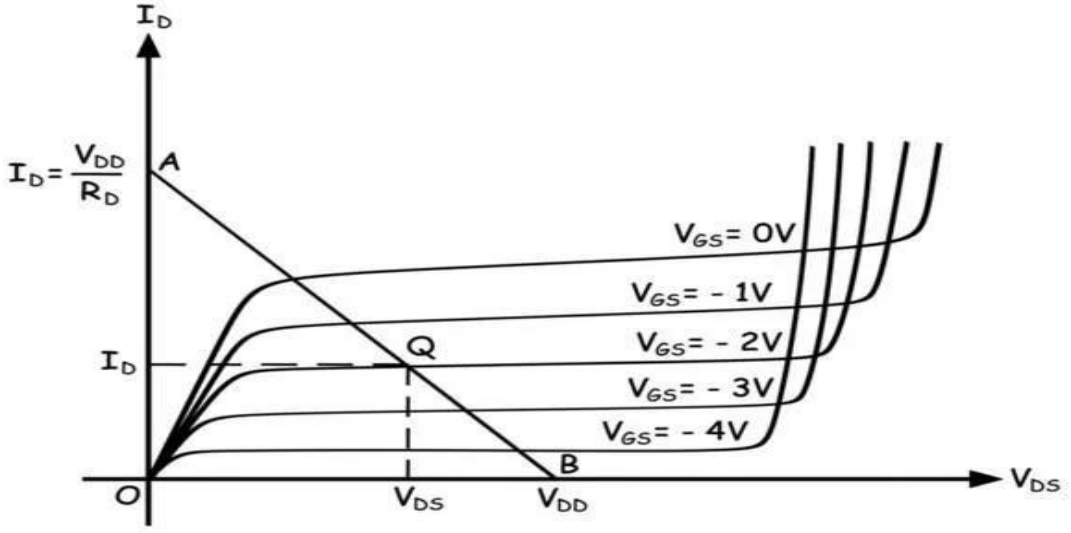


Figure 1.6.2 DC load line drawn between V_{DD} andI_D

Diagram Source Brain Kart

For better understanding, let us consider an n channel JFET with applied input biasing voltage V_{GG} and output biasing voltage V_{DD}. V_{DS} and I_D are the drain to source voltage across the JFET element and drain current through the JFET respectively. Applying Kirchhoff Voltage Law we get, From here, we can say that V_{DS} gets its maximum value when current I_D is zero and the maximum V_{DS} is,

The maximum drain current occurs when V_{DS} becomes zero and then the maximum value of drain current is, Now we will connect the coordinate of maximum V_{DS} and maximum I_D in JFET characteristic by a straight line. This line is called dc load line. This line is so called because during determining the line no ac signal present in the circuit only dc components are there for biasing purpose. During operation of a JFET as an amplifier operating point can be chosen somewhere well within the active zone of the characteristic. But when it is determined by dc load line analysis it would be the most optimized position of Q point.

Biasing of MOSFET

N-channel enhancement mode MOSFET circuit shows the source terminal at ground potential and is common to both the input and output sides of the circuit. The coupling capacitor acts as an open circuit to d.c. but it allows the signal voltage to be coupled to the gate of the MOSFET

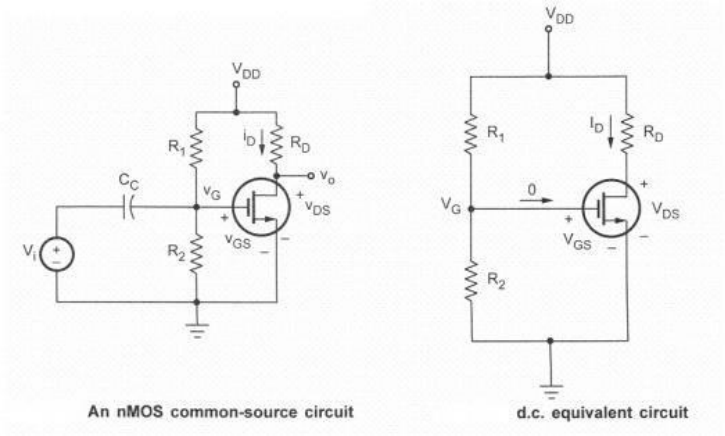


Figure 1.8.1 N MOS Common Source Circuit and its DC equivalent

Diagram Source Brain Kart

As $I_g = 0$ in V_G is given as,

$$V_G = V_{GS} = \left(\frac{R_2}{R_1 + R_2} \right) V_{DD}$$

Assume VG > VT , MOSFET is biased in the saturation region, the drain current is,

$$I_D = K(V_{GS} - V_T)^2$$

Applying KVL to drain circuit we have,

$$V_{DS} = V_{DD} - I_D R_D$$

If $V_{DS} > V_{DS(sat)} = V_{GS} - V_T$, then the MOSFET is biased in the saturation region,

If $V_{DS} < V_{DS(sat)}$, then the MOSFET is

PMOS Common Source Circuit

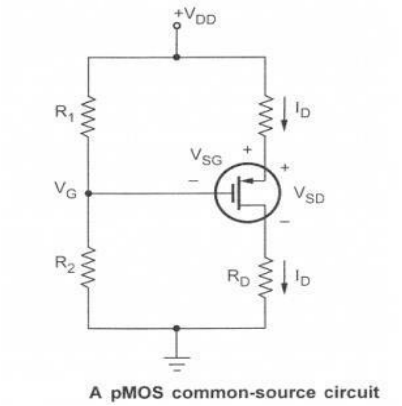


Figure 1.8.2 P MOS Common Source Circuit and its DC equivalent

Diagram Source Brain Kart

Here, the source is tied to +VDD, Which become signal ground in the a.c. equivalent circuit. Thus it is also a common-source circuit.

The d.c. analysis for this circuit is essentially the same as for the n-channel MOSFET circuit. The gate voltage is given by,

$$V_G = \left(\frac{R_2}{R_1 + R_2}\right)(V_{DD})$$

and the source-to-gate voltage is given by,

$$V_{SG} = V_{DD} - V_G$$

Assuming that $V_{GS} < V_T$, or $V_{SG} > |V_T|$, and that the device is biased in saturation region, the drain current is given by,

$$I_D = K(V_{SG} + V_T)^2$$

and the source-to-drain voltage is,

$$V_{SD} = V_{DD} - I_D R_D$$

If $V_{SD} > V_{SD(sat)} = V_{SG} + V_T$, then the MOSFET is indeed biased in the saturat region, as we have assumed. However, if $V_{SD} < V_{SD(sat)}$, the MOSFET is biased in nonsaturation region.

Load Line and Modes of Operation

The load line gives a graphical picture showing the region in whichthe MOSFET is biased. Consider the common-source circuit shown in Figure 1.8.2

Writing Kirchhoff's voltage law around the drain-source loop results $V_{Ds} = V_{DD} - I_{DRD}$, which is the load line equation. It shows a linear relationship between the drain current and drain-to-source voltage. Figure 1.8.3 shows the $V_{DS(sat)}$ characteristic for the MOSFET

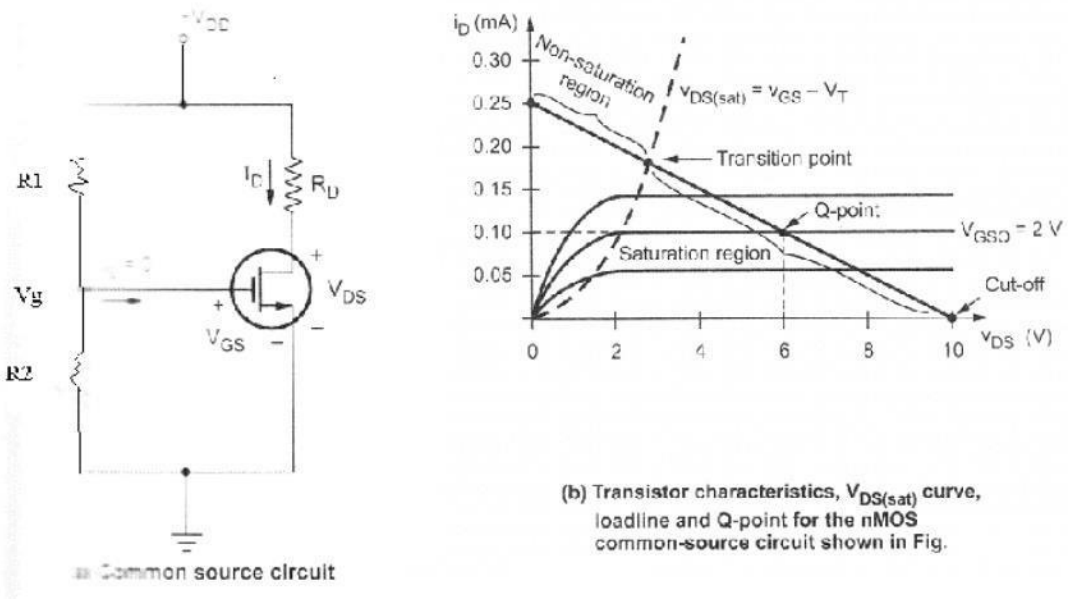


Figure 1.8.3 Common Source Circuit and its Transfer Characterictics

Diagram Source Brain Kart

The load line is given by

$$V_{DS} = V_{DD} - I_D R_D = 10 - I_D(40)$$

$$I_D = \frac{10}{40} - \frac{V_{DS}}{40} \text{ (mA)}$$

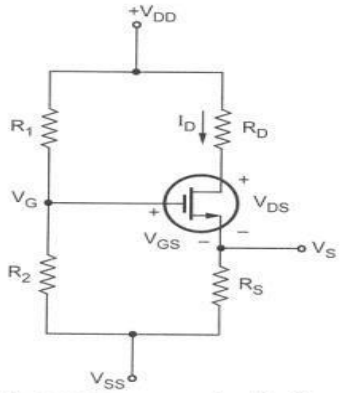
The two end points of the load line are determine in the usual manner. If the drain current = 0, then V_{DS}= 10 v; if V_{DS} = 0, then drain current = 10/40 = 0.25 mA. The Q-point of the MOSFET is given by the d.c. drain current (I_D) and drain-to-source voltage (V_{DS}) and it is always on the load line, as shown in the Figure 1.8.3and 1.8.4.

If the gate-to-source voltage is less than V1, the drain current is zero and the MOSFET is in cut-off. As the gate-to- source voltage becomes just greater than the

threshold voltage, the MOSFET turns ON and is biased in the saturation region. As V_{GS} increases, the Q-point moves up the load line. The transition point is the boundary between the saturation and non-saturation regions. It is the point where,

$V_{DS} = V_{DS(sat)} = V_{GS} - V_T$. As V_{GS} increases further, the MOSFET operates in un satu ration region.

Common Source circuit for EMOSFET with source resistor



nMOS common-source circuit with source resistor

Figure 1.8.4 N MOS Common Source Circuit with Source Resistor

Diagram Source Brain Kart

Voltage Divider Bias

As

$$I_G = 0 \text{ A}$$

$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$$

Applying KVL to input circuit we get,

$$-V_{GS} - V_S = 0$$

$$V_{GS} = V_G - I_S R_S = V_G - I_D R_D \quad \because I_D = I_S$$

$$V_{GS} = V_G - I_D R_S$$

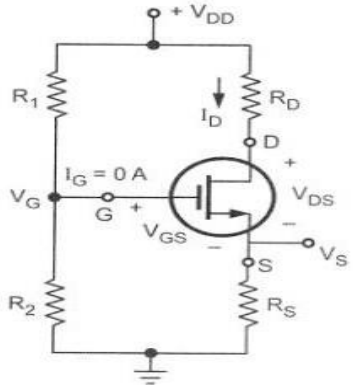


Figure 1.8.5 Common Source Circuit

Diagram Source Brain Kart

In figure 1.8.5.

Applying KVL to output circuit we get,

$$V_{DD} - I_D R_D - V_{DS} - I_S R_S = 0$$

$$\therefore \quad V_{DS} = V_{DD} - I_D R_D - I_S R_S = V_{DD} - I_D R_D - I_D R_S$$

$$= V_{DD} - I_D (R_D + R_S)$$

Because $I_D = I_S$

Biasing Circuit for D MOSFET

Biasing circuits for depletion type MOSFET are quite similar to the circuits used for JFET biasing. The primary difference between the two is the fact that depletion type MOSFETs also permit operating points with positive value of V6s for n-channel and negative values of V6s for p-channel MOSFET. To have positive value of V_{GS} for n-channel and negative value of V6s for p-channel self bias circuit is unsuitable.

P Channel Enhancement Mode MOSFET

Figure 1.8.6 shows A Common Source P - Channel Enhancement mode MOSFET .

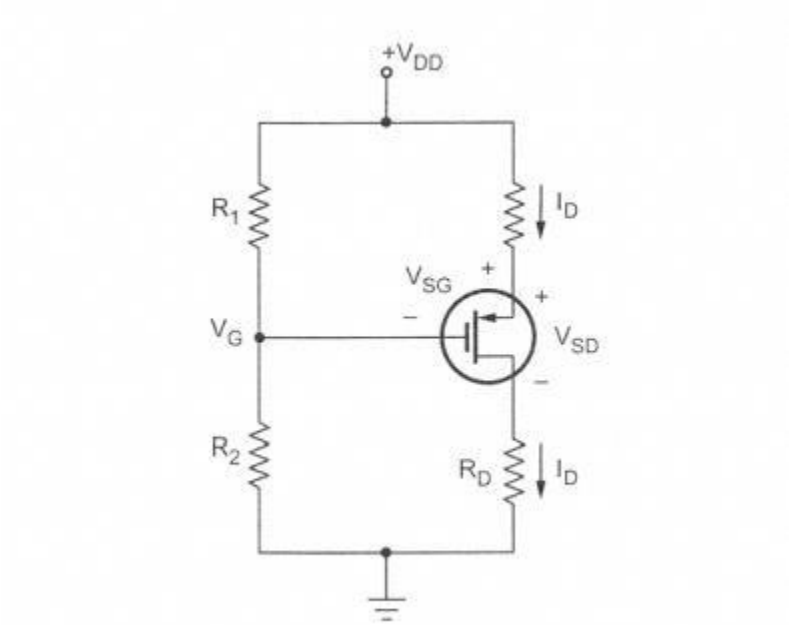


Fig. A pMOS common-source circuit

Figure 1.8.6 A Common Source P - Channel Enhancement mode MOSFET

Diagram Source Brain Kart

$$V_G = \left(\frac{R_2}{R_1 + R_2}\right)(V_{DD})$$

and the source-to-gate voltage is given by,

$$V_{SG} = V_{DD} - V_G$$

Assuming that $V_{GS} < V_T$, or $V_{SG} > |V_T|$, and that the device is biased in the saturation region, the drain current is given by,

$$I_D = K(V_{SG} + V_T)^2$$

and the source-to-drain voltage is,

$$V_{SD} = V_{DD} - I_D R_D$$

If $V_{SD} > V_{SD(sat)} = V_{SG} + V_T$, then the MOSFET is indeed biased in the saturation region, as we have assumed. However, if $V_{SD} < V_{SD(sat)}$, the MOSFET is biased in the nonsaturation region.

Transistor Biasing

The proper flow of zero signal collector current and the maintenance of proper collector emitter voltage during the passage of signal is known as **Transistor Biasing**. The circuit which provides transistor biasing is called as **Biasing Circuit**.

Need for DC biasing

If a signal of very small voltage is given to the input of BJT, it cannot be amplified. Because, for a BJT, to amplify a signal, two conditions have to be met.

- The input voltage should exceed **cut-in voltage** for the transistor to be **ON**.
- The BJT should be in the **active region**, to be operated as an **amplifier**.

Transistor Biasing is the process of setting a transistor's DC operating voltage or current conditions to the correct level so that any AC input signal can be amplified correctly by the transistor. Transistors are one of the most widely used semiconductor devices which are used for a wide variety of applications, including amplification and switching. However, to achieve these functions satisfactorily, a transistor must be supplied with a certain amount of current and/or voltage. The process of setting these conditions for a transistor circuit is referred to as transistor biasing. Transistor biasing can be accomplished by various techniques that give rise to different kinds of biasing circuits. However, all of these circuits are based on the principle of providing the right amount of base current, IB, and, in turn, the collector current, IC from the supply voltage, VCC when no signal is present at an input.

Moreover, the collector resistor RC has to be chosen so that the collector-

emitter voltage, VCE, remains greater than 0.5V for transistors made of germanium and greater than 1V for the transistors made of silicon. If appropriate DC voltages and currents are given through BJT by external sources, so that BJT operates in active region and superimpose the AC signals to be amplified, then this problem can be avoided. The given DC voltage and currents are so chosen that the transistor remains in active region for entire input AC cycle. Hence DC biasing is needed.

The below figure shows a transistor amplifier that is provided with DC biasing on both input and output circuits.

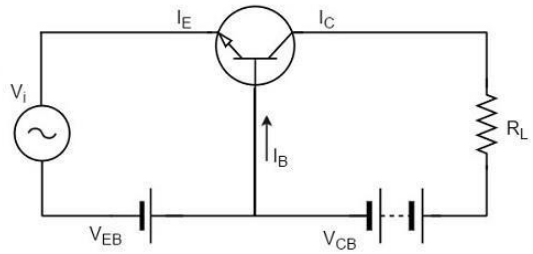


Figure 1.2.1 Transistor amplifier provided with DC biasing on both input and output circuits.

Diagram Source electronic Tutorials

For a transistor to be operated as a faithful amplifier, the operating point should be stabilized. Let us have a look at the factors that affect the stabilization of operating point.

Factors affecting the operating point

The main factor that affect the operating point is the temperature. The operating point shifts due to change in temperature.

As temperature increases, the values of I_{CE}, β, V_{BE} gets affected.

- I_{CBO} gets doubled (for every 10^o rise)
- V_{BE} decreases by 2.5mv (for every 1^o rise)

So the main problem which affects the operating point is temperature. Hence operating point should be made independent of the temperature so as to achieve stability. To achieve this, biasing circuits are introduced.

Various biasing methods of BJT

Types of Transistor Biasing

The types of transistor biasing include:

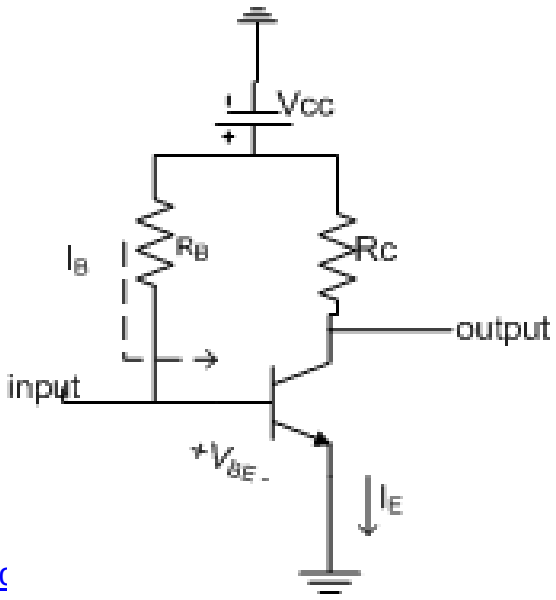
- Fixed Bias Circuit
- Collector to Base bias Circuit
- Voltage Divider Bias
- Emitter Feedback

Fixed Bias (Base Resistor Bias)

The biasing circuit shown in Figure 1.4.1 has a base resistor R_B connected between the base and the V_{CC}. Here the base-emitter junction of the transistor is forward biased by the voltage drop across R_B, which is the result of I_B flowing through it

Figure 1.4.1 Fixed bias circuit

Diagram Source Brain Kart



The Figure 1.4.1 shows the fixed bias circuit. It is the simplest d.c. bias configuration. For the d.c. analysis we can replace capacitor with an open circuit because the reactance of a capacitor for d.c. is

$$X_C = 1 / 2\pi fC = 1 / 2\pi(0)C = \infty.$$

$V_{CC} = I_B R_B + V_{BE}$

Therefore,

$I_B = (V_{CC} - V_{BE})/R_B$

For a given transistor, V_{BE} does not vary significantly during use. As V_{CC} is of fixed value, on selection of R_B, the base current I_B is fixed. Therefore this type is called *fixed bias* type of circuit.

In the Collector circuit

Apply KVL, we get

$V_{CC} = I_C R_C + V_{CE}$

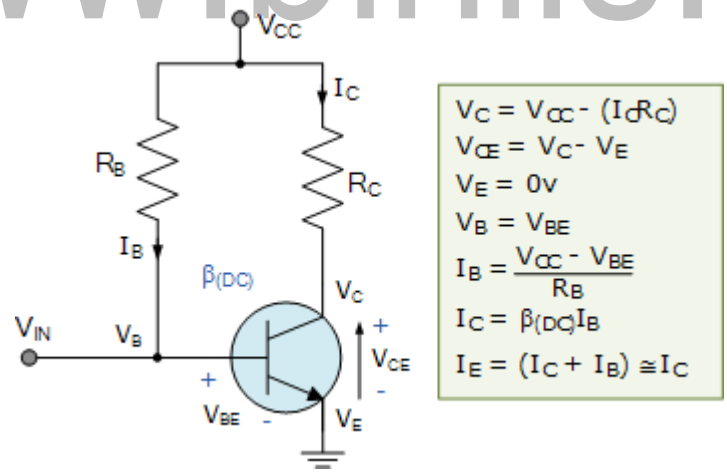


Figure 1.4.2 DC Analysis Fixed bias circuit

Diagram Source Brain Kart

In the base circuit figure 1.4.2,

Apply KVL, we get

Therefore,

$V_{CE} = V_{CC} - I_C R_C$

The common-emitter current gain of a transistor is an important parameter in circuit design, and is specified on the data sheet for a particular transistor. It is denoted as β.

$I_C = \beta I_B$

$$I_C = \frac{V_{CC} - V_{CE}}{R_C}$$

$$V_{CE} = V_C - V_E$$

$$V_{BE} = V_B - V_E$$

In this circuit $V_E = 0$

$$V_{BE} = V_B$$

$$V_{CE} = V_C$$

Stability factor S for Fixed bias circuit

Stability factor S

$$I_B \cong \frac{V_{CC}}{R_B}$$

When I_B changes by ∂I_B, V_{CC} and V_{BE} are unaffected.

$$\therefore \frac{\partial I_B}{\partial I_C} = 0 \quad \because I_C \text{ is not present in the equation.}$$

Substituting this value in equation , we get,

$$S = \frac{1+\beta}{1-\beta(\partial I_B / \partial I_C)} = \frac{1+\beta}{1-0}$$

$$\therefore \quad S = 1 + \beta$$

Merits:

- It is simple to shift the operating point anywhere in the active region by merely changing the base resistor (R_B).
- A very small number of components are required.

Demerits:

- The collector current does not remain constant with variation in temperature or power supply voltage. Therefore the operating point is unstable.
- Changes in V_{be} will change I_B and thus cause R_E to change. This in turn will alter the gain of the stage.

- =When the transistor is replaced with another one, considerable change in the value of β can be expected. Due to this change the operating point will shift.
- For small-signal transistors (e.g., not power transistors) with relatively high values of β (i.e., between 100 and 200), this configuration will be prone to thermal runaway. In particular, the stability factor, which is a measure of the change in collector current with changes in reverse saturation current, is approximately β+1. To ensure absolute stability of the amplifier, a stability factor of less than 25 is preferred, and so small-signal transistors have large stability factors.

Usage:

Due to the above inherent drawbacks, fixed bias is rarely used in linear circuits (i.e., those circuits which use the transistor as a current source). Instead, it is often used in circuits where transistor is used as a switch. However, one application of fixed bias is to achieve crude automatic gain control in the transistor by feeding the base resistor from a DC signal derived from the AC output of a later stage.

Collector to Base Bias

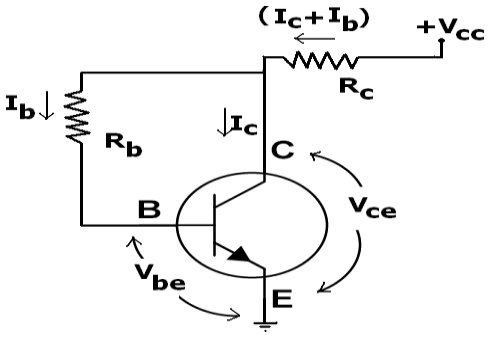


Figure 1.4.4 DC Analysis Collector to Base Bias circuit

Diagram Source Brain Kart

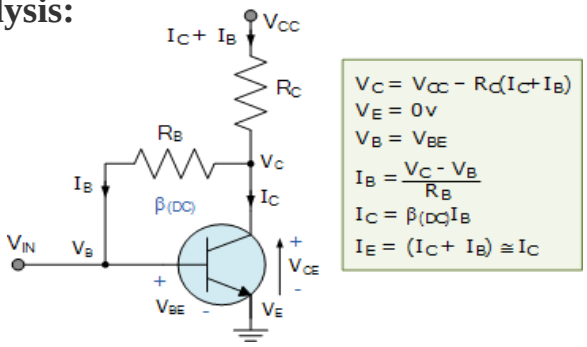
Figure 1.4.3 Collector to Base Bias circuit

Diagram Source Brain Kart

Figure 1.4.3 shows the dc bias with voltage feedback. It is also called as collector to base bias circuit. It is an improvement over fixed bias method. In this, biasing resistor is connected between collector and base of the transistor to provide feedback path.

Circuit analysis:

Base circuit:



$V_C = V_{CC} - R_C(I_C + I_B)$
$V_E = 0v$
$V_B = V_{BE}$
$I_B = \frac{V_C - V_B}{R_B}$
$I_C = \beta_{(DC)} I_B$
$I_E = (I_C + I_B) \cong I_C$

$$V_{CC} - (I_B + I_C) R_C - I_B R_B - V_{BE} = 0$$

$$V_{CC} = (R_B + R_C) I_B + I_C R_C + V_{BE}$$

$$= (R_B + R_C) I_B + \beta I_B R_C + V_{BE}$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (1+\beta) R_C}$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + \beta R_C} \qquad \because \beta >> 1$$

Only the difference between the equation for I_B and that obtained for fixed bias configuration is βR_C, so the feedback path results in a reflection of the resistance R_C to the input circuit.

Collector circuit:

Applying KVL to the collector circuit,

$$V_{CC} - (I_C + I_B) R_C - V_{CE} = 0$$

$$V_{CE} = V_{CC} - (I_C + I_B) R_C$$

If there is a change in β due to piece to piece variation between transistors or if there is a change in β and I_{CO} due to the change in temperature. So collector current tends to increase. As a result, voltage drop across R_C increases. Due to reduction in V_{CE}, I_B reduces. The result is that the circuit tends to maintain a stable value of collector current, keeping the Q point fixed.

In this circuit, R_B appears directly across input and output. A part of output is feedback to the input. And increase in collector current decreases the base current. So negative feedback exists in the circuit. It is also called as voltage feedback bias circuit.

Modified collector to base bias circuit:

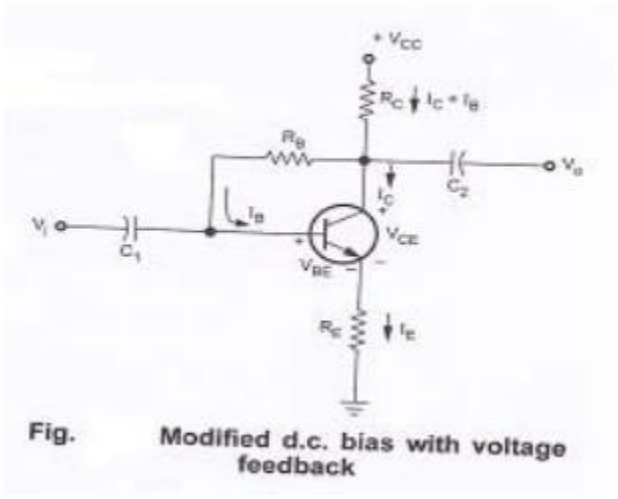


Figure 1.4.5 Modified collector to base bias circuit

Diagram Source Brain Kart

To improve the level of stability, emitter resistance is connected in this circuit.

Base circuit:

Applying KVL to base circuit in figure 1.4.5,

$$V_{CC} - (I_C + I_B)\, RC - I_B R_B - V_{BE} - I_E R_E = 0$$

$$I_B = [V_{CC} - V_{BE}] / [R_B + (1+\beta)(R_C + R_E)]$$

$$I_B = [V_{CC} - V_{BE}] / [R_B + \beta (R_C + R_E)]$$

Only difference between the equation for I_B and that obtained for the fixed bias configuration is the term $\beta (R_C + R_E)$.So feedback path results in a reflection of the resistance R_C back to the input circuit.

In general,

$I_B = V' / R_B + \beta R'$

Where $V' = V_{CC} - V_{BE}$

$R' = 0$ for fixed bias

$R' = R_E$ for emitter bias

$R' = R_C$ for collector to base bias

$R' = R_C + R_E$ for collector to base bias with R_E

Collector circuit:

Applying KVL to collector circuit,

$V_{CC} - (I_C + I_B) RC - V_{CE} - I_E R_E = 0$

$V_{CE} = V_{CC} - I_E (R_C + R_E)$

Stability factor S for collector to base bias circuit:

$V_{CC} = I_C RC - I_B(R_B + R_C) + V_{BE}$

When I_{CBO}, I_B and I_C changes with no effect on VCC and V_{BE}, the equation becomes,

$S = [1+\beta] / 1+\beta (R_C / (R_C + R_B))$

$$S = \frac{1+\beta}{1+\beta (R_C / (R_C + R_B))}$$

Collector to base bias circuit is having lesser stability factor than for fixed bias circuit. So this circuit provides better stability than fixed bias circuit.

Voltage divider bias circuit:

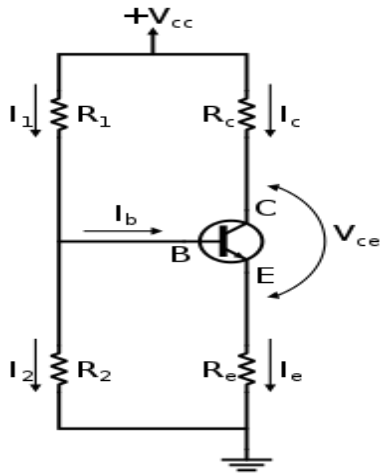


Figure 1.4.6 Voltage divider bias circuit

Diagram Source Brain Kart

Figure 1.4.6 shows the voltage divider bias circuit. In this, biasing is provided by three resistors R_1, R_2 and R_E. The resistors R_1& R_2 act as a potential divider giving a fixed voltage to base. If collector current increases due to change in temperature or change in β, emitter current I_E also increases and voltage drop across R_E increases thus reducing the voltage difference between base and emitter. Due to reduction in base emitter voltage, base current and collector current reduces. So we can say that negative feedback exists in emitter bias circuit. This reduction in collector current compensates for the original change in I_C.

Circuit analysis:

Base circuit:

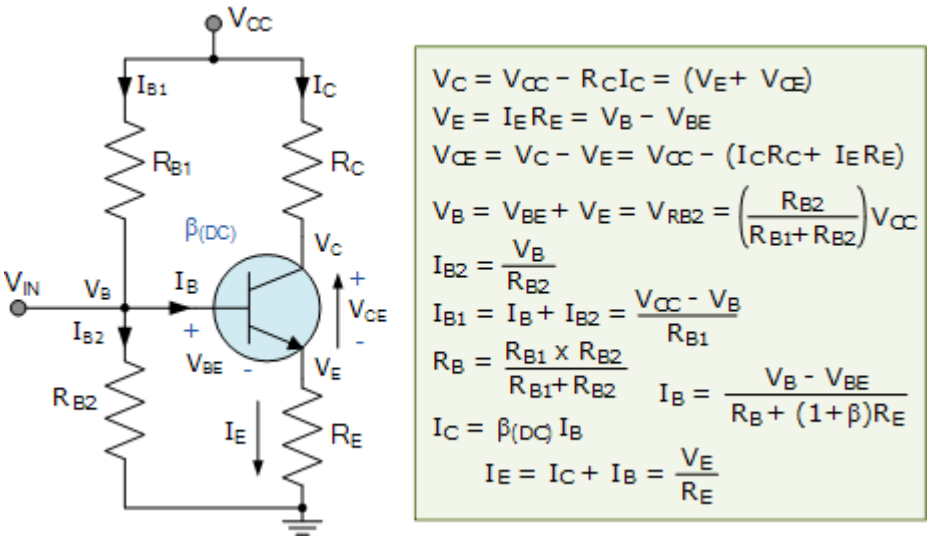


Figure 1.4.7 Voltage divider bias circuit Base circuit

Diagram Source Brain Kart

Let us consider figure 1.4.7 the base circuit as shown in above figure. Voltage

across R_2 is base voltage V_B. Applying voltage divider rule to find V_B

$$V_B = \frac{R_2 (I)}{R_1 (I+I_B) + R_2 (I)} * V_{CC}$$

$$= \frac{R2}{R_1+R_2} * V_{CC} \qquad \text{with } I >> I_B$$

Collector circuit:

Let us consider the collector circuit as shown in above figure 1.4.7 . Voltage across R_E can be obtained as,

$$V_E = I_E R_E = V_B - V_{BE}$$

$$I_E = \frac{V_B - V_{BE}}{R_E}$$

Apply KVL to collector circuit,

$$V_{CE} = V_{CC} - I_C R_C - I_E R_E$$

Simplified circuit of voltage divider bias

Thevenin's equivalent circuit for voltage divider bias From above figure 1.4.7 , R_1 and R_2 are replaced by R_B and V_T. Where R_B is the parallel combination of R=1 and R_2 V_T is the thevenin's voltage

$$R_B = \frac{R_1 R_2}{R_1 + R_2}$$

$$V_T = I_B R_B + V_{BE} + I_E R_E$$

$$V_T = V_{BE} + (R_B + R_E) I_B + I_C R_E$$

$$V_{BE} = V_T - (R_B + R_E) I_B - I_C R_E$$

Stability factor for voltage divider bias:

Stability factor S:

For determining stability factor S for voltage divider bias, consider the equivalent circuit. Thevenin's voltage is given by,

$$V_T = \frac{R_2 \times V_{CC}}{R_1 + R_2}$$

R_1, R_2 are replaced by R_B which is the parallel combination of R_1 and R_2.

$$R_B = \frac{R_1 R_2}{R_1 + R_2}$$

Apply KVL to base circuit,

$$V_T = I_B R_B + V_{BE} + (I_B + I_C) R_E$$

Differentiating with respect to I_C and considering V_{BE} to be independent of I_C,

$$0 = \frac{\partial I_B}{\partial I_C} \times R_B + \frac{\partial I_B}{\partial I_C} \times R_E + R_E$$

$$\frac{\partial I_B}{\partial I_C}(R_E + R_B) = -R_E$$

$$\frac{\partial I_B}{\partial I_C} = \frac{-R_E}{R_E + R_B}$$

Stability factor S is given by,

$$S = \frac{1+\beta}{1-\beta(\partial I_B/\partial I_C)}$$

From above equation, the following points are observed.

1. The ratio R_B / R_E controls value of stability factor S. If $R_B/R_E << 1$ then it is reduced to $S = (1+\beta). 1/ (1+\beta) = 1$

Practically R_B/R_E not equal to zero. But to have better stability factor S , we have to keep ratio R_B/R_E as small as possible.

2. To keep R_B/R_E small, it is necessary to keep R_B small. Due to small value of R_1 and R_2, potential divider circuit will draw more current from V_{CC} reducing the life of the battery. Another important aspect is that reducing R_B will reduce input impedance of the circuit, since R_B comes in parallel with the input. This reduction of input impedance in amplifier circuit is not desirable and hence R_B cannot be made very small.

3. Emitter resistance R_E is another parameter, it is used to decrease the ratio R_B/R_E. Drop across R_C will reduce. This shifts the operating point Q which is not desirable and hence there is limit for increasing R_E.

While designing voltage divider bias circuit, the following conditions are to be satisfied,

S – Small

RB - Reasonably small

RE - Not very large

4. If ratio R_B/R_E is fixed, S increases with β. So stability decreases with increasing β.

5. Stability factor S is essentially independent of β for small value of S.

$$S = \frac{1+\beta}{1+\beta\left(\frac{R_E}{R_E+R_B}\right)}$$

Dividing each term by R_E,

$$S = \frac{(1+\beta)(R_E+R_B)}{R_B+R_E+\beta R_E} = \frac{(1+\beta)(R_E+R_B)}{R_B+(1+\beta)R_E}$$

$$S = (1+\beta)\frac{1+R_B/R_E}{(1+\beta)+R_B/R_E}$$

Transistor Biasing with Emitter Feedback

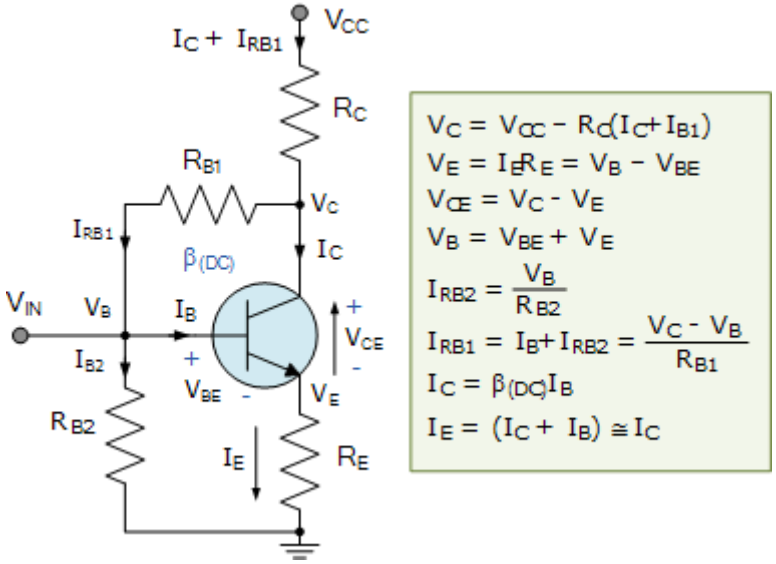


Figure 1.4.8 Transistor Biasing with Emitter Feedback circuit

Diagram Source Brain Kart

This type of transistor biasing configuration, often called self-emitter biasing, uses both emitter and base-collector feedback to stabilize the collector current even further. This is because resistors R_{B1} and R_E as well as the base-emitter junction of the transistor are all effectively connected in series as shown in the figure 1.4.8 with the supply voltage, V_{CC}.

The downside of this emitter feedback configuration is that it reduces the output gain due to the base resistor connection. The collector voltage determines the current flowing through the feedback resistor, R_{B1} producing what is called “degenerative feedback”.

The current flowing from the emitter, I_E (which is a combination of $I_C + I_B$) causes a voltage drop to appear across R_E in such a direction, that it reverse biases the base-emitter junction.

So if the emitter current increases, due to an increase in collector current, voltage drop $I*R_E$ also increases. Since the polarity of this voltage reverse biases the base-emitter junction, I_B automatically decrease. Therefore the emitter current increase less than it would have done had there been no self biasing resistor.

Generally, resistor values are set so that the voltage dropped across the emitter resistor R_E is approximately 10% of V_{CC} and the current flowing through resistor R_{B1} is 10% of the collector current I_C.

Thus this type of transistor biasing configuration works best at relatively low power supply voltages.