3.4 CHANNEL LENGTH MODULATION

Channel length modulation (CLM) is an effect in field effect transistors, a shortening of the length of the inverted channel region with increase in drain bias for large drain biases. The result of CLM is an increase in current with drain bias and a reduction of output resistance. It is one of several short-channel effects in MOSFET scaling. It also causes distortion in JFET amplifiers.

To understand the effect, first the notion of pinch-off of the channel is introduced. The channel is formed by attraction of carriers to the gate, and the current drawn through the channel is nearly a constant independent of drain voltage in saturation mode. However, near the drain, the gate and drain jointly determine the electric field pattern. Instead of flowing in a channel, beyond the pinch-off point the carriers flow in a subsurface pattern made possible because the drain and the gate both control the current. In the figure at the right, the channel is indicated by a dashed line and becomes weaker as the drain is approached, leaving a gap of uninverted silicon between the end of the formed inversion layer and the drain (the pinch-off region).

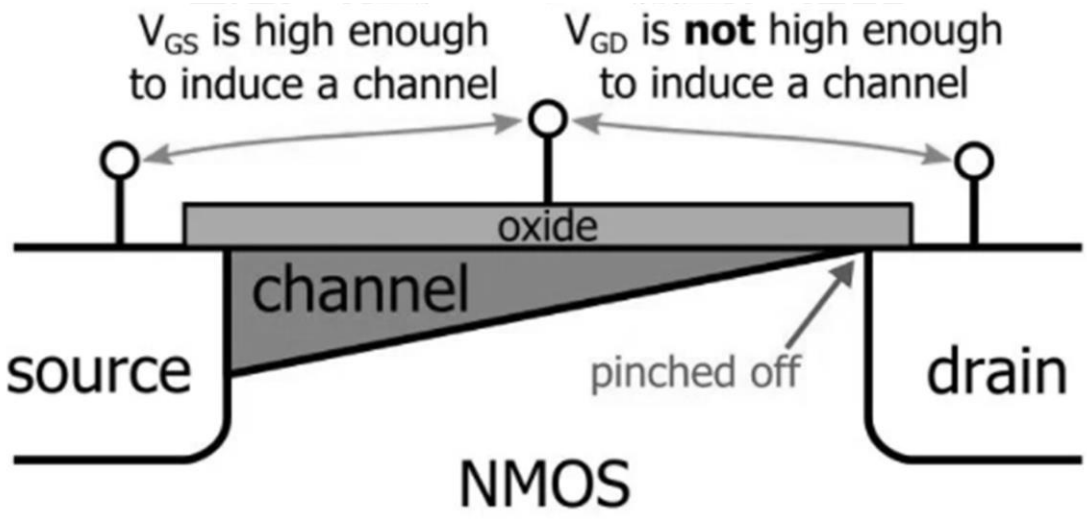

Fig:3.4.1 Pinch off Voltage

As the drain voltage increases, its control over the current extends further toward the source, so the uninverted region expands toward the source, shortening the length of

the channel region, the effect called channel-length modulation. Because resistance is proportional to length, shortening the channel decreases its resistance, causing an increase in current with increase in drain bias for a MOSFET operating in saturation. The effect

is more pronounced the shorter the source-to-drain separation, the deeper the drain junction, and the thicker the oxide insulator.

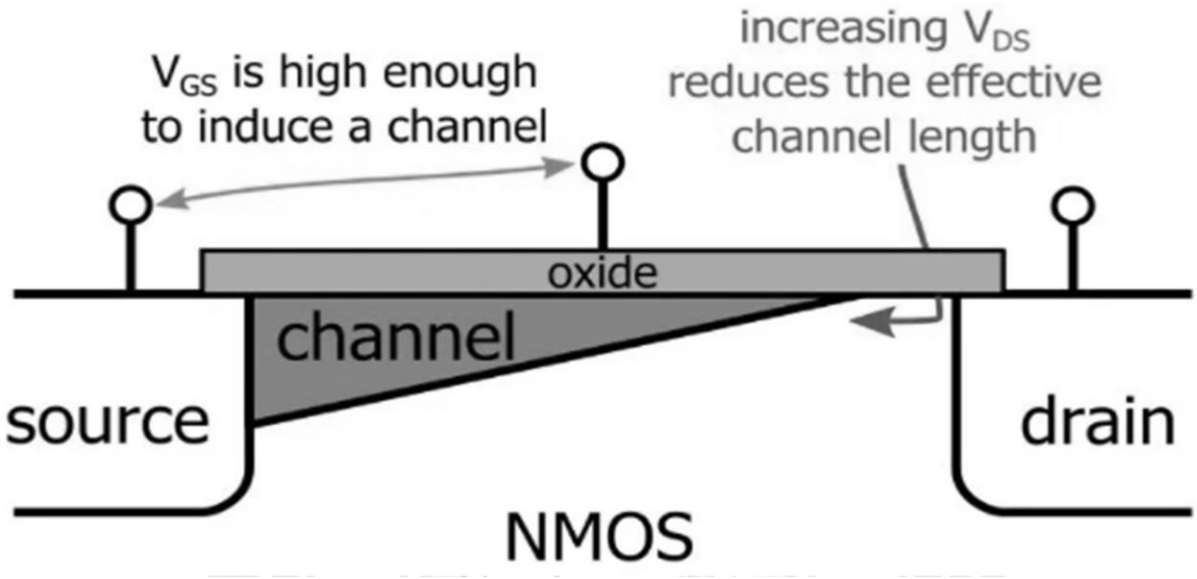

Fig:3.4.2 Channel-Length Modulation

In the weak inversion region, the influence of the drain analogous to channel-length modulation leads to poorer device turn off behavior known as drain-induced barrier lowering, a drain induced lowering of threshold voltage.

In bipolar devices, a similar increase in current is seen with increased collector voltage due to base-narrowing, known as the Early effect. The similarity in effect upon the current has led to use of the term "Early effect" for MOSFETs as well, as an alternative name for "channel-length modulation".

The effect of channel-length modulation upon the MOSFET output resistance varies both with the device, particularly its channel length, and with the applied bias. The main factor affecting the output resistance in longer MOSFETs is channel length modulation as just described. In shorter MOSFETs additional factors arise such as: drain-induced barrier lowering (which lowers the threshold voltage, increasing the current and decreasing the output resistance), velocity saturation (which tends to limit the increase in channel current with drain voltage, thereby increasing the output resistance) and ballistic transport (which modifies the collection of current by the drain, and modifies drain-induced barrier lowering so as to increase supply of carriers to the pinch-off region, increasing the current and decreasing the output resistance).

3.3 Comparison of MOSFET with JFET

BASIS OF COMPARISON	JFET	MOSFET
Acronym For	JFET stands for Junction Field Effect Transistor.	MOSFET stands for Metal Oxide Semiconductor Field Effect Transistor.
Operation	It can only be operated in the depletion mode	It can be operated in either depletion or in enhancement mode
Input Impedance	It has input impedance of (~10^8 Ω) which is very much lower than that of MOSFETs.	It has input impedance of (~10^10 Ω to 10^15 Ω) which is very much higher than that of JFETs.
Gate Leakage Current	The gate leakage current of JFET is of the order of nanoAMPs (10^-9 A).	The gate leakage current of MOSFET is in order of PicoAMPs (10^-12 A).
Input Characteristics	The drain resistance of MOSFETs is lower than that of JFETs and therefore the output characteristics tend to be less flat (curved) than the JFETs.	The drain resistance of MOSFETs is lower than that of JFETs and therefore the output characteristics tend to be less flat than the JFETs.
Use	JFETs have been in use for a longer period of time and therefore they have slowly been replaced in many of its original use cases by more modern devices like the CMOS OpAmp.	MOSFETs are generally popular around the globe and therefore they have an important component in most of the integrated circuits.
Fabrication Process	JFETs are simpler to fabricate and thus they are very much available and cheaper in cost.	Addition of metal oxide layer to MOSFETs, make the fabrication process complex and sophisticated, therefore they are comparatively expensive to JFETs.
Application	JFETs are perfect for use in low noise applications such as electronic switches, buffer amplifiers etc.	MOSFETs are mainly used for high noise applications such as switching and amplifying analog or digital signals. Also, they are used in embedded systems and motor controlled applications.

UNIT III FIELD EFFECT TRANSISTORS

3.1 JUNCTION FIELD EFFECT TRANSISTOR (JFET)

There are two basic configurations of junction field effect transistor, the N-channel JFET and the P-channel JFET. The N-channel JFET's channel is doped with donor impurities meaning that the flow of current through the channel is negative (hence the term N-channel) in the form of electrons.

Likewise, the P-channel JFET's channel is doped with acceptor impurities meaning that the flow of current through the channel is positive (hence the term P-channel) in the form of holes. N-channel JFET's have a greater channel conductivity (lower resistance) than their equivalent P-channel types, since electrons have a higher mobility through a conductor compared to holes. This makes the N-channel JFET's a more efficient conductor compared to their P-channel counterparts.

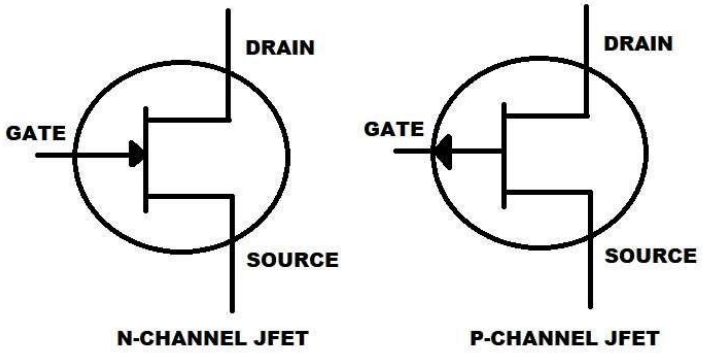

Fig:3.1.1 Symbol of N-Channel and P-Channel JFET

There are two ohmic electrical connections at either end of the channel called the Drain and the Source. But within this channel there is a third electrical connection which is called the Gate terminal and this can also be a P-type or N-type material forming a PN-junction with the main channel.

Construction

The semiconductor "channel" of the Junction Field Effect Transistor is a resistive path through which a voltage VDS causes a current ID to flow and as such the junction

field effect transistor can conduct current equally well in either direction. As the channel is resistive in nature, a voltage gradient is thus formed down the length of the channel with this voltage becoming less positive as go from the Drain terminal to the Source terminal.

The result is that the PN-junction therefore has a high reverse bias at the Drain terminal and a lower reverse bias at the Source terminal. This bias causes a "depletion layer" to be formed within the channel and whose width increases with the bias.

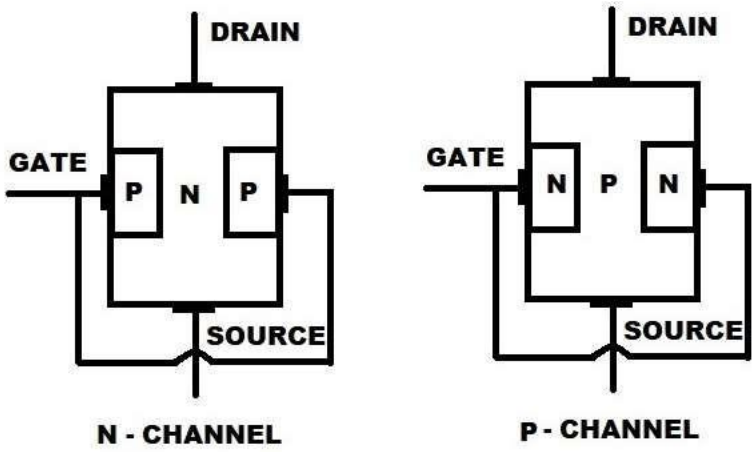

Fig:3.1.2 Construction of N-Channel and P-Channel JFET

The magnitude of the current flowing through the channel between the Drain and the Source terminals is controlled by a voltage applied to the Gate terminal, which is a reverse-biased. In an N-channel JFET this Gate voltage is negative while for a P-channel JFET the Gate voltage is positive.

The main difference between the JFET and a BJT device is that when the JFET junction is reverse-biased the Gate current is practically zero, whereas the Base current of the BJT is always some value greater than zero.

Biasing of N-channel JFET

The cross sectional diagram above shows an N-type semiconductor channel with a P-type region called the Gate diffused into the N-type channel forming a reverse biased PN-junction and it is this junction which forms the depletion region around the Gate area

when no external voltages are applied. JFETs are therefore known as depletion mode devices.

This depletion region produces a potential gradient which is of varying thickness around the PN-junction and restrict the current flow through the channel by reducing its effective width and thus increasing the overall resistance of the channel itself.

The most-depleted portion of the depletion region is in between the Gate and the Drain, while the least-depleted area is between the Gate and the Source. Then the JFET's channel conducts with zero bias voltage applied (ie, the depletion region has near zero width).

With no external Gate voltage (VG = 0), and a small voltage (VDS) applied between the Drain and the Source, maximum saturation current (IDSS) will flow through the channel from the Drain to the Source restricted only by the small depletion region around the junctions.

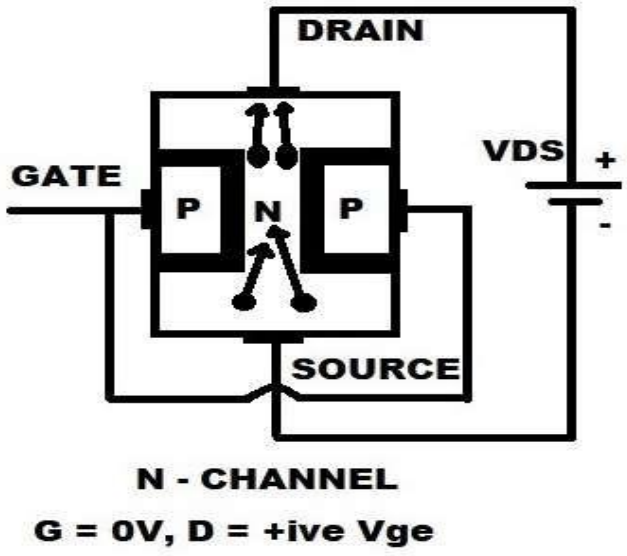

Fig:3.1.3 Working of N-Channel JFET (Gate = 0V, Drain = +ive Vge)

If a small negative voltage (-VGS) is now applied to the Gate the size of the depletion region begins to increase reducing the overall effective area of the channel and thus reducing the current flowing through it, a sort of "squeezing" effect takes place. So

by applying a reverse bias voltage increases the width of the depletion region which in turn reduces the conduction of the channel.

Since the PN-junction is reverse biased, little current will flow into the gate connection. As the Gate voltage (-VGS) is made more negative, the width of the channel decreases until no more current flows between the Drain and the Source and the FET is said to be “pinched-off” (similar to the cut-off region for a BJT). The voltage at which the channel closes is called the “pinch-off voltage”, (VP).

JFET Channel Pinched-off

In this pinch-off region the Gate voltage, VGS controls the channel current and VDS has little or no effect.

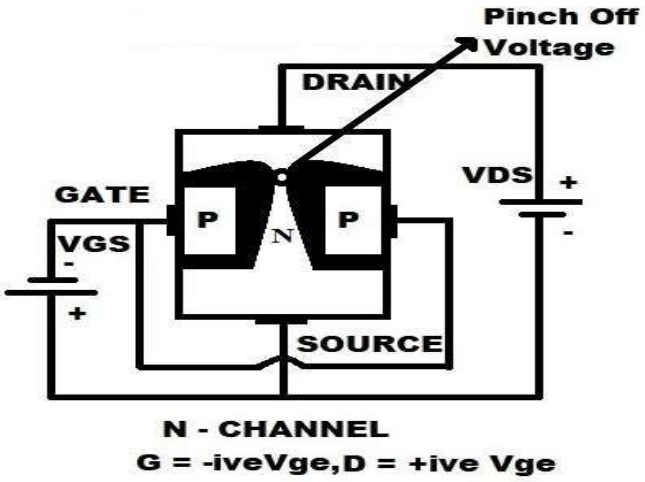

Fig:3.1.4 Working of N-Channel JFET (Gate = -ive Vge, Drain = +ive Vge)

The result is that the FET acts more like a voltage controlled resistor which has zero resistance when VGS = 0 and maximum “ON” resistance (RDS) when the Gate voltage is very negative. Under normal operating conditions, the JFET gate is always negatively biased relative to the source.

It is essential that the Gate voltage is never positive since if it is all the channel current will flow to the Gate and not to the Source, the result is damage to the JFET. Then to close the channel:

- No Gate Voltage (VGS) and VDS is increased from zero.
- No VDS and Gate control is decreased negatively from zero.
- VDS and VGS varying.

The P-channel Junction Field Effect Transistor operates exactly the same as the N-channel above, with the following exceptions: 1). Channel current is positive due to holes, 2). The polarity of the biasing voltage needs to be reversed.

Drain Characteristics

The drain characteristics of an N-channel JFET with the gate short-circuited to the source.

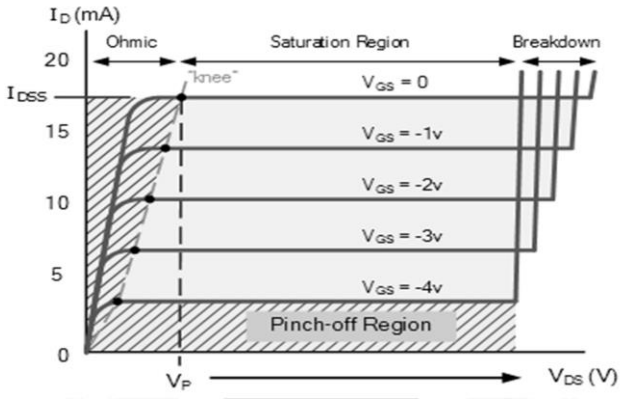

Fig:3.1.5 Drain Characteristics of N-Channel JFET

The voltage VGS applied to the Gate controls the current flowing between the Drain and the Source terminals. VGS refers to the voltage applied between the Gate and the Source while VDS refers to the voltage applied between the Drain and the Source.

Because a Junction Field Effect Transistor is a voltage controlled device, “NO current flows into the gate!” then the Source current (IS) flowing out of the device equals the Drain current flowing into it and therefore (ID = IS).

The characteristics curves example shown above, shows the four different regions of operation for a JFET and these are given as:

- Ohmic Region – When VGS = 0 the depletion layer of the channel is very small and the JFET acts like a voltage controlled resistor.

- Cut-off Region – This is also known as the pinch-off region were the Gate voltage, VGS is sufficient to cause the JFET to act as an open circuit as the channel resistance is at maximum.
- Saturation or Active Region – The JFET becomes a good conductor and is controlled by the Gate-Source voltage, (VGS) while the Drain-Source voltage, (VDS) has little or no effect.
- Breakdown Region – The voltage between the Drain and the Source, (VDS) is high enough to causes the JFET's resistive channel to break down and pass uncontrolled maximum current.

Transfer characteristics

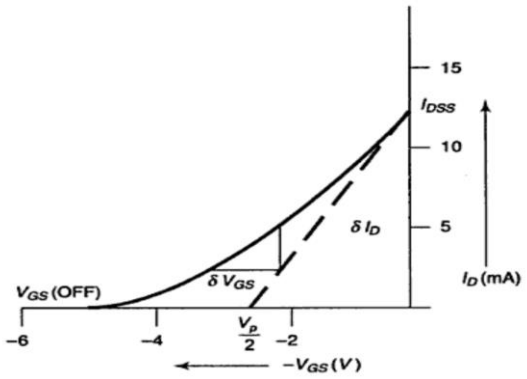

Fig:3.1.5 Transfer Characteristics of N-Channel JFET

The characteristics curves for a P-channel junction field effect transistor are the same as those above, except that the Drain current ID decreases with an increasing positive Gate-Source voltage, VGS.

The Drain current is zero when VGS = VP. For normal operation, VGS is biased to be somewhere between VP and 0. Then can calculate the Drain current, ID for any given bias point in the saturation or active region.

Drain current in the active region.

$$I_D = I_{DSS}\left[1-\frac{V_{GS}}{V_P}\right]^2$$

Note that the value of the Drain current will be between zero (pinch-off) and IDSS(maximum current). By knowing the Drain current ID and the Drain-Source voltage VDSthe resistance of the channel (ID) is given as:

Drain-Source channel resistance.

$$R_{DS} = \frac{\Delta V_{DS}}{\Delta I_D} = \frac{1}{g_m}$$

Where: gm is the "transconductance gain" since the JFET is a voltage controlled device and which represents the rate of change of the Drain current with respect to the change in Gate-Source voltage.

JFET Applications

- JFET is used as a switch.
- JFET is used as a chopper.
- Used as an amplifier.
- Used as a buffer.
- Used in the oscillatory circuits because of its low frequency drift.
- Used in communication equipments, such as FM and TV receivers because of their low modulation distortion.
- Used as voltage controlled resistors in operational amplifiers.
- JFETs are used in cascade amplifiers and in RF amplifiers.

3.2 METAL OXIDE SEMICONDUCTOR FIELD EFFECT TRANSISTOR (MOSFET)

MOSFET stands for Metal Oxide Silicon Field Effect Transistor or Metal Oxide Semiconductor Field Effect Transistor. This is also called as IGFET meaning Insulated Gate Field Effect Transistor. The FET is operated in both depletion and enhancement modes of operation.

Symbol of MOSFET

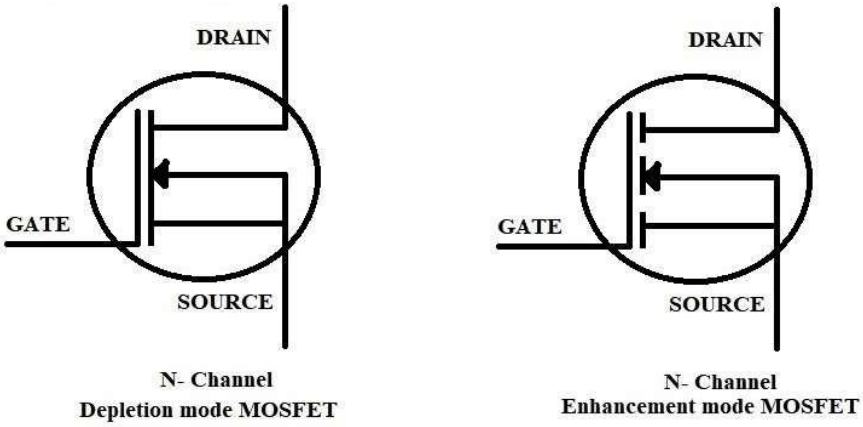

Fig:3.2.1 Symbol of N-Channel Depletion MOSFET and Enhancement MOSFET

The N-channel MOSFETs are simply called as NMOS. The symbols for N-channel MOSFET

Construction of N- Channel MOSFET

A lightly doped P-type substrate is taken into which two heavily doped N-type regions are diffused, which act as source and drain. Between these two N+ regions, there occurs diffusion to form an Nchannel, connecting drain and source.

A thin layer of Silicon dioxide (SiO2) is grown over the entire surface and holes are made to draw ohmic contacts for drain and source terminals. A conducting layer of aluminum is laid over the entire channel, upon this SiO2 layer from source to drain which constitutes the gate. The SiO2 substrate is connected to the common or ground terminals.

Because of its construction, the MOSFET has a very less chip area than BJT, which is 5% of the occupancy when compared to bipolar junction transistor. This device can be operated in modes. They are depletion and enhancement modes.

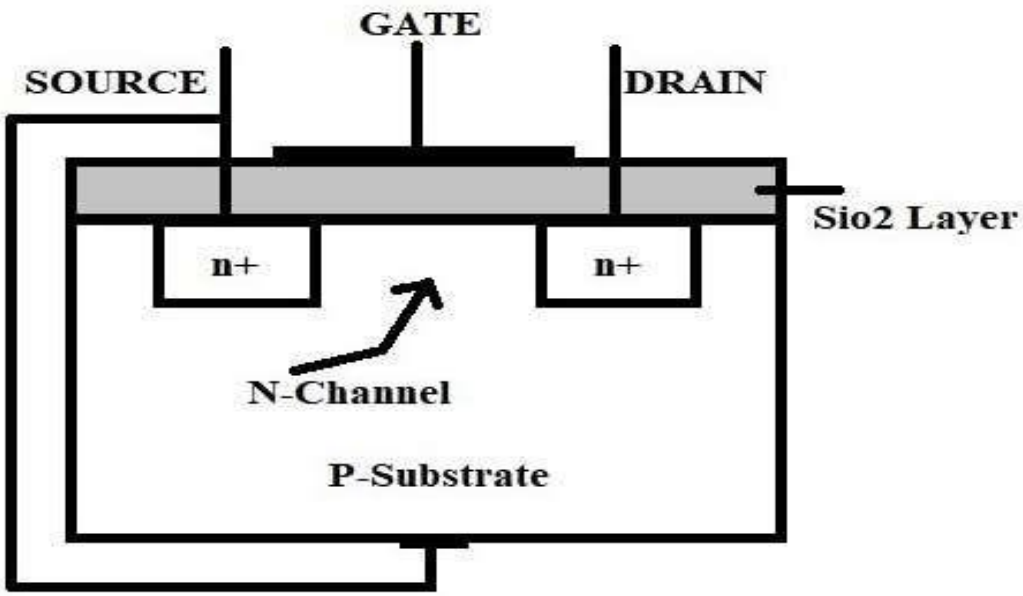

Fig:3.2.2 Construction of N-Channel MOSFET

Working of N-Channel MOSFET Enhancement Mode

The same MOSFET can be worked in enhancement mode, if we can change the polarities of the voltage VGG. So, let us consider the MOSFET with gate source voltage VGG being positive.

When no voltage is applied between gate and source, some current flows due to the voltage between drain and source. Let some positive voltage is applied at VGG. Then the minority carriers i.e. holes, get repelled and the majority carriers i.e. electrons gets attracted towards the SiO2 layer.

With some amount of positive potential at VGG a certain amount of drain current ID flows through source to drain. When this positive potential is further increased, the current ID increases due to the flow of electrons from source and these are pushed further due to the voltage applied at VGG. Hence the more positive the applied VGG, the more the value of drain current ID will be. The current flow gets enhanced due to the increase in electron flow better than in depletion mode. Hence this mode is termed as Enhanced Mode MOSFET.

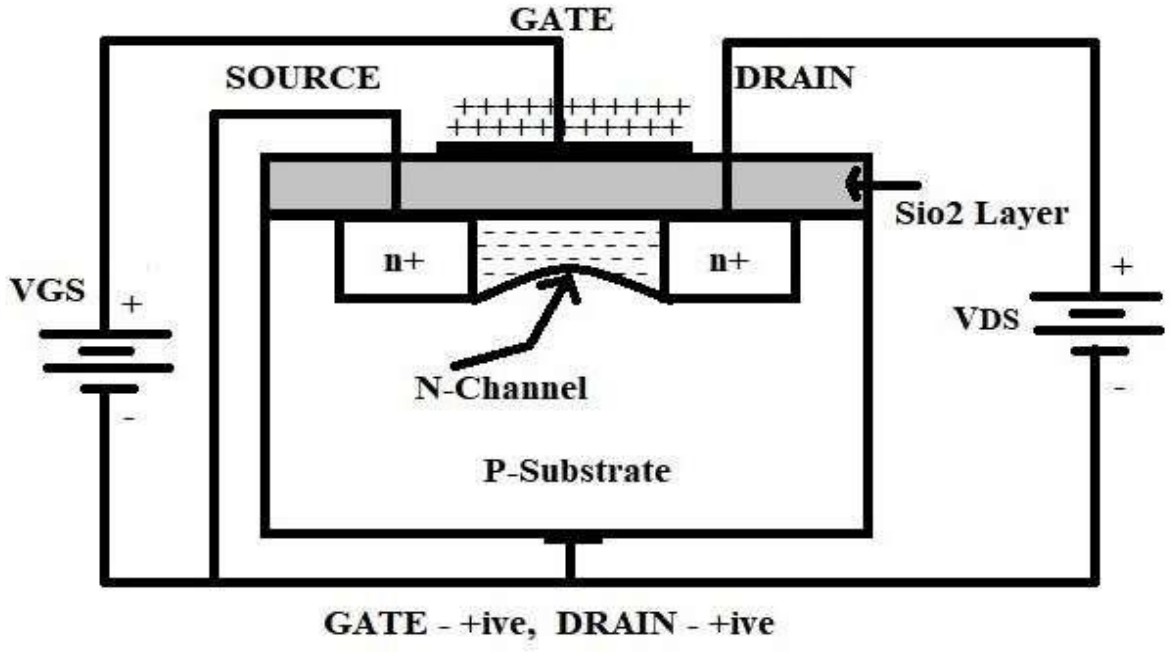

Fig:3.2.3 Working of N - Channel Enhancement mode MOSFET

Working of N - Channel depletion mode MOSFET

There is no PN junction present between gate and channel in this, unlike a FET. The diffused channel N between two N+ regions, the insulating dielectric SiO2 and the aluminum metal layer of the gate together form a parallel plate capacitor.

If the NMOS has to be worked in depletion mode, the gate terminal should be at negative potential while drain is at positive potential, as shown in the following figure.

When no voltage is applied between gate and source, some current flows due to the voltage between drain and source. Let some negative voltage is applied at VGG. Then the minority carriers i.e. holes, get attracted and settle near SiO2 layer. But the majority carriers, i.e., electrons get repelled.

With some amount of negative potential at VGG a certain amount of drain current ID flows through source to drain. When this negative potential is further increased, the electrons get depleted and the current ID decreases.

Hence the more negative the applied VGG, the lesser the value of drain current ID will be the channel nearer to drain gets more depleted than at source like in FET and the current flow decreases due to this effect. Hence it is called as depletion mode MOSFET.

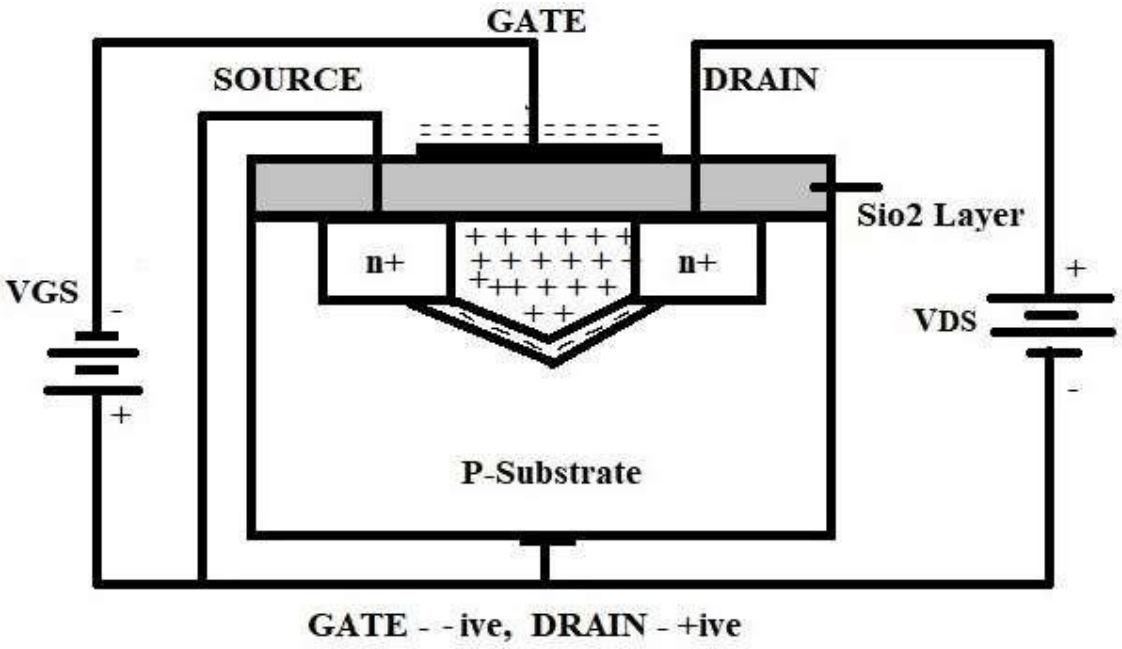

Fig:3.2.4 Working of N - Channel Depletion mode MOSFET

Drain Characteristics

The drain characteristics of a MOSFET are drawn between the drain current ID and the drain source voltage VDS. The characteristic curve is as shown below for different values of inputs.

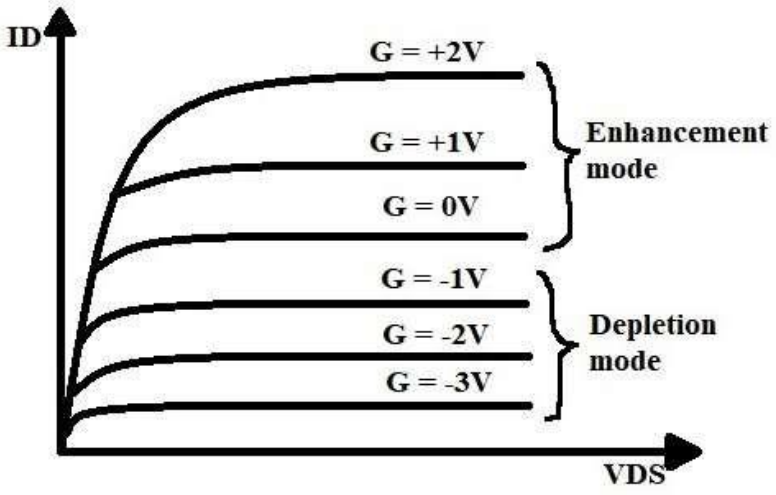

Fig:3.2.5 Drain Characteristics of N - Channel Depletion mode and Enhancement mode MOSFET

Actually when VDS is increased, the drain current ID should increase, but due to the applied VGS, the drain current is controlled at certain level. Hence the gate current controls the output drain current.

Transfer Characteristics

Transfer characteristics define the change in the value of VDS with the change in ID and VGS in both depletion and enhancement modes. The below transfer characteristic curve is drawn for drain current versus gate to source voltage.

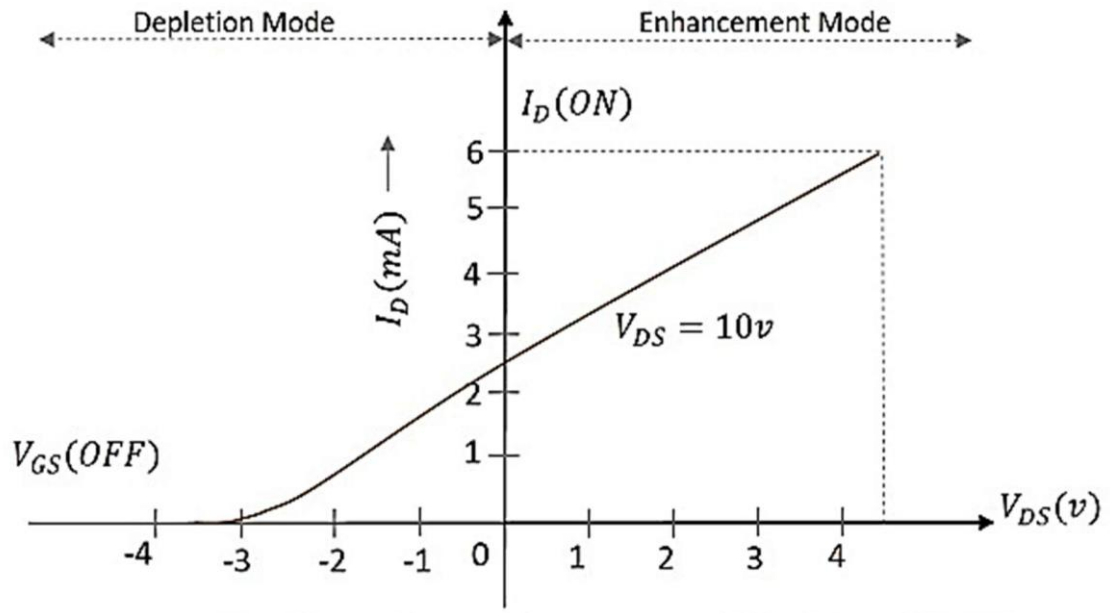

Fig:3.2.6 Transfer Characteristics of N - Channel Depletion mode and Enhancement mode MOSFET

Applications

- Amplifiers made of MOSFET are extremely employed in extensive frequency applications
- The regulation for DC motors are provided by these devices
- As because these have enhanced switching speeds, it acts as perfect for the construction of chopper amplifiers
- Functions as a passive component for various electronic elements.