2.4 COMMON BASE CONFIGURATION

In common base configuration, emitter is the input terminal, collector is the output terminal and base terminal is connected as a common terminal for both input and output. That means the emitter terminal and common base terminal are known as input terminals whereas the collector terminal and common base terminal are known as output terminals.

In common base configuration, the base terminal is grounded so the common base configuration is also known as grounded base configuration. Sometimes common base configuration is referred to as common base amplifier, CB amplifier, or CB configuration.

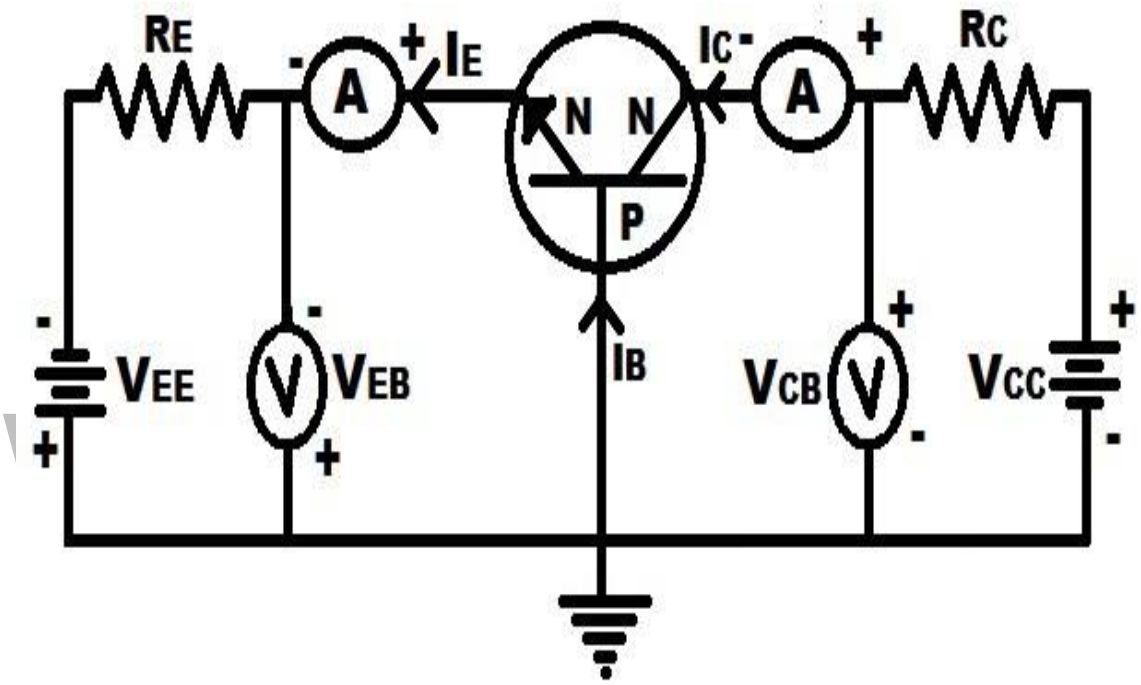

Fig:2.4.1 Common Base Configuration of NPN Transistor

The input signal is applied between the emitter and base terminals while the corresponding output signal is taken across the collector and base terminals. Thus the base terminal of a transistor is common for both input and output terminals and hence it is named as common base configuration.

The supply voltage between base and emitter is denoted by VBE while the supply voltage between collector and base is denoted by VCB.

In every configuration, the base-emitter junction JE is always forward biased and collector-base junction JC is always reverse biased. Therefore, in common base configuration, the base-emitter junction JE is forward biased and collector-base junction JC is reverse biased.

Input characteristics

The input characteristics describe the relationship between input current (IE) and the input voltage (VBE).

First, draw a vertical line and horizontal line. The vertical line represents y-axis and horizontal line represents x-axis. The input current or emitter current (IE) is taken along the y-axis (vertical line) and the input voltage (VBE) is taken along the x-axis (horizontal line).

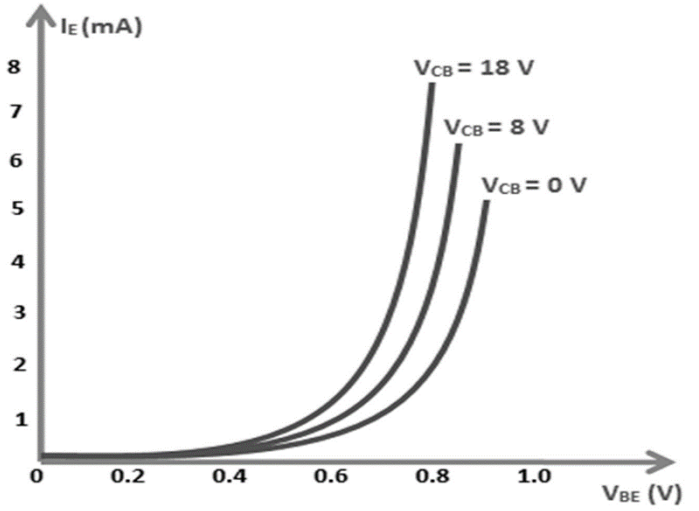

Fig:2.4.2 Input characteristics of Common Base Configuration

To determine the input characteristics, the output voltage VCB (collector-base voltage) is kept constant at zero volts and the input voltage VBE is increased from zero volts to different voltage levels. For each voltage level of the input voltage (VBE), the input current (IE) is recorded on a paper or in any other form.

A curve is then drawn between input current IE and input voltage VBE at constant output voltage VCB (0 volts).

The output voltage (VCB) is increased from zero volts to a certain voltage level (8 volts) and kept constant at 8 volts. While increasing the output voltage (VCB), the input voltage (VBE) is kept constant at zero volts. After kept the output voltage (VCB) constant at 8 volts, the input voltage VBE is increased from zero volts to different voltage levels. For each voltage level of the input voltage (VBE), the input current (IE) is recorded on a paper or in any other form.

A curve is then drawn between input current IE and input voltage VBE at constant output voltage VCB (8 volts).

This is repeated for higher fixed values of the output voltage (VCB).

When output voltage (VCB) is at zero volts and emitter-base junction JE is forward biased by the input voltage (VBE), the emitter-base junction acts like a normal p-n junction diode. So the input characteristics are same as the forward characteristics of a normal pn junction diode.

The cut in voltage of a silicon transistor is 0.7 volts and germanium transistor is 0.3 volts. In our case, it is a silicon transistor. So from the above graph, can see that after 0.7 volts, a small increase in input voltage (VBE) will rapidly increase the input current (IE).

When the output voltage (VCB) is increased from zero volts to a certain voltage level (8 volts), the emitter current flow will be increased which in turn reduces the depletion region width at emitter-base junction. As a result, the cut in voltage will be reduced. Therefore, the curves shifted towards the left side for higher values of output voltage VCB.

Output characteristics

The output characteristics describe the relationship between output current (IC) and the output voltage (VCB).

First, draw a vertical line and a horizontal line. The vertical line represents y-axis and horizontal line represents x-axis. The output current or collector current (IC) is taken along the y-axis (vertical line) and the output voltage (VCB) is taken along the x-axis (horizontal line).

To determine the output characteristics, the input current or emitter current IE is kept constant at zero mA and the output voltage VCB is increased from zero volts to different voltage levels. For each voltage level of the output voltage VCB, the output current (IC) is recorded.

A curve is then drawn between output current IC and output voltage VCB at constant input current IE (0 mA).

When the emitter current or input current IE is equal to 0 mA, the transistor operates in the cut-off region.

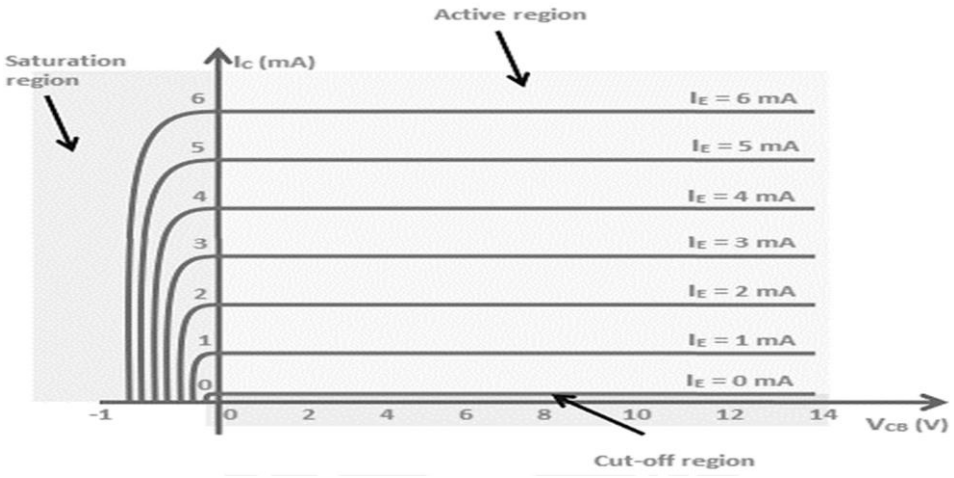

Fig:2.4.3 Output characteristics of Common Base Configuration

Next, the input current (IE) is increased from 0 mA to 1 mA by adjusting the input voltage VBE and the input current IE is kept constant at 1 mA. While increasing the input current IE, the output voltage VCB is kept constant.

After kept the input current (IE) constant at 1 mA, the output voltage (VCB) is increased from zero volts to different voltage levels. For each voltage level of the output voltage (VCB), the output current (IC) is recorded.

A curve is then drawn between output current IC and output voltage VCB at constant input current IE (1 mA). This region is known as the active region of a transistor.

This is repeated for higher fixed values of input current IE (I.e. 2 mA, 3 mA, 4 mA and so on).

From the above characteristics, can see that for a constant input current IE, when the output voltage VCB is increased, the output current IC remains constant.

At saturation region, both emitter-base junction JE and collector-base junction JCare forward biased. From the above graph, can see that a sudden increase in the collector current when the output voltage VCB makes the collector-base junction JC forward biased.

Early effect

Due to forward bias, the base-emitter junction JE acts as a forward biased diode and due to reverse bias, the collector-base junction JC acts as a reverse biased diode. Therefore, the width of the depletion region at the base-emitter junction JE is very small whereas the width of the depletion region at the collector-base junction JC is very large.

If the output voltage VCB applied to the collector-base junction JC is further increased, the depletion region width further increases. The base region is lightly doped as compared to the collector region. So the depletion region penetrates more into the base region and less into the collector region. As a result, the width of the base region decreases. This dependency of base width on the output voltage (VCB) is known as an early effect.

If the output voltage VCB applied to the collector-base junction JC is highly increased, the base width may be reduced to zero and causes a voltage breakdown in the transistor. This phenomenon is known as punch through.

Transistor parameters

Dynamic input resistance (ri)

Dynamic input resistance is defined as the ratio of change in input voltage or emitter voltage (VBE) to the corresponding change in input current or emitter current (IE), with the output voltage or collector voltage (VCB) kept at constant.

$$r_i = \frac{\Delta V_{BE}}{\Delta I_E}, \qquad V_{CB} = \text{constant}$$

The input resistance of common base amplifier is very low.

Dynamic output resistance (ro)

Dynamic output resistance is defined as the ratio of change in output voltage or collector voltage (VCB) to the corresponding change in output current or collector current (IC), with the input current or emitter current (IE) kept at constant.

$$r_o = \frac{\Delta V_{CB}}{\Delta I_C}, \qquad I_E = \text{constant}$$

The output resistance of common base amplifier is very high.

Current gain (α)

The current gain of a transistor in CB configuration is defined as the ratio of output current or collector current (IC) to the input current or emitter current (IE).

$$\alpha = \frac{I_C}{I_E}$$

The current gain of a transistor in CB configuration is less than unity. The typical current gain of a common base amplifier is 0.98.

2.5 COMMON COLLECTOR CONFIGURATION

In this configuration, the base terminal of the transistor serves as the input, the emitter terminal is the output and the collector terminal is common for both input and output. Hence, it is named as common collector configuration. The input is applied between the base and collector while the output is taken from the emitter and collector.

In common collector configuration, the collector terminal is grounded so the common collector configuration is also known as grounded collector configuration.

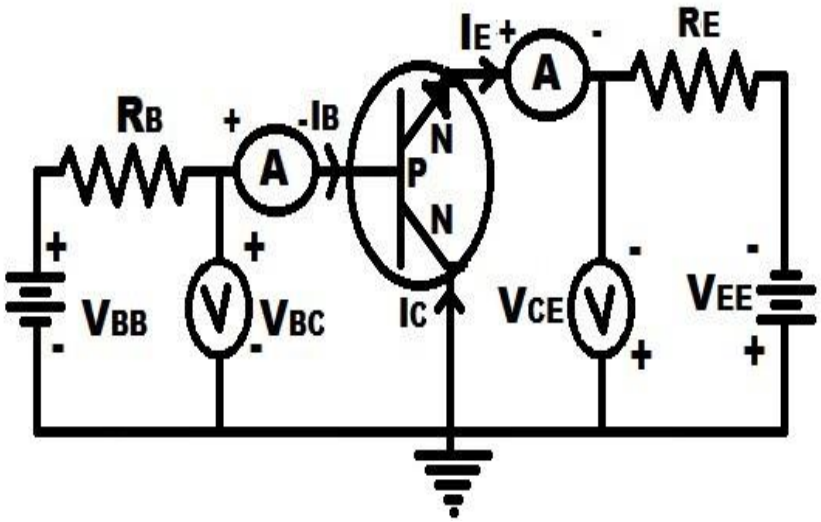

Fig:2.5.1 Common Collector Configuration of NPN Transistor

Sometimes common collector configuration is also referred to as emitter follower, voltage follower, common collector amplifier, CC amplifier, or CC configuration. This configuration is mostly used as a voltage buffer.

The input supply voltage between base and collector is denoted by VBC while the output voltage between emitter and collector is denoted by VEC.

In this configuration, input current or base current is denoted by IB and output current or emitter current is denoted by IE. The common collector amplifier has high input impedance and low output impedance. It has low voltage gain and high current gain.

The power gain of the common collector amplifier is medium. To fully describe the behavior of a transistor with CC configuration, need two set of characteristics input characteristics and output characteristics.

Input characteristics

The input characteristics describe the relationship between input current or base current (IB) and input voltage or base-collector voltage (VBC).

The input current or base current (IB) is taken along y-axis (vertical line) and the input voltage or base-collector voltage (VBC) is taken along x-axis (horizontal line).

To determine the input characteristics, the output voltage VEC is kept constant at 3V and the input voltage VBC is increased from zero volts to different voltage levels. For each level of input voltage VBC, the corresponding input current IB is noted. A curve is then drawn between input current IB and input voltage VBC at constant output voltage VEC (3V).

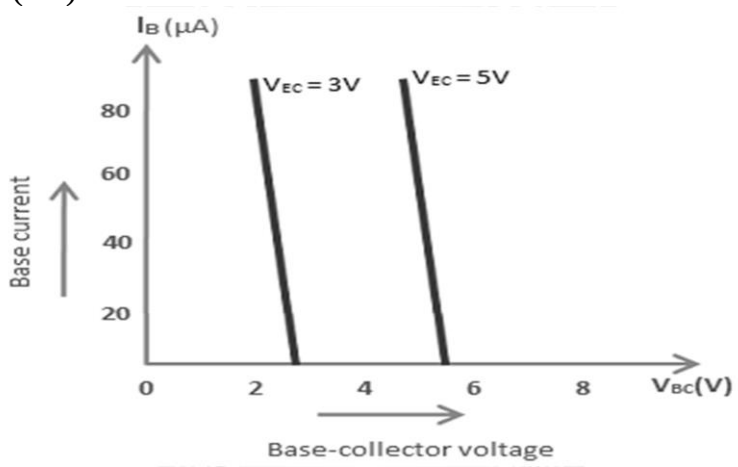

Fig:2.5.2 Input characteristics of Common Collector Configuration

Next, the output voltage VEC is increased from 3V to different voltage level, say for example 5V and then kept constant at 5V. While increasing the output voltage VEC, the input voltage VBC is kept constant at zero volts.

After kept the output voltage VEC constant at 5V, the input voltage VBC is increased from zero volts to different voltage levels. For each level of input voltage VBC, the corresponding input current IB is noted. A curve is then drawn between input current IB and input voltage VBC at constant output voltage VEC (5V).

This process is repeated for higher fixed values of output voltage (VEC).

Output characteristics

The output characteristics describe the relationship between output current or emitter current (IE) and output voltage or emitter-collector voltage (VEC).

The output current or emitter current (IE) is taken along y-axis (vertical line) and the output voltage or emitter-collector voltage (VEC) is taken along x-axis (horizontal line).

To determine the output characteristics, the input current IB is kept constant at zero micro amperes and the output voltage VEC is increased from zero volts to different voltage levels. For each level of output voltage VEC, the corresponding output current IE is noted. A curve is then drawn between output current IE and output voltage VEC at constant input current IB (0 μA).

Next, the input current (IB) is increased from 0 μA to 20 μA and then kept constant at 20 μA. While increasing the input current (IB), the output voltage (VEC) is kept constant at 0 volts.

After kept the input current (IB) constant at 20 μA, the output voltage (VEC) is increased from zero volts to different voltage levels. For each level of output voltage (VEC), the corresponding output current (IE) is recorded. A curve is then drawn between output current IE and output voltage VEC at constant input current IB (20μA). This region is known as the active region of a transistor.

This process is repeated for higher fixed values of input current IB (I.e. 40 μA, 60 μA, 80 μA and so on).

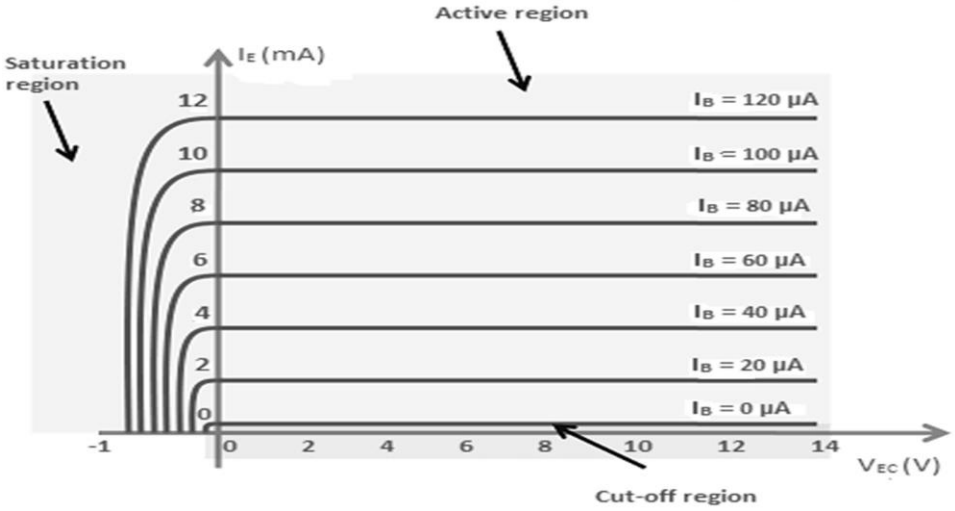

Fig:2.5.3 Output characteristics of Common Collector Configuration

In common collector configuration, if the input current or base current is zero then the output current or emitter current is also zero. As a result, no current flows through the transistor. So the transistor will be in the cutoff region. If the base current is slightly increased, then the output current or emitter current also increases. So the transistor falls into the active region. If the base current is heavily increased, then the current flowing through the transistor also heavily increases. As a result, the transistor falls into the saturation region.

Transistor parameters

Dynamic input resistance (ri)

Dynamic input resistance is defined as the ratio of change in input voltage or base voltage (VBC) to the corresponding change in input current or base current (IB), with the output voltage or emitter voltage (VEC) kept at constant.

$$r_i = \frac{\Delta V_{BC}}{\Delta I_B}, \qquad V_{EC} = \text{constant}$$

The input resistance of common collector amplifier is high.

Dynamic output resistance (ro)

Dynamic output resistance is defined as the ratio of change in output voltage or emitter voltage (VEC) to the corresponding change in output current or emitter current (IE), with the input current or base current (IB) kept at constant. The output resistance of common collector amplifier is low.

$$r_o = \frac{\Delta V_{EC}}{\Delta I_E}, \qquad I_B = \text{constant}$$

Current amplification factor (γ)

The current amplification factor is defined as the ratio of change in output current or emitter current IE to the change in input current or base current IB. It is expressed by γ.

$$\gamma = \frac{\Delta I_E}{\Delta I_B}$$

The current gain of a common collector amplifier is high.

2.3 COMMON EMITTER CONFIGURATION

A transistor is a three terminal device. The terminals are emitter, base, collector. In common emitter configuration, input voltage is applied between base and emitter terminals and output is taken across the collector and emitter terminals. Therefore, the emitter terminal is common to both input and output.

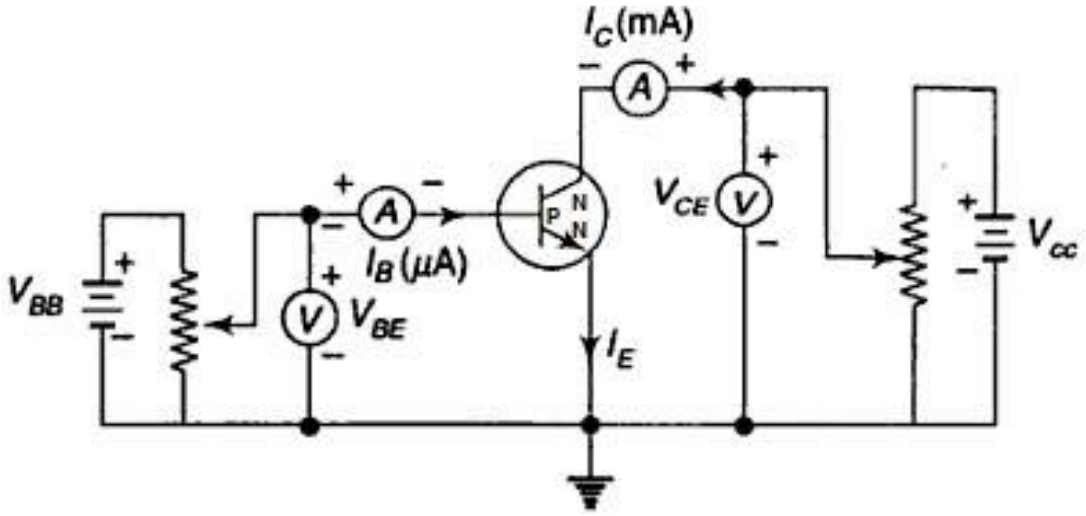

Fig:2.3.1 Common Emitter Configuration of NPN Transistor

Input characteristics

The input characteristics describe the relationship between input current or base current (IB) and input voltage or base-emitter voltage (VBE).

First, draw a vertical line and a horizontal line. The vertical line represents y-axis and horizontal line represents x-axis. The input current or base current (IB) is taken along y-axis (vertical line) and the input voltage (VBE) is taken along x-axis (horizontal line).

To determine the input characteristics, the output voltage VCE is kept constant at zero volts and the input voltage VBE is increased from zero volts to different voltage levels. For each voltage level of input voltage (VBE), the corresponding input current (IB) is recorded.

A curve is then drawn between input current IB and input voltage VBE at constant output voltage VCE (0 volts). Next, the output voltage (VCE) is increased from zero volts to certain voltage level (10 volts) and the output voltage (VCE) is kept constant at 10 volts. While increasing the output voltage (VCE), the input voltage (VBE) is kept constant at zero volts. After kept the output voltage (VCE) constant at 10 volts, the input

voltage VBE is increased from zero volts to different voltage levels. For each voltage level of input voltage (VBE), the corresponding input current (IB) is recorded.

A curve is then drawn between input current IB and input voltage VBE at constant output voltage VCE (10 volts). This process is repeated for higher fixed values of output voltage (VCE). When output voltage (VCE) is at zero volts and emitter-base junction is forward biased by input voltage (VBE), the emitter-base junction acts like a normal p-n junction diode. So the input characteristics of the CE configuration is same as the characteristics of a normal pn junction diode.

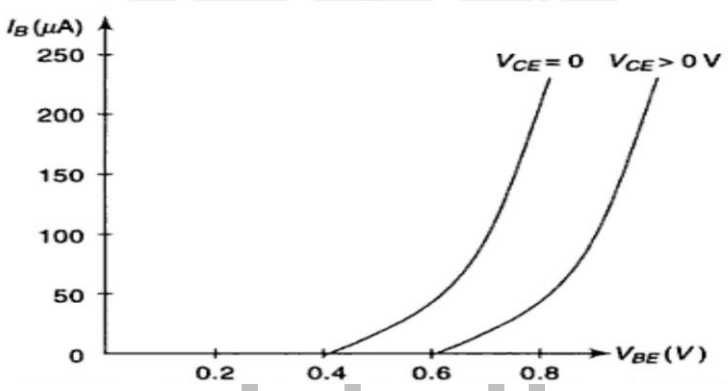

Fig:2.3.2 Input characteristics of Common Emitter Configuration

The cut in voltage of a silicon transistor is 0.7 volts and germanium transistor is 0.3 volts. In our case, it is a silicon transistor. So from the above graph, after 0.7 volts, a small increase in input voltage (VBE) will rapidly increases the input current (IB).

In common emitter (CE) configuration, the input current (IB) is very small as compared to the input current (IE) in common base (CB) configuration. The input current in CE configuration is measured in microamperes (μA) whereas the input current in CB configuration is measured in milliamperes (mA).

In common emitter (CE) configuration, the input current (IB) is produced in the base region which is lightly doped and has small width. So the base region produces only a small input current (IB). On the other hand, in common base (CB) configuration, the input current (IE) is produced in the emitter region which is heavily doped and has large width. So the emitter region produces a large input current (IE). Therefore, the input current (IB) produced in the common emitter (CE) configuration is small as compared to the common base (CB) configuration.

Due to forward bias, the emitter-base junction acts as a forward biased diode and due to reverse bias, the collector-base junction acts as a reverse biased diode. Therefore, the width of the depletion region at the emitter-base junction is very small whereas the width of the depletion region at the collector-base junction is very large.

If the output voltage VCE applied to the collector-base junction is further increased, the depletion region width further increases. The base region is lightly doped as compared to the collector region. So the depletion region penetrates more into the base region and less into the collector region. As a result, the width of the base region decreases which in turn reduces the input current (IB) produced in the base region.

From the above characteristics, for higher fixed values of output voltage VCE, the curve shifts to the right side. This is because for higher fixed values of output voltage, the cut in voltage is increased above 0.7 volts. Therefore, to overcome this cut in voltage, more input voltage VBE is needed than previous case.

Output characteristics

The output characteristics describe the relationship between output current (IC) and output voltage (VCE).

First, draw a vertical line and a horizontal line. The vertical line represents y-axis and horizontal line represents x-axis. The output current or collector current (IC) is taken along y-axis (vertical line) and the output voltage (VCE) is taken along x-axis (horizontal line).

To determine the output characteristics, the input current or base current IB is kept constant at 0 μA and the output voltage VCE is increased from zero volts to different voltage levels. For each level of output voltage, the corresponding output current (IC) is recorded.

A curve is then drawn between output current IC and output voltage VCE at constant input current IB (0 μA).

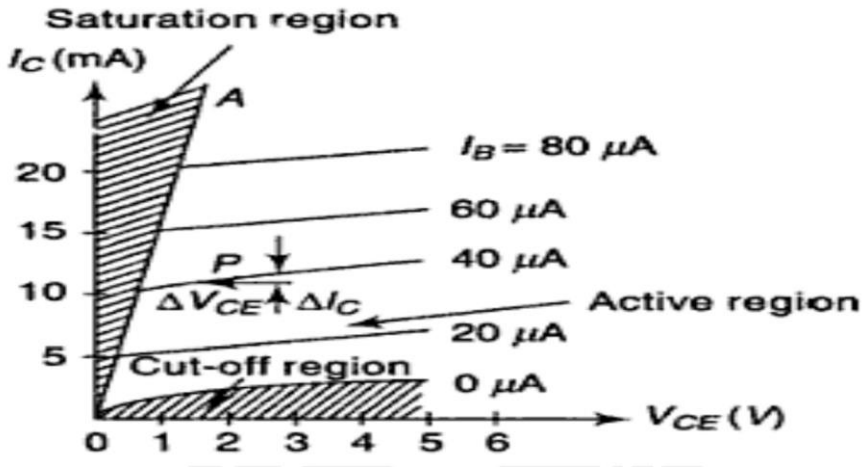

Fig:2.3.3 Output characteristics of Common Emitter Configuration

When the base current or input current IB = 0 μA, the transistor operates in the cut-off region. In this region, both junctions are reverse biased.

Next, the input current (IB) is increased from 0 μA to 20 μA by adjusting the input voltage (VBE). The input current (IB) is kept constant at 20 μA.

While increasing the input current (IB), the output voltage (VCE) is kept constant at 0 volts.

After kept the input current (IB) constant at 20 μA, the output voltage (VCE) is increased from zero volts to different voltage levels. For each voltage level of output voltage (VCE), the corresponding output current (IC) is recorded.

A curve is then drawn between output current IC and output voltage VCE at constant input current IB (20 μA). This region is known as the active region of a transistor. In this region, emitter-base junction is forward biased and the collector-base junction is reverse biased.

This steps are repeated for higher fixed values of input current IB (I.e. 40 μA, 60μA, 80 μA and so on).

Transistor parameters

Dynamic input resistance (ri)

Dynamic input resistance is defined as the ratio of change in input voltage or base voltage (VBE) to the corresponding change in input current or base current (IB), with the output voltage or collector voltage (VCE) kept at constant.

$$r_i = \frac{\Delta V_{BE}}{\Delta I_B}, \qquad V_{CE} = \text{constant}$$

In CE configuration, the input resistance is very low.

Dynamic output resistance (ro)

Dynamic output resistance is defined as the ratio of change in output voltage or collector voltage (VCE) to the corresponding change in output current or collector current (IC), with the input current or base current (IB) kept at constant.

$$r_o = \frac{\Delta V_{CE}}{\Delta I_C}, \qquad I_B = \text{constant}$$

In CE configuration, the output resistance is high.

Current gain (α)

The current gain of a transistor in CE configuration is defined as the ratio of output current or collector current (IC) to the input current or base current (IB).

$$\alpha = \frac{I_C}{I_B}$$

The current gain of a transistor in CE configuration is high. Therefore, the transistor in CE configuration is used for amplifying the current.

2.6 BASE WIDTH MODULATION OR EARLY EFFECT.

A change in the neutral base width will change the collector current as can be observed. A reduction in base width will cause the gradient in the minority carrier concentration to increase, which in turn causes an increase in the diffusion current. This effect is known as base width modulation; it is also called the Early effect.

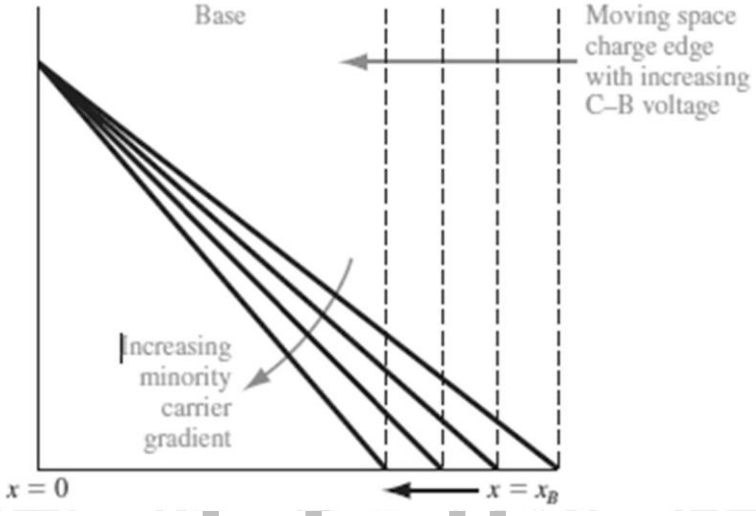

Fig:2.6.1 The change in the base width and the change in the minority carrier gradient as the B–C space charge width changes.
(Source : Semiconductor Physics and Devices)

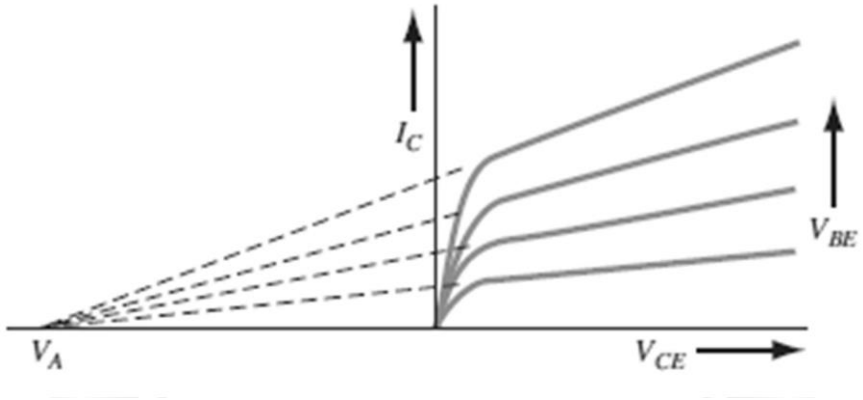

Fig:2.6.2 The collector current versus collector–emitter voltage showing the Early effect and Early voltage.
(Source : Semiconductor Physics and Devices)

2.8 GUMMEL–POON MODEL

The Gummel–Poon model of the BJT considers more physics of the transistor than the Ebers–Moll model. This model can be used if, for example, there is a nonuniform doping concentration in the base. The electron current density in the base of an npn transistor can be written as

$$J_n = e\mu_n n(x)\mathrm{E} + eD_n \frac{dn(x)}{dx}$$

An electric field will occur in the base if nonuniform doping exists in the base.

$$\mathrm{E} = \frac{kT}{e} \cdot \frac{1}{p(x)} \cdot \frac{dp(x)}{dx}$$

where p(x) is the majority carrier hole concentration in the base. Under low injection, the hole concentration is just the acceptor impurity concentration. The electric field is negative (from the collector to the emitter). The direction of this electric field aids the flow of electrons across the base.

$$J_n = e\mu_n n(x) \cdot \frac{kT}{e} \cdot \frac{1}{p(x)} \cdot \frac{dp(x)}{dx} + eD_n \frac{dn(x)}{dx}$$

Using Einstein's relation,

$$J_n = \frac{eD_n}{p(x)}\left[n(x)\frac{dp(x)}{dx} + p(x)\frac{dn(x)}{dx}\right] = \frac{eD_n}{p(x)} \cdot \frac{d(pn)}{dx}$$

Above can be written in the form

$$\frac{J_n p(x)}{eD_n} = \frac{d(pn)}{dx}$$

Integrating above Equation through the base region while assuming that the electron current density is essentially a constant and the diffusion coeffi cient is a constant,

$$\frac{J_n}{eD_n}\int_0^{x_B} p(x)\,dx = \int_0^{x_B} \frac{dp(x)}{dx}\,dx = p(x_B)n(x_B) - p(0)n(0)$$

Assuming that the B–E junction is forward biased and the B–C junction is reverse biased, $n(0) = n_{B0} \exp(V_{BE}/V_t)$ and $n(x_B) = 0$. Note that $n_{B0}p = ni^2$ so that Equation written as

$$J_n = \frac{-eD_n n_i^2 \exp(V_{BE}/V_t)}{\int_0^{x_B} p(x)\,dx}$$

The integral in the denominator is the total majority carrier charge in the base and is known as the base Gummel number, defined as Q_B. The hole current density in the emitter of an npn transistor can be expressed as

$$J_p = \frac{-eD_p n_i^2 \exp(V_{BE}/V_t)}{\int_0^{x_E} n(x')\,dx'}$$

The integral in the denominator is the total majority carrier charge in the emitter and is known as the emitter Gummel number, defi ned as QE.

Since the currents in the Gummel–Poon model are functions of the total integrated charges in the base and emitter, these currents can easily be determined for nonuniformly doped transistors.

The Gummel–Poon model can also take into account nonideal effects, such as the Early effect and high-level injection. As the B–C voltage changes, the neutral base width changes so that the base Gummel number Q_B changes. The change in Q_B with B–C voltage then makes the electron current density given by a function of the B–C voltage.

If the B–E voltage becomes too large, low injection no longer applies, which leads to high-level injection. In this case, the total hole concentration in the base increases because of the increased excess hole concentration. This means that the base Gummel number will increase.

The Gummel–Poon model can then be used to describe the basic operation of the transistor as well as to describe nonideal effects.

2.7 HYBRID-PI MODEL

Bipolar transistors are commonly used in circuits that amplify time-varying or sinusoidal signals. In these linear amplifier circuits, the transistor is biased in the forward-active region and small sinusoidal voltages and currents are superimposed on dc voltages and currents. The sinusoidal parameters are of interest, so it is convenient to develop a small-signal equivalent circuit of the bipolar transistor using the small-signal admittance parameters of the pn junction.

The C, B, and E terminals are the external connections to the transistor, while the C', B', and E' points are the idealized internal collector, base, and emitter regions.

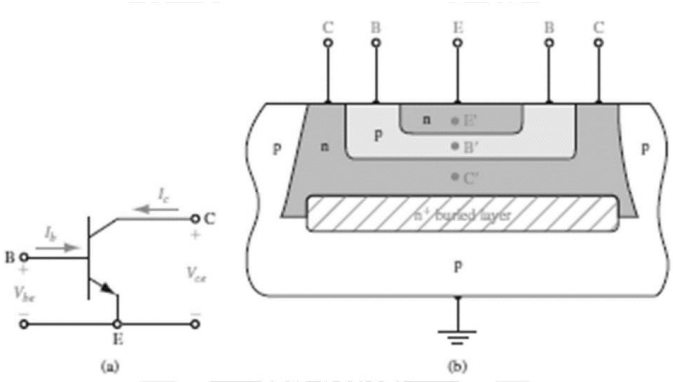

Fig:2.7.1 (a) Common-emitter npn bipolar transistor with small-signal current and voltages. (b) Cross section of an npn bipolar transistor for the hybrid-pi model. (Source : Semiconductor Physics and Devices)

The equivalent circuit between the external input base terminal and the external emitter terminal. The resistance r_b is the series resistance in the base between the external base terminal B and the internal base region B'. The B'-E' junction is forward biased, so $C\pi$ is the junction diffusion capacitance and r_π is the junction diffusion resistance.

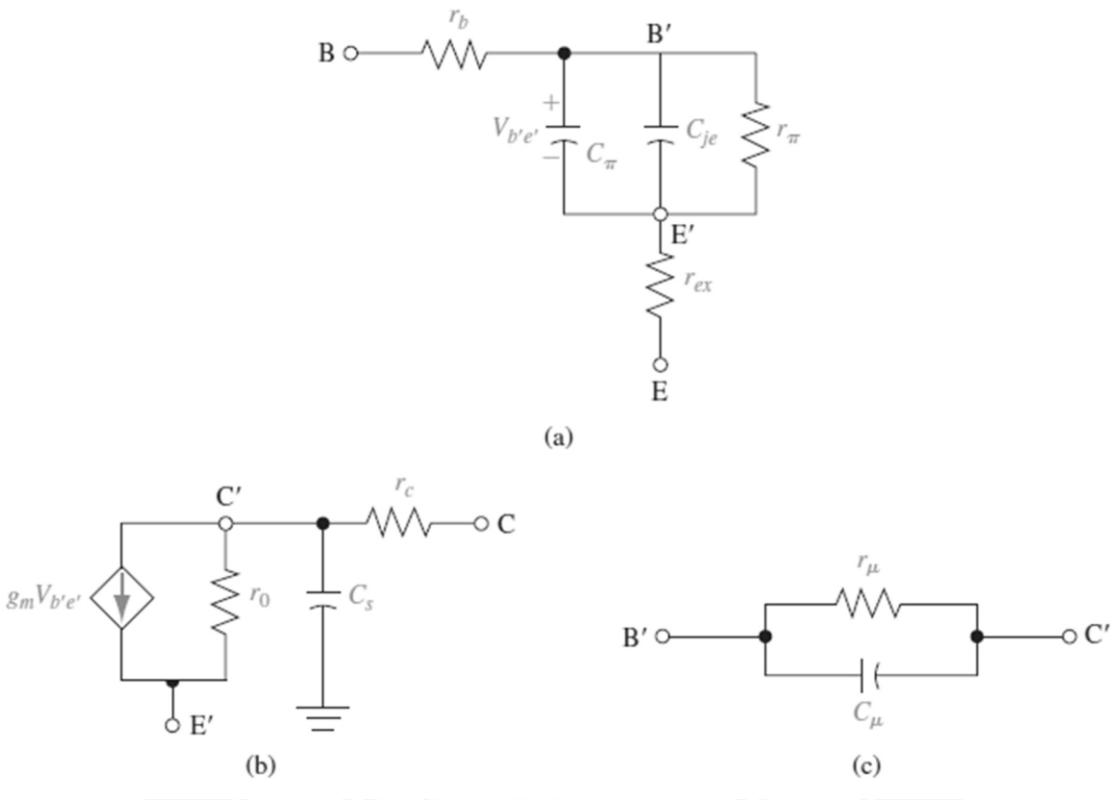

Fig:2.7.2 Components of the hybrid-pi equivalent circuit between (a) the base and emitter, (b) the collector and emitter, and (c) the base and collector.

(Source : Semiconductor Physics and Devices)

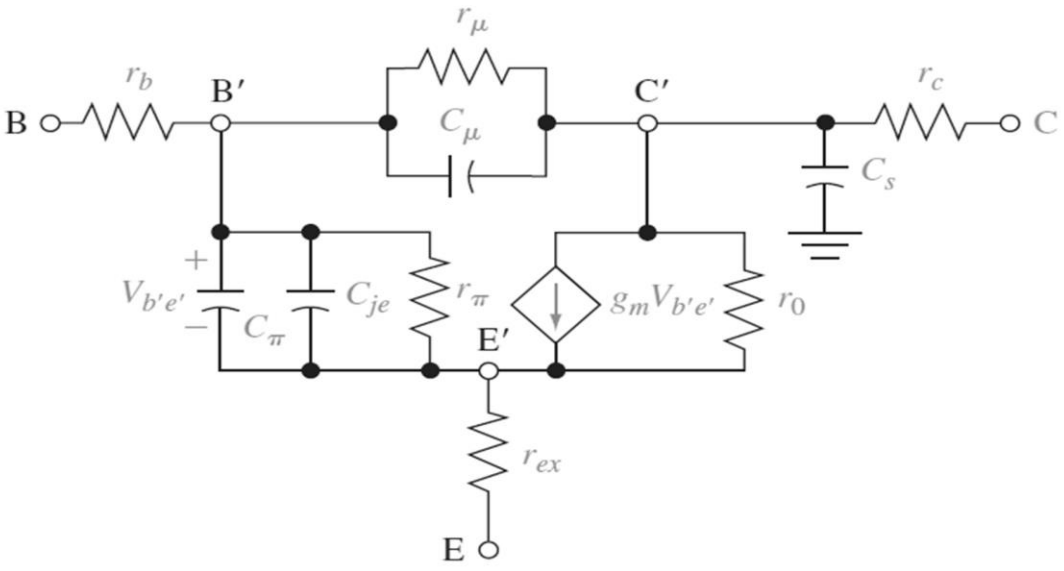

Fig:2.7.3 Hybrid-pi equivalent circuit.

(Source : Semiconductor Physics and Devices)

These two elements are in parallel with the junction capacitance, which is Cje. Finally, r_{ex} is the series resistance between the external emitter terminal and the internal emitter region. This resistance is usually very small and may be on the order of 1 to 2 Ω.

The r_c resistance is the series resistance between the external and internal collector connections and the capacitance C_s is the junction capacitance of the reverse-biased collector substrate junction. The dependent current source, $g_m V_{b'e'}$, is the collector current in the transistor, which is controlled by the internal base–emitter voltage. The resistance r_0 is the inverse of the output conductance g_0 and is primarily due to the Early effect.

The equivalent circuit of the reverse-biased B'-C' junction. The C_μ parameter is the reverse-biased junction capacitance and r_μ is the reverse-biased diffusion resistance. Normally, r_μ is on the order of mega ohms and can be neglected. The value of C_μ is usually much smaller than C_π but, because of the

feedback effect that leads to the Miller effect and Miller capacitance, C_μ cannot be ignored in most cases.

The Miller capacitance is the equivalent capacitance between B' and E' due to C_μ and the feedback effect, which includes the gain of the transistor. The Miller effect also reflects C_μ between the C' and E' terminals at the output. However, the effect on the output characteristics can usually be ignored.

2.9 MULTI EMITTER TRANSISTOR

When the input is HIGH, the emitter base junction of Q1 is reverse-biased and current flows through R, base collector junction of Q1, is forward-biased into the base of Q2. Thus, the collector of transistor Q1 operates as an emitter and the emitter as a collector and the transistor Q2 is pulled into saturation resulting in a LOW output. When the input is LOW, the emitter-base junction of Q1 is forward-biased. The charge stored in the base of flows through the collector of transistor Q1.

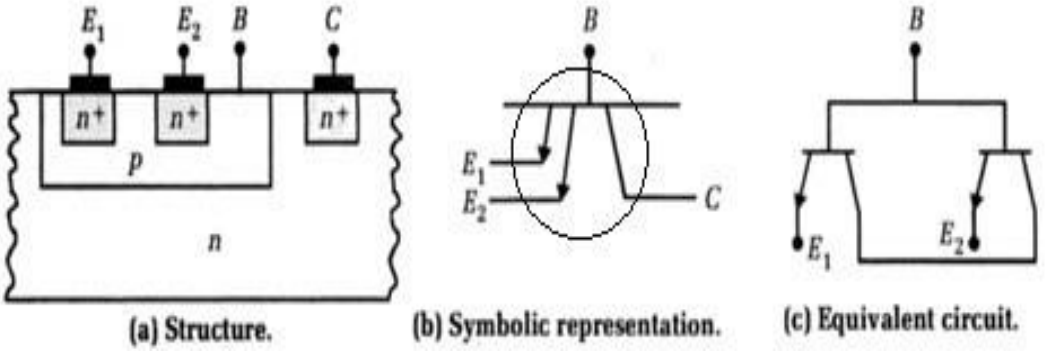

Fig:2.9.1 Multi Emitter Transistor

(Source : Linear Integrated Circuits)

When the input is HIGH, Q2 is in saturation with a base-to-ground voltage = 0.75V, indicating that the base-emitter junction of Q1 is reverse-biased. The transistor operates with an inverse common-base current gain α_I. Since it operates in the inversion region, the corresponding common-collector current gain is

$$h_{FC} = \frac{\alpha_I}{1-\alpha_I}$$

Designing low value of current gain minimizes the loading effect on the driving source when the input is HIGH. In order to achieve this,

UNIT II BIPOLAR JUNCTION TRANSISTORS

2.1 TRANSISTOR

A transistor is a type of a semiconductor device that can be used to both conduct and insulate electric current or voltage. A transistor basically acts as a switch and an amplifier. A transistor is a miniature device that is used to control or regulate the flow of electronic signals.

A typical transistor is composed of three layers of semiconductor materials or more specifically terminals which helps to make a connection to an external circuit and carry the current. A voltage or current that is applied to anyone pair of the terminals of a transistor controls the current through the other pair of terminals. There are three terminals for a transistor.

Emitter

Base

Collector

The very basic working principle of a transistor is based on controlling the flow of current through one channel by varying intensity of a very smaller current that is flowing through a second channel.

BIPOLAR JUNCTION TRANSISTOR (BJT)

The three terminals of BJT are base, emitter and collector. A very small current flowing between base and emitter can control a larger flow of current between the collector and emitter terminal.

There are two types of BJT.

P-N-P Transistor

It is a type of BJT where one n-type material is introduced or placed between two p-type materials. In such a configuration, the device will control the flow of current. PNP transistor consists of 2 crystal diodes which are connected in series. The right side and left side of the diodes are known as the collector-base diode and emitter-base diode respectively.

N-P-N Transistor

This transistor one p-type material that is present between two n-type materials. N-P-N transistor is basically used to amplify weak signals to strong signals. In NPN

transistor, the electrons move from the emitter to collector region resulting in the formation of current in the transistor. This transistor is widely used in the circuit.

NPN TRANSISTOR

An NPN transistor is the most commonly used bipolar junction transistor, and is constructed by sandwiching a P-type semiconductor between two N-type semiconductors. An NPN transistor has three terminals a collector, emitter and base. The NPN transistor behaves like two PN junction diodes connected back to back.

The Emitter is a region is used to supply charge carriers to the Collector via the Base region. The Collector region collects most of all charge carriers emitted from the Emitter. The Base region triggers and controls the amount of current flows through the Emitter to Collector.

Symbol of NPN Transistor

The NPN transistor has two junctions and three terminals. The arrowhead shows the conventional direction of Collector current (IC), Base current (IB) and Emitter current (IE).

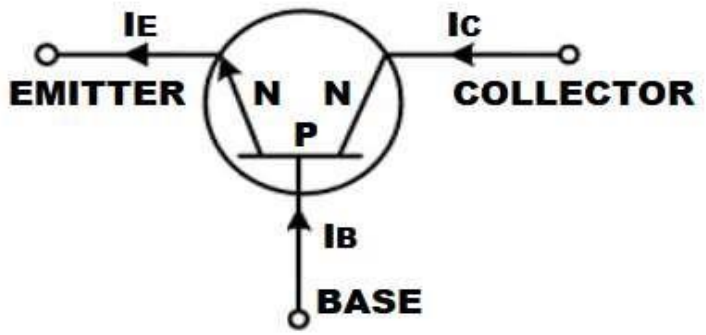

Fig:2.1.1 Symbol of NPN Transistor

Construction of NPN Transistor

The emitter and collector layers are wider compared to the base. The emitter is heavily doped. Therefore, it can inject a large number of charge carriers to the base.

The base is lightly doped and very thin compared to the other two regions. It passes most of all charge carriers to the collector which is emitted by the emitter.

The collector is moderately doped and collects charge carriers from the base layer.

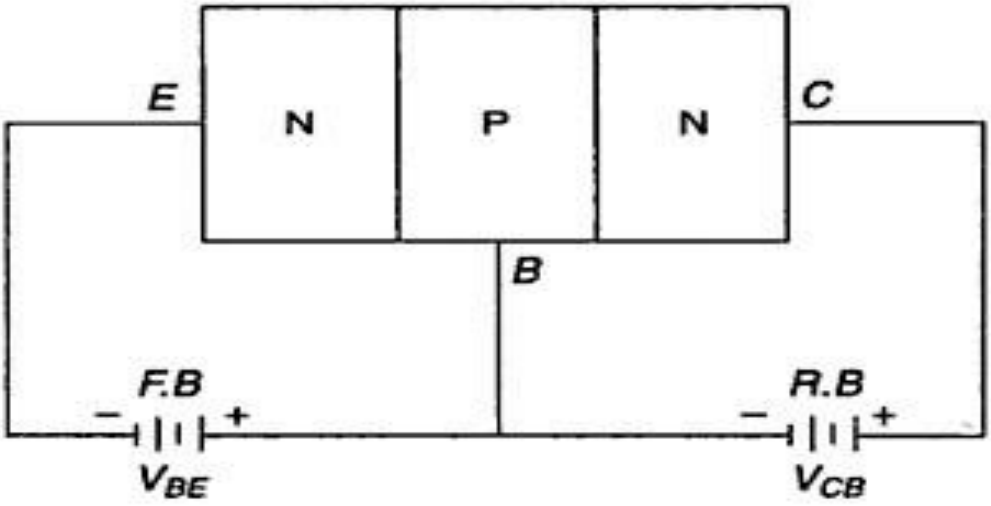

Fig:2.1.2 Construction of NPN Transistor

Working of NPN Transistor

The base-emitter junction is connected in the forward bias condition by supply voltage VEE. And the collector-base junction is connected in the reverse bias condition by supply voltage VCC.

In forward bias condition, the negative terminal of supply source (VEE) is connected to the N-type semiconductor (Emitter). Similarly, in a reverse bias condition, the positive terminal of the supply source (VCC) is connected to the N-type semiconductor (Collector).

The depletion region of the emitter-base region is thin compared to the depletion region of the collector-base junction (The depletion region is a region where no mobile charge carriers are present and it behaves like a barrier that opposes the flow of the current).

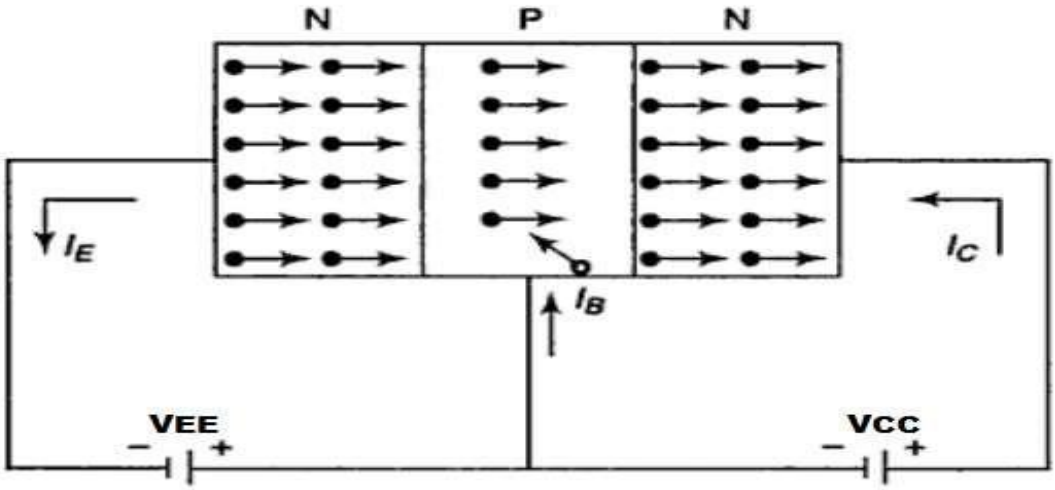

Fig:2.1.2 Working Principle of NPN Transistor

In N-type emitter, the majority charge carrier is electrons. Therefore, electrons start flowing from N-type emitter to a P-type base. And because of electrons, the current will start flowing the emitter-base junction. This current is known as emitter current IE.

These electrons move further to the base. The base is a P-type semiconductor. Therefore, it has holes. But the base region is very thin and lightly doped. So, it has a few holes to recombine with the electrons. Hence, most of the electrons will pass the base region and few of them will recombine with the holes.

Because of the recombination, the current will flow through the circuit and this current is known as base current IB. The base current is very small compared to the emitter current. Typically, it is 2-5% of the total emitter current.

Most of the electrons pass the depletion region of a collector-base junction and pass through the collector region. The current flowing by the remaining electrons is known as the collector current IC. The collector current is large compared to the base current.

2.2 PNP TRANSISTOR

A PNP transistor is a bipolar junction transistor constructed by sandwiching an N-type semiconductor between two P-type semiconductors. A PNP transistor has three terminals – a Collector (C), Emitter (E) and Base (B). The PNP transistor behaves like two PN junction diodes connected back to back.

Symbol of PNP Transistor

In P-type semiconductors, the majority charge carriers are holes. Therefore, in the PNP transistor, the formation of the current is due to the movement of holes.

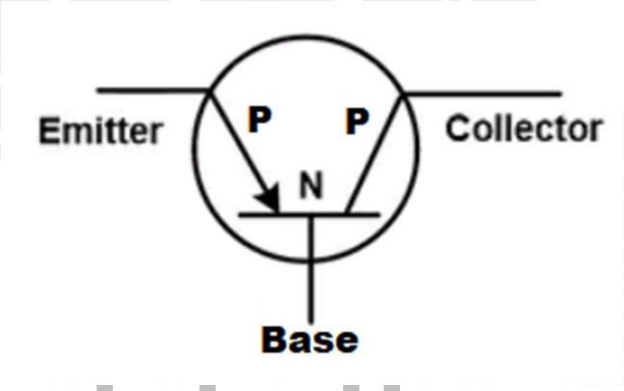

Fig:2.2.1 Symbol of PNP Transistor

The middle layer (N-type layer) is called the Base terminal (B). The left P-type layer works as an Emitter terminal (E) and the right P-type layer works as a Collector terminal (C).

Construction of PNP Transistor

The Emitter and Collector (P-type) layers are heavily doped compared to the Base (N-type) layer. Therefore, the depletion region at both junctions is more penetrate towards the Base layer. The area of the Emitter and Collector layer is more compared to the Base layer.

In N-type semiconductors, a large number of free electrons are available. But, the width of the middle layer is very small and it is lightly doped. So significantly less free electrons are present in the Base region.

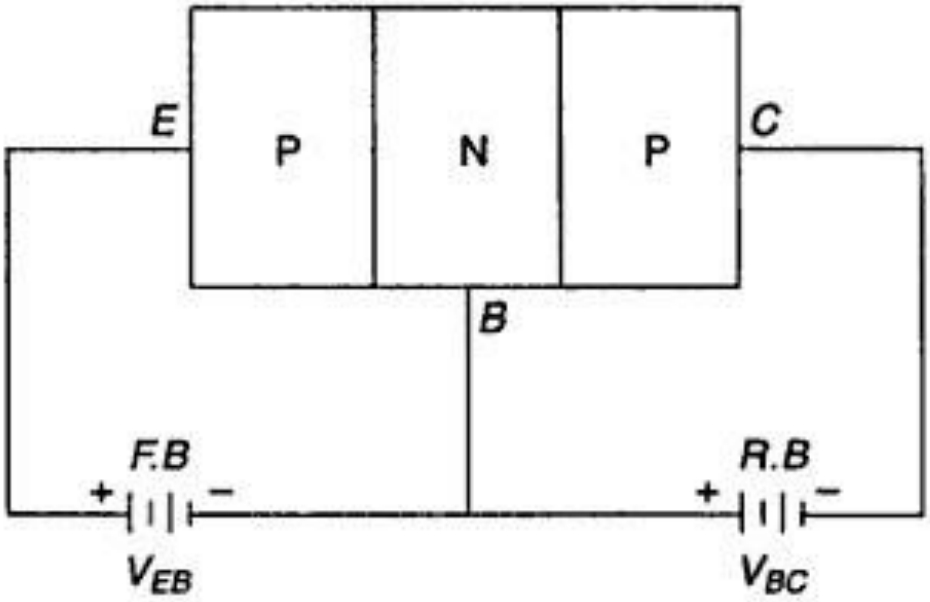

Fig:2.2.2 Construction of PNP Transistor

Working of PNP Transistor

The positive terminal of a voltage source (VEB) is connected with Emitter (P-type) and the negative terminal is connected with the Base terminal (N-type). Therefore, the Emitter-Base junction is connected in forward bias. And the positive terminal of a voltage source (VCB) is connected with the Base terminal (N-type) and the negative terminal is connected with the Collector terminal (P-type). Hence, the Collector-Base junction is connected in reverse bias.

Due to this type of bias, the depletion region at Emitter-Base junction is narrow, because it is connected in forward bias. While the Collector-Base junction is in reverse bias and hence the depletion region at Collector-Base junction is wide.

The Emitter-base junction is in forward bias. Therefore, a very large number of holes from emitter cross the depletion region and enter the Base. Simultaneously, very few electrons enter in Emitter from the base and recombine with the holes.

The loss of holes in the emitter is equal to the number of electrons present in the Base layer. But The number of electrons in the Base is very small because it is a very lightly doped and thin region. Therefore, almost all holes of Emitter will cross the depletion region and enter into the Base layer.

Because of the movement of holes, the current will flow through the Emitter-Base junction. This current is known as Emitter current (IE). The holes are majority charge carriers to flow the Emitter current.

The remaining holes which do not recombine with electrons in Base, that holes will further travel to the Collector. The Collector current (IC) flows through the Collector-Base region due to holes.

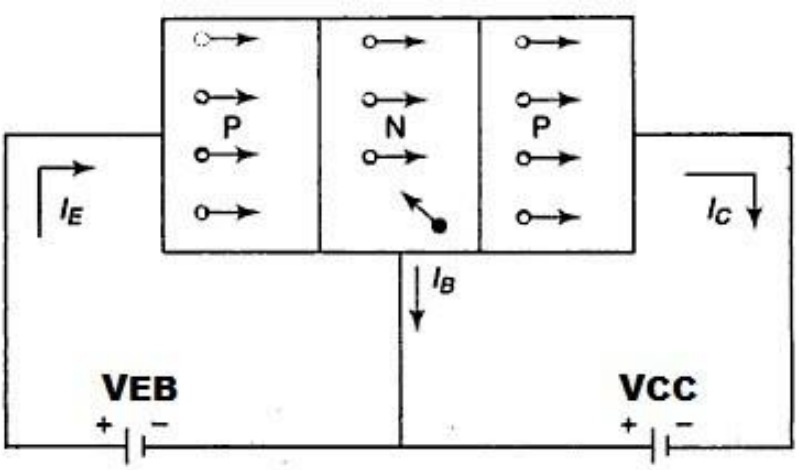

Fig:2.2.3 Working Principle of PNP Transistor

The working of the PNP transistor, if the Base voltage is not more negative then Emitter voltage, the current cannot flow through the device. So, Base voltage is a minimum of 0.7 V in reverse bias to conduct the transistor.

It means that, if the Base voltage is zero or less than 0.7 V, the current cannot flow and it acts as an open circuit.