Reg. No. : | | | | | | | | | | | | |

Question Paper Code : 40965

B.E./B.Tech. DEGREE EXAMINATION, APRIL/MAY 2018
Sixth/Seventh/Eighth Semester
Electronics and Communication Engineering
EC 6601 – VLSI DESIGN
(Common to Biomedical Engineering/Electrical and Electronics Engineering/ Electronics and Instrumentation Engineering/Medical Electronics/Robotics and Automation Engineering)
(Regulations 2013)

Time : Three Hours | Maximum : 100 Marks

Answer ALL questions

PART – A (10×2=20 Marks)

1. What is velocity saturation effect ?
2. List the scaling principles.
3. Define Elmore's constant.
4. List the types of power dissipation.
5. Define clock skew.
6. Compare Registers and Latches.
7. Write the full adder output interms of propagate and generate.
8. Draw the structure of 4 × 4 barrel shifter.
9. What is the role of cell libraries in ASIC design ?
10. What are the two different types of routing ?

PART – B (5×13=65 Marks)

11. a) Explain the dynamic behavior of MOSFET transistor with neat diagram. (6+7)

(OR)

b) Write the layout design rules and draw diagram for four input NAND and NOR gate. (6+7)

12. a) i) Draw the CMOS logic circuit for the Boolean expression $Z = [A(B + C) + DE]'$ and explain. **(6)**

ii) Explain the basic principle of transmission gate in CMOS design. **(7)**

(OR)

b) Briefly discuss the signal integrity issues in dynamic design. **(13)**

13. a) Discuss about CMOS register concept and design master slave triggered register, explain its operation with overlapping periods. **(13)**

(OR)

b) Explain the memory architecture and its control circuits in detail. **(6+7)**

14. a) Explain the concept of carry look ahead adder and discuss its types. **(6+7)**

(OR)

b) Design a multiplier for 5 bit by 3 bit. Explain its operation and summarize the number of adders. Discuss it over Wallace multiplier. **(5+4+4)**

15. a) Explain the various types of ASIC with neat diagram. **(6+7)**

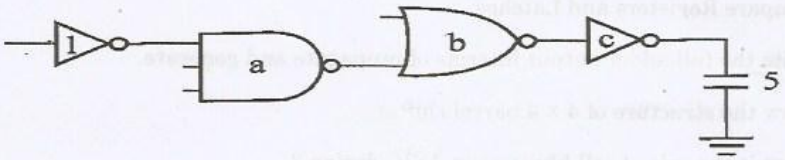
(OR)

b) Draw and explain the building blocks of FPGA. **(6+7)**

PART – C **(1×15=15 Marks)**

16. a) i) Design a CMOS logic circuit for the given expression $X = [(A + B).(C + D)]'$ and draw its stick diagram. **(7)**

ii) Obtain the logical effort and path efforts of the given circuit. **(8)**



(OR)

b) i) Design a clock distribution network based on H tree model for 16 nodes. **(7)**

ii) Design a four input NAND gate and obtain its delay during the transition from high to low. **(8)**