Reg. No. : | | | | | | | | | | | | |

Question Paper Code : 40902

B.E./B.Tech. DEGREE EXAMINATION, APRIL/MAY 2018
Third/Fifth/Sixth Semester
Computer Science and Engineering
CS 6303 – COMPUTER ARCHITECTURE
(Common to : Electronics and Communication Engineering/Electronics and Instrumentation Engineering/Instrumentation and Control Engineering/Robotics and Automation Engineering/Information Technology)
(Regulations 2013)

Time : Three Hours | Maximum : 100 Marks

Answer ALL questions

PART – A **(10×2=20 Marks)**

1. Write the equation for the dynamic power required per transistor.
2. Classify the instructions based on the operations they perform and give one example to each category.
3. Show the IEEE 754 binary representation of the number $(-0.75)_{10}$ in single precision.
4. Define a datapath in a CPU.
5. What is the ideal CPI of a pipelined processor ?
6. What is meant by exception ? Give one example of MIPS exception.
7. Protein String Matching Code has 4 days execution time on current machine doing integer instructions in 20% of time, doing I/O in 35% of time and other operations in the remaining time. Which is the better tradeoff among the following two proposals ? First : Compiler optimization that reduces number of integer instructions by 25% (assume each integer instruction takes the same amount of time); Second : Hardware optimization that reduces the latency of each IO operations from 6μs to 5μs.
8. Give example for each class in Flynn's classification.
9. Distinguish SRAM and DRAM.
10. What is the use of DMA Controller ?

PART – B (5×13=65 Marks)

11. a) i) Consider three different processors P1, P2 and P3 executing the same instruction set. P1 has a 3 GHz clock rate and a CPI of 1.5. P2 has a 2.5 GHz clock rate and a CPI of 1.0. P3 has a 4.0 GHz clock rate and has a CPI of 2.2.

a) Which processor has the highest performance expressed in instructions per second ?

b) If the processors each execute a program in 10 seconds, find the number of cycles and the number of instructions in each processor. (5)

ii) Explain in detail the components of a computer system. (8)

(OR)

b) i) Translate the following C code to MIPS assembly code. Use a minimum number of instructions. Assume that i and k correspond to registers $s3 and $s5 and the base of the array save is in $s6. What is the MIPS assembly code corresponding to this C segment ?

```
while (save[i] = = k)
i + = 1;
```

(5)

ii) What is an addressing mode in a computer ? Classify MIPS addressing modes and give one example instruction to each category. (8)

12. a) i) Perform X + Y and Y – X using 2's complements for given the two binary numbers X = 0000 1011 1110 1111 and Y = 1111 0010 1001 1101. (5)

ii) Multiply the following signed 2's compliment numbers using the Booth algorithm. A = 001110 and B = 111001 where A is multiplicand and B is multiplier. (8)

(OR)

b) i) Draw the block diagram of integer divider and explain the division algorithm. (5)

ii) Add the numbers $(0.75)_{10}$ and $(-0.275)_{10}$ in binary using the Floating point addition algorithm. (8)

13. a) Design a simple datapath with the control unit and explain in detail. (13)

(OR)

b) Discuss the limitations of pipelining a processor's datapath. Suggest the methods to overcome them. (13)

14. a) i) List the limitations of instruction level parallelism. (5)

ii) What are the challenges in parallel processing ? (8)

(OR)

b) i) Compare and contrast fine-grained multi-threading, coarse-grained multi-threading and simultaneous multi-threading. (9)

ii) Classify shared memory multiprocessor based on the memory access latency. (4)

15. a) i) What is the need for Cache memory ? List the three mapping methods of Cache memory and explain any two. (10)

ii) Define virtual memory. What is the advantage of using virtual memory ? (3)

(OR)

b) i) Discuss about Programmed I/Os associated with computers. (6)

ii) Write the sequence of operations carried out by a processor when interrupted by a peripheral device connected to it. (7)

PART – C (1×15=15 Marks)

16. a) The following sequence of instructions are executed in the basic 5-stage pipelined processor :

or r1, r2, r3
or r2, r1, r4
or r1, r1, r2

a) Indicate dependences and their type.

b) Assume there is no forwarding in this pipelined processor. Indicate hazards and add NOP instructions to eliminate them.

c) Assume there is full forwarding. Indicate hazards and add NOP instructions to eliminate them. (15)

(OR)

b) Explain the detail of DMA control with suitable diagrams. Discuss how it improve the overall performance of the system. (15)

———————