10. Show the IEEE 754 binary representation of the number -0.75 10in single and double precision

UNIT III
Processor and Control Unit

PART-A

1. What are the three kinds of core instruction in MIPS.

MIPS have three kinds of core instruction:

4. The arithmetic-logical instructions add, sub, and, or, and slt
5. The memory-reference instructions load word (lw) and store word (sw)
6. The branch instructions- branch equal (beq) and jump (j), which we add last

2. What is the use of PC register?

Program Counter (PC) is the register containing the address of the instruction in the program being executed.

3. What is meant by register file?

The processor's 32 general -purpose registers are stored in a structure called a register file. A register file is a collection of registers in which any register can be read or written by specifying the number of the register in the file. The register file contains the register state of the computer

4. What is pipelining and precise exception?

Pipelining: The technique of overlapping the execution of successive instruction for substantial improvement in performance is called pipelining.

Precise exception:A precise exception is one in which all instructions prior to the faulting instruction are complete and instruction following the faulting instruction, including the faulty instruction; do not change the state of the machine.

5. Define processor cycle in pipelining.

The time required between moving an instruction one step down the pipeline is a processor cycle.

6. What is meant by pipeline bubble?

To resolve the hazard the pipeline is stall for 1 clock cycle. A stall is commonly called a pipeline bubble, since it floats through the pipeline taking space but carrying no useful work.

7. What is meant by data path element?

A data path element is a unit used to operate on or hold data within a processor. In the MIPS implementation, the data path elements include the instruction and data memories, the register file, the ALU, and adders.

8. What is pipeline register delay?

Adding registers between pipeline stages me adding logic between stages and setup and hold times for proper operations. This delay is known as pipeline register delay.

9. What are the major characteristics of a pipeline?

The major characteristics of a pipeline are:

1. Pipelining cannot be implemented on a single task, as it works by splitting multiple tasks into a number of subtasks and operating on them simultaneously.
2. The speedup or efficiency achieved by suing a pipeline depends on the number of pipe stages and the number of available tasks that can be subdivided.

10. What is data path?

As instruction execution progress data are transferred from one instruction to another, often passing through the ALU to perform some arithmetic or logical operations. The registers, ALU, and the interconnecting bus are collectively referred as the data path.

11. What is a pipeline hazard and what are its types?

Any condition that causes the pipeline to stall is called hazard. They are also called as stalls or bubbles. The various pipeline hazards are:

1. Data hazard
2. Structural Hazard
3. Control Hazard.

12. What is meant by data hazard in pipelining?

Any condition in which either the source or the destination operands of an instruction are not available at the time expected in the pipeline is called data hazard.

13. What are the five steps in MIPS instruction execution?

1. Fetch instruction from memory.
2. Read registers while decoding the instruction. The regular format of MIPS instructions allows reading and decoding to occur simultaneously.
3. Execute the operation or calculate an address.
4. Access an operand in data memory.
5. Write the result into a register.

14. What is Instruction or control hazard?

The pipeline may be stalled because of a delay in the availability of an instruction. For example, this may be a result of a miss in the cache, requiring the instruction to be fetched from the main memory. Such hazards are often called control hazards or instruction hazard.

15. Define structural hazards.

This is the situation when two instruction require the use of a given hardware resource at the same time. The most common case in which this hazard may arise is in access to memory.

16. What is side effect?

When a location other than one explicitly named in an instruction as a destination operand is affected, the instruction is said to have a side effect.

17. What do you mean by branch penalty?

The time lost as a result of a branch instruction is often referred to as branch penalty.

18. What is branch folding?

When the instruction fetch unit executes the branch instruction concurrently with the execution of the other instruction, then this technique is called branch folding.

19. What do you mean by delayed branching?

Delayed branching is used to minimize the penalty incurred as a result of conditional branch instruction. The location following the branch instruction is called delay slot. The instructions in the delay slots are always fetched and they are arranged such that they are fully executed whether or not branch is taken. That is branching takes place one instruction later than where the branch instruction appears in the instruction sequence in the memory hence the name delayed branching.

20. Define Sign Extend

Sign-extend is used to increase the size of a data item by replicating the high-order sign bit of the original data item in the high order bits of the larger, destination data item.

21. What is meant by branch target address?

Branch target address is the address specified in a branch, which becomes the new program counter (PC) if the branch is taken. In the MIPS architecture the branch target is given by the sum of the off set field of the instruction and the address of the instruction following the branch.

22. Differentiate branch taken from branch not taken.

Branch taken is a branch where the branch condition is satisfied and the program counter (PC) becomes the branch target. All unconditional jumps are taken branches. Branch not taken or (untaken branch) is a branch where the branch condition is false and the program counter (PC) becomes the address of the instruction that sequentially follows the branch.

23. Define exception and interrupt.

Exception: The term exception is used to refer to any event that causes an interruption.

Interrupt: An exception that comes from outside of the processor. There are two types of interrupt.

1. Imprecise interrupt
2. Precise interrupt

24. Why is branch prediction algorithm needed? Differentiate between the static and dynamic techniques.

The branch instruction will introduce branch penalty which would reduce the gain in performance expected from pipelining. Branch instructions can be handled in several ways to reduce their negative impact on the rate of execution of instructions. Thus the branch prediction algorithm is needed.

Static Branch prediction

The static branch prediction, assumes that the branch will not take place and to continue to fetch instructions in sequential address order.

Dynamic Branch prediction

The idea is that the processor hardware assesses the likelihood of a given branch being taken by keeping track of branch decisions every time that instruction is executed. The execution history used in predicting the outcome of a given branch instruction is the result of the most recent execution of that instruction.

25. What is branch Target Address?

The address specified in a branch, which becomes the new program counter, if the branch is taken. In MIPS the branch target address is given by the sum of the offset field of the instruction and the address of the instruction following the branch.

26. Define Pipeline speedup.

The ideal speedup from a pipeline is equal to the number of stages in the pipeline.

$$\frac{\text{Time per instruction on unpipelined machine}}{\text{Number of pipe stages}}$$