UNIT I

BIASING OF DISCRETE BJT AND MOSFET

1.1. Introduction:

Transistor is a three terminal device: Base, emitter and collector, can be operated in three configurations common base, common emitter and common collector. It is used in amplifier and oscillator circuits, and as a switch in digital circuits. It has wide applications in computers, satellites and other modern communication systems.

There are two types of transistors:

1. Unipolar junction transistor(UJT): The current conduction is only due to one type of charge carriers, majority carriers.

2. Bipolar junction transistor(BJT): The current conduction is due to both the types of charge carriers, holes and electrons.

There are two types of BJT:

1. PNP transistor: A thin layer of N-type silicon material is sandwiched between two layers of P-type silicon.

2. NPN transistor: A layer of P-type material is sandwiched between two layers of N-type material.

(a) **NPN transistor** **(b) PNP transistor**

Fig 1.1. Standard transistor symbols

1.2. Need for biasing:

The transistor can be operated in three regions: cut-off, active and saturation. In order to operate transistor in the desired region we have to apply external d.c. voltages of correct polarity and magnitude to the two junction of the transistor. This is called as d.c. biasing of the transistor.

1.3. Operating point:

When we bias a transistor we establish a certain current & voltage condition for the transistor. These conditions are known as d.c. operating point or quiescent point. The operating point must be stable for proper operation of the transistor. The operating point shifts with changes in transistor parameters such as β, I_{co} & V_{BE}.

1.4. Stability factor:

Stability factor indicates degree of change in operating point due to variation in temperature. Three stability factors are,

i) $$S = \frac{\partial I_c}{\partial I_{co}}\Big| V_{BE}, \beta \text{ constant}$$

ii) $$S' = \frac{\partial I_C}{\partial V_{BE}}\Big| I_{CO}, \beta \text{ constant}$$

iii) $$S'' = \frac{\partial I_c}{\partial \beta}\Big| I_{CO}, V_{BE} \text{ constant}$$

1.5. Various biasing methods for BJT:

1. Fixed bias circuit
2. Collector to base bias circuit
3. Voltage divider (or) self bias circuit

1.5.1. Fixed bias circuit:

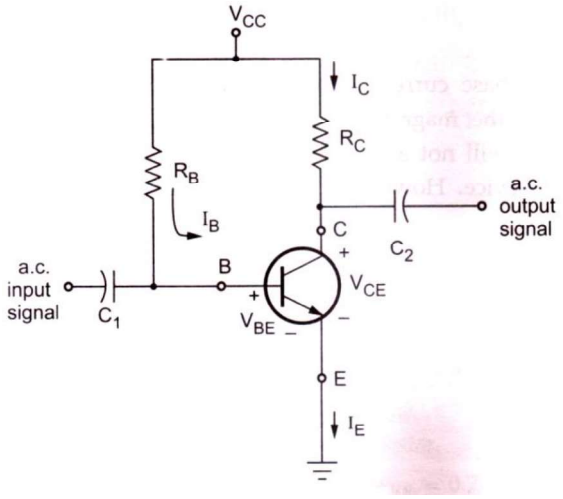


Fig 1.2. Fixed bias circuit

DC analysis:

For the d.c. analysis we can replace capacitor with an open circuit because the reactance of a capacitor for d.c. is $X_c = \frac{1}{2\pi fC} = \frac{1}{2\pi(0)C} = \infty$.

i) Base current:

Applying KVL to the base circuit we get,

$$V_{CC} - I_B R_B - V_{BE} = 0$$

$$I_B R_B = V_{CC} - I_B R_B$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

ii) Collector current:

Applying KVL to the collector circuit,

$$V_{CC} - I_C R_C - V_{CE} = 0$$

$$I_C R_C = V_{CC} - V_{CE}$$

$$I_C = \frac{V_{CC} - V_{CE}}{R_C}$$

$$V_{CE} = V_{CC} - I_C R_C$$

The magnitude of the collector current is given by,

$$I_C = \beta I_B$$

Input voltage: $V_{BE} = V_B$

Output voltage: $V_{CE} = V_C$

Advantages:

1. This is a simple circuit which uses very few components.
2. The operating point can be fixed anywhere in the active region of the characteristics by simply changing the value of R_B. Thus, it provides maximum flexibility in the design.

Disadvantages:

1. The collector current increases with the rise in temperature. So the operating point is not maintained.

$$I_C = \beta I_B + I_{CEO}$$

2. Since $I_C = \beta I_B$ and I_B is already fixed. I_C depends on β which changes unit to unit and shifts the operating point.

1.5.2. Collector to base bias circuit:

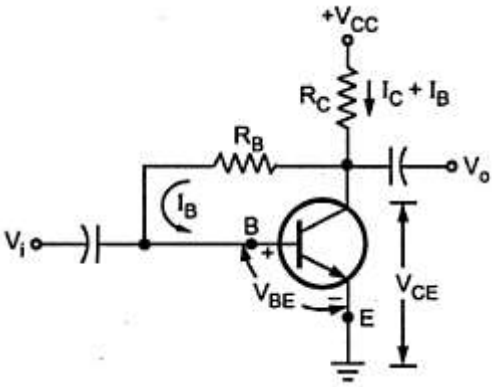


Fig 1.3. Collector to base bias circuit

DC analysis:

i) Base current:

Applying KVL to the circuit,

$$V_{CC} - (I_C + I_B)R_C - I_B R_B - V_{BE} = 0$$

$$V_{CC} - I_C R_C - I_B R_C - I_B R_B - V_{BE} = 0$$

$$V_{CC} - \beta I_B R_C - I_B R_C - I_B R_B - V_{BE} = 0$$

$$V_{CC} - I_B R_C(1 + \beta) - I_B R_B - V_{BE} = 0$$

$$I_B R_C(1 + \beta) + I_B R_B = V_{CC} - V_{BE}$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_C(1 + \beta) + R_B}$$

If $\beta \gg 1$, $\quad I_B = \dfrac{V_{CC} - V_{BE}}{\beta R_C + R_B}$

ii) Collector Voltage:

Applying KVL to the collector circuit,

$$V_{CC} - (I_C + I_B)R_C - V_{CE} = 0$$

$$V_{CE} = V_{CC} - (I_C + I_B)R_C$$

1.5. 3. Voltage divider bias circuit:

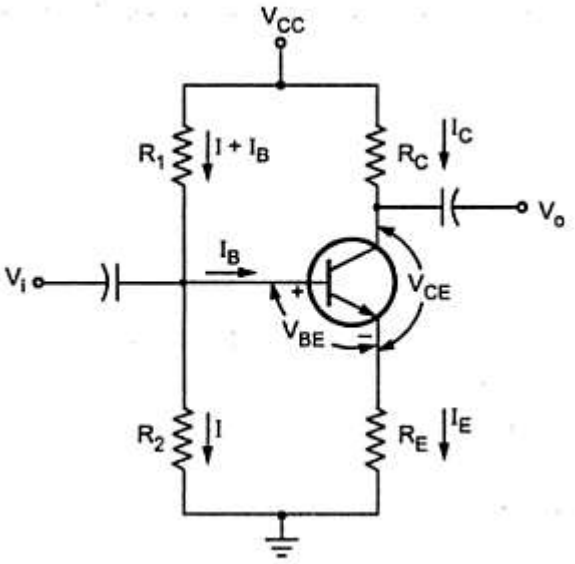


Fig 1.4. Voltage divider bias circuit

In this circuit, the biasing is provided by three resistors: R_1, R_2 & R_E. The resistors R_1 & R_2 act as a potential divider giving a fixed voltage to point B. If collector current increases due to the change in temperature, the emitter current also increases & voltage drop across R_E increases, reducing the voltage difference between base and emitter (V_{BE}). Due to reduction in V_{BE}, I_B & I_C also reduces. This reduction in collector current I_C compensate for the original change in I_C.

DC analysis:

i) Base circuit:

Applying voltage divider theorem,

$$V_B = \frac{R_2 I}{R_1(I + I_B) + R_2(I)} \times V_{CC}$$

$$\text{If } I >> I_B, \quad V_B = \frac{R_2}{R_1 + R_2} \times V_{CC}$$

ii) Collector circuit:

Applying KVL to the collector circuit,

$$V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$$

$$V_{CE} = V_{CC} - I_C R_C - I_E R_E$$

By Ohm's law,

$$V_E = I_E R_E = V_B - V_{BE}$$

$$I_E = \frac{V_B - V_{BE}}{R_E}$$

Simplified circuit of voltage divider bias,

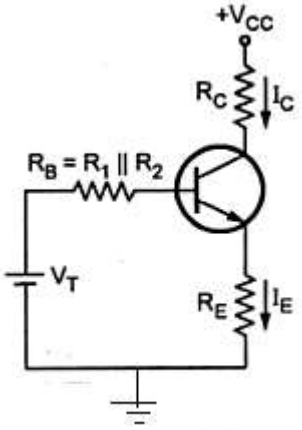


Fig 1.5. Thevenin's equivalent circuit for voltage divider bias

Where, V_T -Thevenin's voltage,

$$R_B = R_1 \parallel R_2$$

$$R_B = \frac{R_1 + R_2}{R_1 + R_2}$$

Applying KVL to the base circuit,

$$V_T - I_B R_B - V_{BE} - I_E R_E = 0$$

$$V_T = I_B R_B + V_{BE} + I_E R_E$$

$$V_T = I_B R_B + V_{BE} + I_B R_E + I_C R_E \qquad \because I_E = I_B + I_C$$

$$V_T = V_{BE} + I_B(R_B + R_E) + I_C R_E$$

$$V_{BE} = V_T - I_B(R_B + R_E) - I_C R_E$$

$$V_{BE} = V_T - I_B(R_B + R_E) - \beta I_B R_E \qquad \because I_C = \beta I_B$$

$$V_{BE} = V_T - I_B[R_B + (1+\beta)R_E]$$

$$I_B = \frac{V_T - V_{BE}}{R_B + (1+\beta)R_E}$$

1.6. Stability factors:

1.6.1. Fixed Bias:

Step 1: To calculate stability factor S

$$S = \frac{\partial I_c}{\partial I_{co}} = \frac{1+\beta}{1-\beta\left(\frac{\partial I_B}{\partial I_C}\right)}$$

We know that,

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

$$I_B \approx \frac{V_{CC}}{R_B} \qquad \because V_{BE} = 0.7$$

$$\frac{\partial I_B}{\partial I_C} = 0$$

$$\Rightarrow \quad S = 1 + \beta$$

Step 2: To calculate stability factor S'

$$S' = \frac{\partial I_C}{\partial V_{BE}}$$

W. K. T, $I_C = \beta I_B + I_{CEO}$

$$I_C = \beta I_B + (1+\beta) I_{CBO} \qquad \because I_E = I_B + I_C$$

$$I_E = I_B + \beta I_B$$

Sub $I_B = \frac{V_{CC} - V_{BE}}{R_B}$

$$I_C = \beta\frac{(V_{CC} - V_{BE})}{R_B} + (1+\beta) I_{CBO}$$

$$S' = \frac{\partial I_C}{\partial V_{BE}} = -\frac{\beta}{R_B}$$

Step 3: To calculate stability factor S"

$$S'' = \frac{\partial I_c}{\partial \beta}$$

$$I_C = \beta\frac{(V_{CC} - V_{BE})}{R_B} + (1+\beta)I_{CBO}$$

$$\frac{\partial I_c}{\partial \beta} = \frac{(V_{CC} - V_{BE})}{R_B} + I_{CBO}$$

$$\frac{\partial I_c}{\partial \beta} = I_B + I_{CBO}$$

$$S'' = I_B \approx \frac{I_C}{\beta}$$

1.6.2. Collector to Base Bias:

Step 1: To calculate stability factor S

$$V_{CC} - I_C R_C - I_B R_C - I_B R_B - V_{BE} = 0$$

$$V_{CC} = I_C R_C + I_B(R_B + R_C) + V_{BE}$$

$$I_B(R_B + R_C) = V_{CC} - I_C R_C - V_{BE}$$

$$\frac{\partial I_B}{\partial I_C} = -\frac{R_C}{R_B + R_C}$$

$$S = \frac{1+\beta}{1 - \beta\left(-\frac{R_C}{R_B + R_C}\right)}$$

$$S = \frac{1+\beta}{1 + \beta\left(\frac{R_C}{R_B + R_C}\right)}$$

Step 2: To calculate stability factor S'

$$S' = \frac{\partial I_C}{\partial V_{BE}}$$

$$I_B = \frac{V_{CC} - I_C R_C - V_{BE}}{R_B + R_C}$$

$$\frac{I_C}{\beta} = \frac{V_{CC} - I_C R_C - V_{BE}}{R_B + R_C} \qquad \because I_C = \beta I_B$$

$$\frac{I_C}{\beta} + \frac{I_C R_C}{R_B + R_C} = \frac{V_{CC} - V_{BE}}{R_B + R_C}$$

$$I_C \left[\frac{R_B + R_C + \beta R_C}{\beta(R_B + R_C)}\right] = \frac{V_{CC} - V_{BE}}{R_B + R_C}$$

$$I_C = \frac{\beta(V_{CC} - V_{BE})}{R_B + R_C(1 + \beta)}$$

$$S' = \frac{\partial I_C}{\partial V_{BE}} = -\frac{\beta}{R_B + R_C(1 + \beta)}$$

Step 3: To calculate stability factor S"

$$S'' = \frac{\partial I_c}{\partial \beta}$$

$$I_C = \frac{\beta(V_{CC} - V_{BE})}{R_B + R_C(1 + \beta)}$$

$$\frac{\partial I_C}{\partial \beta} = \frac{[R_B + R_C(1 + \beta)][V_{CC} - V_{BE}] - \beta[V_{CC} - V_{BE}]R_C}{[R_B + R_C(1 + \beta)]^2}$$

$$\because \frac{d}{dt}\left(\frac{u}{v}\right) = \frac{v\frac{du}{dt} - u\frac{dv}{dt}}{v^2}$$

$$S'' = \frac{\partial I_C}{\partial \beta} = \frac{[R_B + R_C][V_{CC} - V_{BE}]}{[R_B + R_C(1 + \beta)]^2}$$

$$S'' = \frac{\partial I_C}{\partial \beta} = \frac{I_C}{\beta}\frac{[R_B + R_C][V_{CC} - V_{BE}]}{[R_B + R_C(1 + \beta)\,]}$$

$$S'' = \frac{I_C S}{(1 + \beta)\beta}$$

1.6.3. Voltage divider bias:

Step 1: To calculate stability factor S

$$V_T = I_B R_B + V_{BE} + I_E R_E$$

$$V_T - I_B R_B - V_{BE} - I_B R_E - I_C R_E = 0$$

$$V_T - I_B(R_B + R_E) - V_{BE} - I_C R_E = 0$$

$$I_B(R_B + R_E) = V_T - V_{BE} - I_C R_E$$

$$\frac{\partial I_B}{\partial I_C}(R_B + R_E) = -R_E$$

$$\frac{\partial I_B}{\partial I_C} = \frac{-R_E}{(R_B + R_E)}$$

$$S = \frac{1+\beta}{1+\beta\left(\frac{R_E}{R_B + R_E}\right)}$$

Step 2: To calculate stability factor S'

$$S' = \frac{\partial I_C}{\partial V_{BE}}$$

$$\text{W.K.T,} \qquad I_C = \beta I_B + (1+\beta) I_{CBO}$$

$$I_B = \frac{I_C - (1+\beta) I_{CBO}}{\beta}$$

$$V_T - \left(\frac{I_C - (1+\beta) I_{CBO}}{\beta}\right)(R_B + R_E) - V_{BE} - I_C R_E = 0$$

$$V_T - \frac{I_C}{\beta}(R_B + R_E) + \frac{(R_B + R_E)(1+\beta) I_{CBO}}{\beta} - V_{BE} - I_C R_E = 0$$

$$V_T - I_C\left[\frac{R_B + (1+\beta) R_E}{\beta}\right] + \frac{(R_B + R_E)(1+\beta) I_{CBO}}{\beta} - V_{BE} = 0$$

$$I_C\left[\frac{R_B + (1+\beta) R_E}{\beta}\right] = V_T - V_{BE} + \frac{(R_B + R_E)(1+\beta) I_{CBO}}{\beta}$$

$$\frac{\partial I_c}{\partial V_{BE}}\left[\frac{R_B + (1+\beta)R_E}{\beta}\right] = -1$$

$$S' = \frac{-\beta}{R_B + (1+\beta)R_E}$$

Step 3: To calculate stability factor S"

$$S'' = \frac{\partial I_c}{\partial \beta}$$

$$I_C\left[\frac{R_B + (1+\beta)R_E}{\beta}\right] = V_T - V_{BE} + \frac{(R_B + R_E)(1+\beta)I_{CBO}}{\beta}$$

$$\text{Let us consider } V' = \frac{(R_B + R_E)(1+\beta)I_{CBO}}{\beta}$$

$$I_C = \frac{\beta(V_T - V_{BE} + V')}{R_B + (1+\beta)R_E}$$

$$\frac{\partial I_c}{\partial \beta} = \frac{[R_B + (1+\beta)R_E][V_T - V_{BE} + V'] - \beta[V_T - V_{BE} + V']R_E}{[R_B + (1+\beta)R_E]^2}$$

$$\frac{\partial I_c}{\partial \beta} = \frac{(R_B + R_E)(V_T - V_{BE} + V')}{[R_B + (1+\beta)R_E]^2}$$

$$\frac{\partial I_c}{\partial \beta} = \frac{I_C}{\beta}\frac{(R_B + R_E)}{[R_B + (1+\beta)R_E]}$$

$$S'' = \frac{I_C S}{(1+\beta)\beta}$$

1.7. DC load line:

For fixed bias circuit,

$$I_C = \frac{V_{CC} - V_{CE}}{R_C}$$

$$I_C = \frac{V_{CC}}{R_C} - \frac{V_{CE}}{R_C}$$

$$I_C = \left(\frac{-1}{R_C}\right) V_{CE} + \frac{V_{CC}}{R_C}$$

We know that equation of the straight line is,

$$y = mx + c$$

where, m = slope of the line

c = intercept on y-axis

i)X axis: $I_C = 0$ $V_{CE} = V_{CC}$ (point A)

ii)Y axis: $V_{CE} = 0$ $I_C = \frac{V_{CC}}{R_{CC}}$ (point B)

The line drawn between points A and B is called d.c. load line.

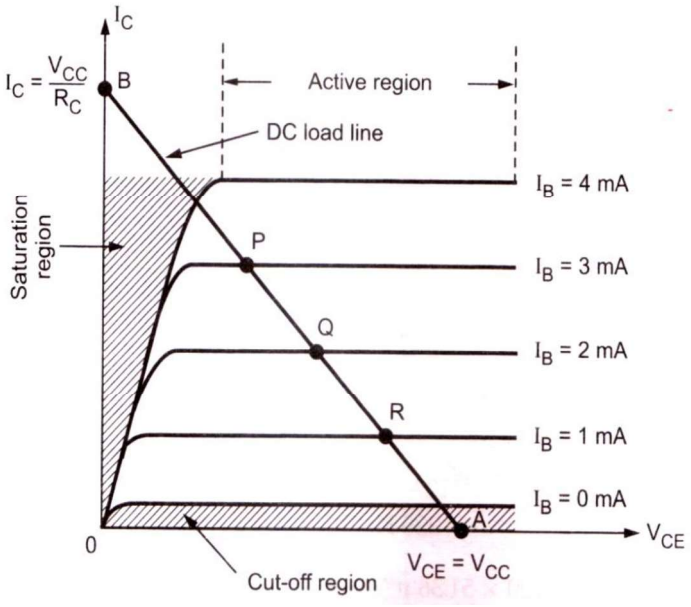


Fig 1.6. CE output characteristics with d.c. load line

1.8. Bias compensation:

The collector to base bias and voltage divider bias use negative feedback to do the stabilization action. This negative feedback reduces the amplification of the signal. If this loss in signal amplification is intolerable and extremely stable biasing conditions are required, then it is necessary to use compensation techniques. Compensation techniques use temperature sensitive devices such as diodes, thermistors ,transistors, etc. Compensation techniques are used to maintain operating point constant.

1.8.1. Diode compensation techniques:

i) Compensation for V_{BE}:

a) Diode in emitter circuit:

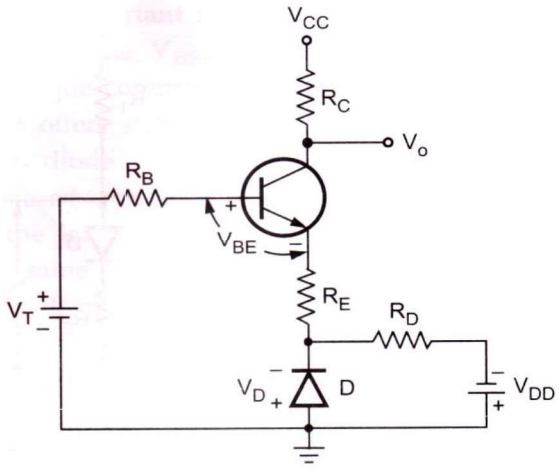


Fig 1.7. Diode compensation in emitter circuit

Separate supply V_{DD} is used to keep diode in forward biased condition. When V_{BE} changes by ∂V_{BE} with change in temperature, V_D changes by $\partial V_D \approx \partial V_{BE}$, the changes tend to cancel to each other.

Applying KVL to the base circuit,

$$V_T - I_B R_B - V_{BE} - I_E R_E + V_D = 0$$

$$V_T = I_B R_B + V_{BE} + (I_B + I_C) R_E - V_D$$

$$V_T = I_B (R_B + R_E) + V_{BE} + I_C R_E - V_D$$

Considering the leakage current,

$$I_C = \beta I_B + (1 + \beta) I_{CBO}$$

$$\text{Sub } I_C = \beta I_B$$

$$\beta I_B = \beta I_B + (1 + \beta) I_{CBO}$$

$$I_B = \frac{I_C}{\beta} + \frac{(1 + \beta) I_{CBO}}{\beta}$$

$$V_T = \left[\frac{I_C}{\beta} + \frac{(1 + \beta) I_{CBO}}{\beta}\right](R_B + R_E) + V_{BE} + I_C R_E - V_D$$

$$V_T = \frac{I_C}{\beta}(R_B + R_E + \beta R_E) + V_{BE} + \frac{(1+\beta)I_{CBO}(R_B + R_E)}{\beta} - V_D$$

$$I_C = \frac{\beta[V_T - V_{BE} + V_D] - (1+\beta)I_{CBO}(R_B + R_E)}{R_B + (1+\beta)R_E}$$

b) Diode in voltage divider circuit:

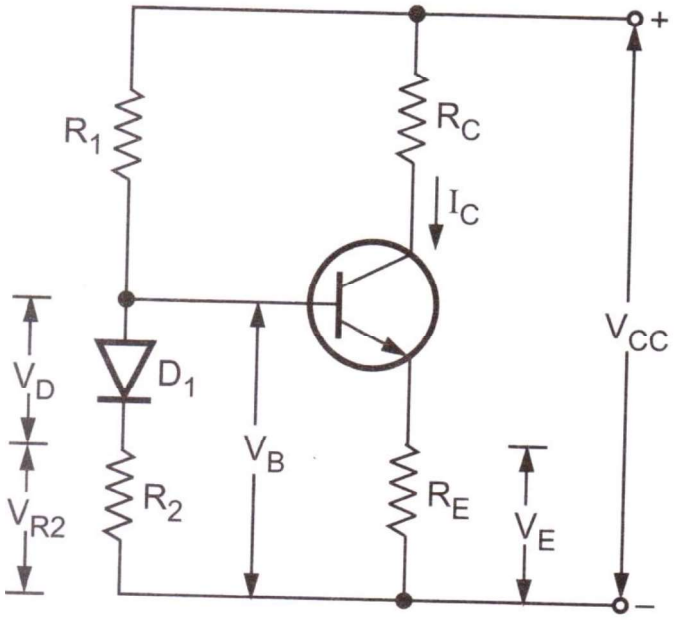


Fig 1.8. Diode compensation in voltage divider bias circuit

Diode is connected in series with resistance R_2 in the voltage divider circuit & it is forward biased condition.

W.K.T,

$$I_E = \frac{V_B - V_{BE}}{R_E}$$

$$I_C \approx \frac{V_B - V_{BE}}{R_E}$$

When V_{BE} changes with temperature, I_C also changes. To cancel the change in I_C, one diode is used in this circuit fo compensation.

$$V_B = V_{R2} + V_D$$

$$I_C \approx \frac{V_{R2} + V_D - V_{BE}}{R_E}$$

ii) Compensation for I_{CO}:

$$I = \frac{V_{CC} - V_{BE}}{R_1}$$

$$I = I_B + I_O \qquad \because I_B = I - I_O$$

$$I \approx \frac{V_{CC}}{R_1}$$

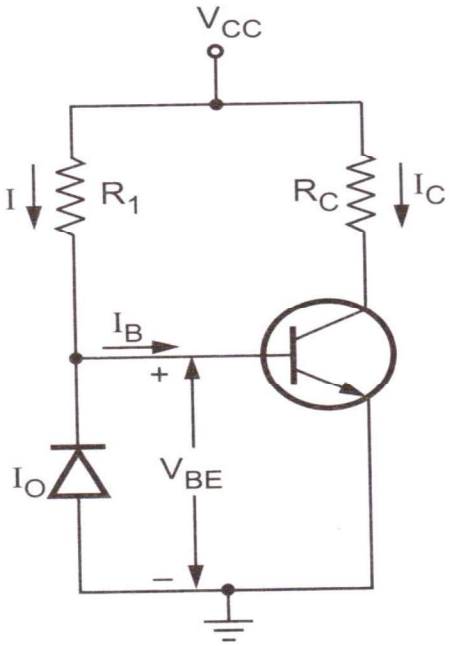


Fig 1.9. Diode compensation

W. K. T $\quad I_C = \beta I_B + (1 + \beta) I_{CBO}$

$$I_C = \beta I - \beta I_O + (1 + \beta) I_{CBO}$$

$$I_C = \beta I - \beta I_O + \beta I_{CBO} \qquad \because \beta \gg 1$$

Now if $I_O = I_{CBO}$ we get,

$$I_C = \beta I$$

As I is constant, I_C remains constant.

1.8.2. Thermistor compensation:

This method of transistor compensation uses temperature sensitive resistive elements, thermistors rather than diodes or transistors. It has a negative temperature coefficient, its resistance decreases exponentially with increasing temperature.

$$\text{Slope} = \frac{\partial R_T}{\partial T}$$

Temperature coefficient for thermistor & slope is negative. So we can say that thermistor has negative temperature coefficient of resistance(NTC).

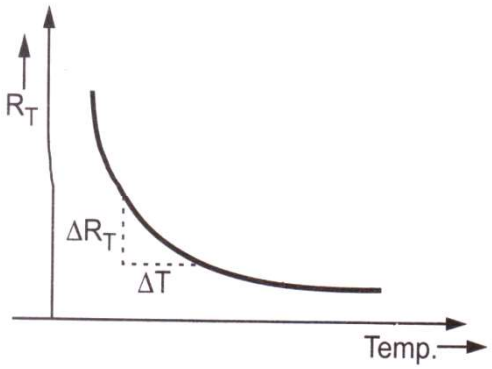


Fig 1.10. Temperature Vs R_T resistance of thermistor

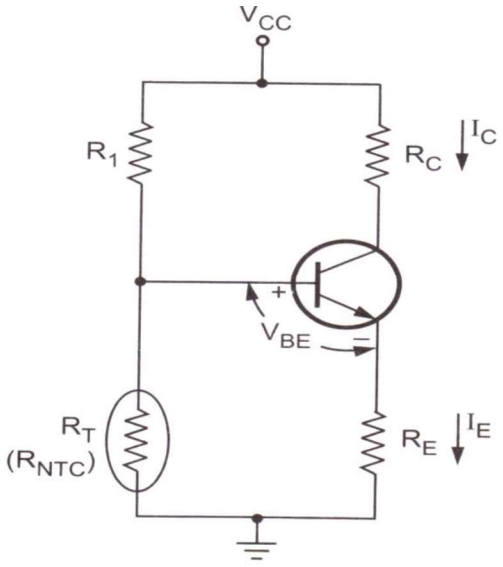


Fig 1.11. Thermistor compensation techniques

R_2 is replaced by thermistors R_T in self bias circuit. With increase in temperature, R_T decreases. Hence voltage drop across it also decreases. Hence, V_{BE} decreases which reduces I_B.

$$I_C = \beta I_B + (1 + \beta) I_{CBO}$$

Increase in I_{CO} & decreases in I_B keeps I_C almost constant.

1.8.3. Sensistor compensation:

It has positive temperature coefficient, its resistance increases exponentially with increasing temperature.

$$\text{Slope} = \frac{\partial R_T}{\partial T}$$

Temperature coefficient for sensistor & the slope is positive. So we can say that thermistor has positive temperature coefficient of resistance(PTC).

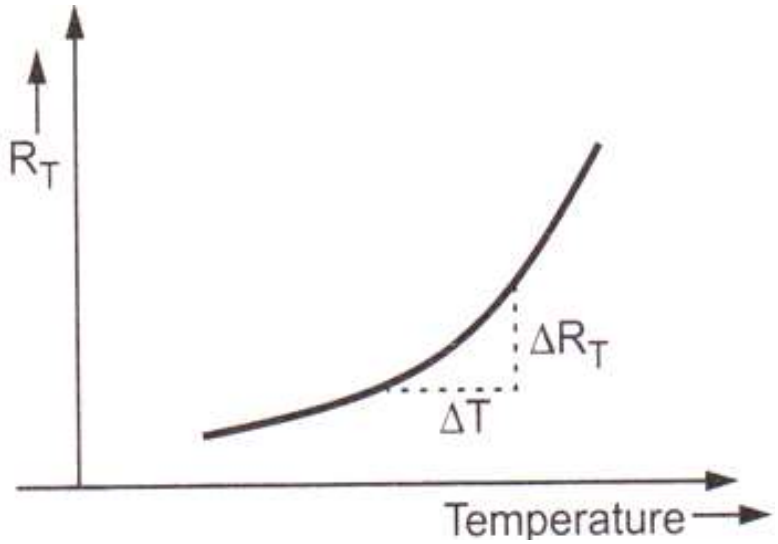


Fig 1.12. Temperature Vs R_T resistance of sensistor

R_1 is replaced by thermistors R_T in self bias circuit.As temperature increase, R_T increases which decreases the current flowing through it. Hence current through R_2 decreases which reduces the voltage drop across it. Hence, V_{BE} decreases which decreases I_B. It means, when I_{CBO} increase with increase in temperature, I_B reduces due to reduction in V_{BE}, maintaining I_C fairly constant.

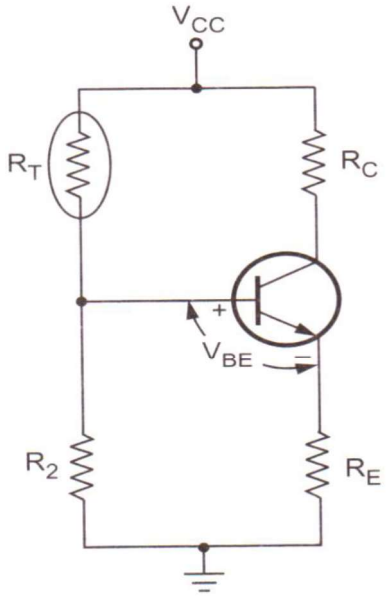


Fig 1.13. Sensistor compensation

1.9. Thermal stability:

The increase in the collector current increases the power dissipated at the collector junction. This in turn further increases the temperature of the junction & hence increase in the collector current. This process is referred to as self heating. The excess heat produced at the collector base junction may even burn & destroy the transistor. This situation is called thermal runaway of the transistor.

1.9.1. Thermal resistance:

The steady state temperature rise at the collector junction is proportional to the power dissipated at the junction.

$$\partial T = T_j - T_A = \theta P_D \quad \ldots\ldots\ldots\ldots\ldots\ldots (1)$$

Where, T_j=junction temperature in °C

T_A=Ambient temperature in °C

P_D= Power in watts dissipated at the collector junction

θ= Constant of proportionality thermal resistance

$$\theta = \frac{T_j - T_A}{P_D} °C/watt \quad \ldots\ldots\ldots\ldots\ldots\ldots (2)$$

1.9.2. The condition for thermal stability:

It is necessary to avoid thermal stability. The required condition to avoid thermal is that the rate at which heat is released at the collector junction must be exceed the rate at which the heat can be dissipated.

It is given by,

$$\frac{\partial P_C}{\partial T_j} < \frac{\partial P_D}{\partial T_j} \quad \ldots\ldots\ldots\ldots\ldots\ldots (3)$$

Differentiate (1) w.r.to T_j,

$$1 = \theta \frac{\partial P_D}{\partial T_j}$$

$$\frac{\partial P_D}{\partial T_j} = \frac{1}{\theta} \ldots\ldots\ldots\ldots\ldots\ldots (4)$$

Sub (4) in (3),

$$\frac{\partial P_D}{\partial T_j} < \frac{1}{\theta} \ldots\ldots\ldots\ldots\ldots\ldots (5)$$

This condition must be satisfied to prevent thermal runaway.

For voltage divider bias circuit we can say that,

P_C =Heat generated at the collector junction

= d.c. power input to the circuit- the power lost as I^2R in R_C & R_E

$$P_C = V_{CC} \times I_C - I_C^2 R_C - I_E^2 R_E \ldots\ldots\ldots\ldots\ldots (6)$$

$$\text{W. K. T.,} \qquad I_C \approx I_E$$

$$P_C = V_{CC} \times I_C - I_C^2 (R_C + R_E) \ldots\ldots\ldots\ldots\ldots\ldots (7)$$

Differentiate (7) w.r.to I_C,

$$\frac{\partial P_C}{\partial I_C} = V_{CC} - 2I_C (R_C + R_E) \ldots\ldots\ldots\ldots\ldots (8)$$

$$\text{Rewritting (5),} \qquad \frac{\partial P_C}{\partial I_C} \cdot \frac{\partial I_C}{\partial T_j} < \frac{1}{\theta} \ldots\ldots\ldots\ldots\ldots (9)$$

$$\frac{\partial I_C}{\partial T_j} = S \cdot \frac{\partial I_C}{\partial T_j} \ldots\ldots\ldots\ldots\ldots (10)$$

As the reverse saturation current increases about 7 percent per ℃

$$\frac{\partial I_C}{\partial T_j} = 0.07 I_{CO} . S \dots \dots \dots \dots \dots \dots (11)$$

Sub (8) & (11) in (9),

$$\{V_{CC} - 2I_C(R_C + R_E)\}. S(0.07 I_{CO}) < \frac{1}{\theta} \dots \dots \dots \dots \dots \dots (12)$$

As S,I_{CO} & θ are positive,

$$V_{CC} < 2I_C(R_C + R_E)$$

$$\frac{V_{CC}}{2} < I_C(R_C + R_E) \dots \dots \dots \dots \dots \dots (13)$$

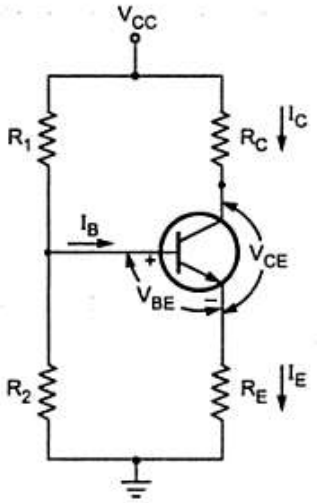


Fig 1.14. Voltage divider bias circuit

Applying KVL to the collector circuit,

$$V_{CC} - V_{CE} - I_C(R_E + R_C) = 0$$

$$I_C(R_E + R_C) = V_{CC} - V_{CE} \dots \dots \dots \dots \dots \dots (14)$$

Sub (14) in (13),

$$\frac{V_{CC}}{2} < V_{CC} - V_{CE}$$

$$V_{CE} < V_{CC} - \frac{V_{CC}}{2}$$

$$V_{CE} < \frac{V_{CC}}{2}$$

1.10. Biasing circuits for FET:

1. Fixed bias circuit
2. Voltage divider bias circuit
3. Self bias circuit

1.10.1. Fixed bias circuit

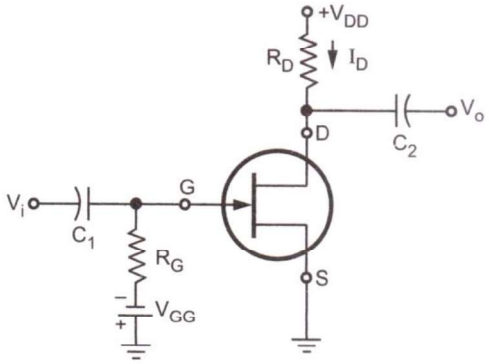


Fig 1.15. Fixed bias circuit

To make gate-source junction reverse biased, a separate supply V_{GG} is connected such that gate is more negative than the source.

DC analysis:

Step 1: To calculate V_{GS}

Applying KVL to the input circuit,

$$-V_{GG} - V_{GS} = 0$$

$$V_{GS} = -V_{GG}$$

Step 2: To calculate I_{DQ}

$$I_{DQ} = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

Step 3: To calculate V_{DS}

Applying KVL to the output side,

$$V_{DD} - I_D R_D - V_{DS} = 0$$

$$V_{DS} = V_{DD} - I_D$$

Drawback: It requires two power supplies.

1.10.2. Voltage divider bias:

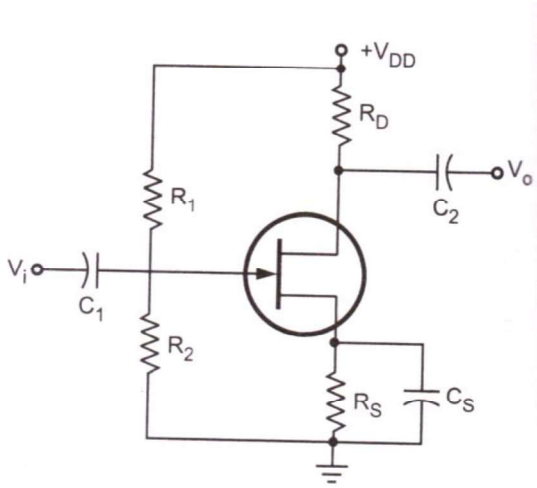


Fig 1.16. Voltage divider bias

The voltage at the source of the JFET must be more positive than the voltage at the gate in order to keep the gate source junction reverse biased. The source voltage is,

$$V_S = I_D R_S$$

DC analysis:

Step 1: Calculate V_G

Using voltage divider theorem,

$$V_G = \frac{R_2}{R_1 + R_2} \times V_{DD}$$

Step 2: To calculate V_{GS}

$$V_G - V_{GS} - I_D R_s = 0$$

$$V_{GS} = V_G - I_D$$

Step 3: To calculate I_{DQ}

$$I_{DQ} = I_{DSS} \left(1 - \frac{V_{GS}}{V_P}\right)^2$$

Step 4: To calculate V_{DS}

$$V_{DD} - I_D R_D - V_{DS} - I_D R_S = 0$$

$$V_{DS} = V_{DD} - I_D R_D - I_D R_S$$

$$V_{DS} = V_{DD} - I_D (R_D + R_S)$$

1.10.3. Self bias:

Self bias is the most common type of JFET bias.

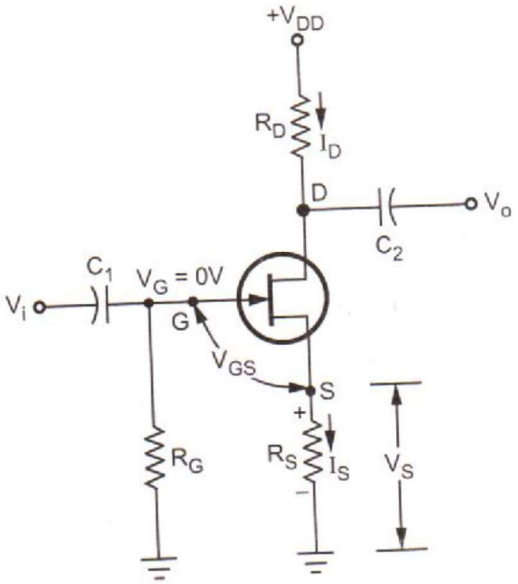


Fig 1.17. Self bias

DC analysis:

Step 1: Calculate V_{GS}

$$V_S = I_S R_S = I_D R_S$$

Step 2: Calculate V_{GS}

$$V_G - V_{GS} - I_D R_s = 0$$

$$V_{GS} = I_D R_s \qquad \because V_G = 0$$

Step 3: Calculate I_{DQ}

$$I_{DQ} = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$I_{DQ} = I_{DSS}\left(1 + \frac{I_D R_S}{V_P}\right)^2$$

Step 4: Calculate V_{DS}

$$V_{DD} - I_D R_D - V_{DS} - I_D R_S = 0$$

$$V_{DS} = V_{DD} - I_D(R_D + R_S)$$

1.11. Biasing of MOSFET:

1.11.1. Biasing of EMOSFET common source circuit:

Applying voltage divider theorem,

$$V_G = V_{GS} = \left(\frac{R_2}{R_1 + R_2}\right) \times V_{DD}$$

$$I_D = K_n (V_G - V_T)^2$$

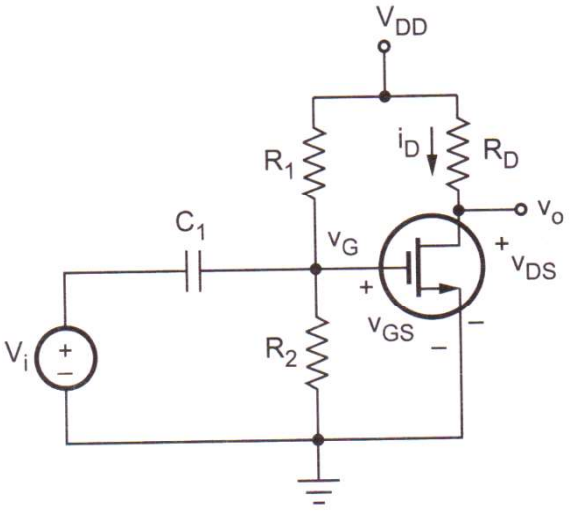


Fig 1.18. NMOS common source circuit

Applying KVL to the drain circuit,

$$V_{DD} - I_D R_D - V_{DS} = 0$$

$$V_{DS} = V_{DD} - I_D R_D$$

1. If $V_{DS} > V_{DS\,(sat)} = V_{GS} - V_T$, then the MOSFET is biased inthe saturation region.

2. If $V_{DS} < V_{DS\,(sat)}$, then the MOSFET is biased in the saturation region & the drain current is given by,

$$I_D = K_n[2(V_{GS} - V_T)V_{DS} - V_{DS}^2]$$

1.11.2. Common MOSFET configuration:

1.11.2.1. CS circuit with source resistor:

$$\text{As} \qquad I_G = 0$$

$$V_G = \left(\frac{R_2}{R_1 + R_2}\right) V_{DD}$$

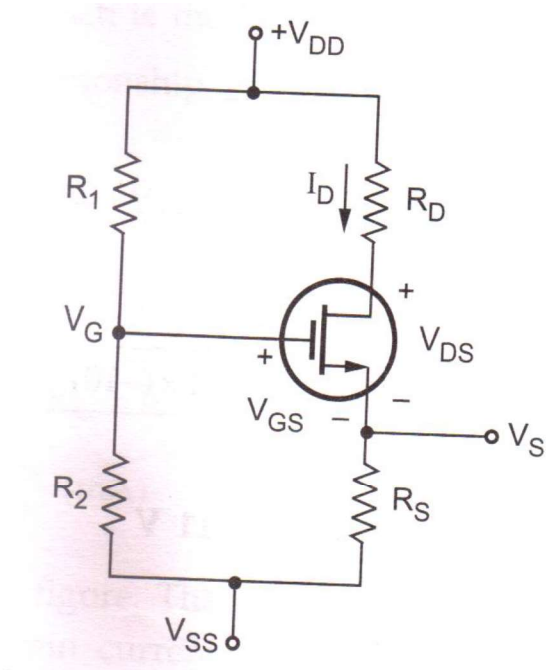


Fig 1.19. NMOS CS circuit with source resistor

Applying KVL to input circuit,

$$V_G - V_{GS} - V_S = 0$$

$$V_{GS} = V_G - I_S R_S$$

$$V_{GS} = V_G - I_D R_S$$

$$V_{DD} - I_D R_D - V_{DS} - I_D R_S = 0$$

$$V_{DS} = V_{DD} - I_D (R_D + R_S)$$

1.11.3. Biasing circuit for DMOSFET:

Biasing circuits for depletion type MOSFET are quite similar to the circuits used for JFET biasing. The only one difference is that V_{GS} is positive for n-channel.

$$V_G = \frac{R_2}{R_1 + R_2} \times V_{DD}$$

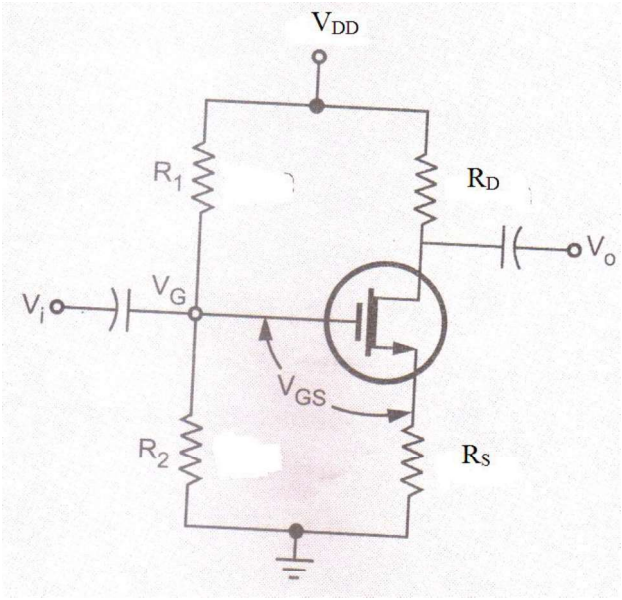


Fig 1.20. Biasing circuit for DMOSFET

$$V_G - V_{GS} - V_S = 0$$

$$V_{GS} = V_G - I_D R_s$$

1.12. Rectifiers:

Rectifier is defined as an electronic device used for converting a.c. voltage into d.c. voltage. Rectifiers are classified into three types. They are,

1. Half - wave rectifier
2. Full- wave rectifier
3. Bridge rectifier

1.12.1. Half wave rectifier:

It converts an a.c. voltage into a pulsating d.c. voltage using only one half of the applied a.c. voltage. The rectifying diode conducts during one of the a.c. cycle only. Let V_i be the voltage to the primary of the transformer & given by the equation,

$$V_i = V_m \sin \omega t, \qquad V_m \gg V_r$$

Where, V_r –cut-in voltage of the diode

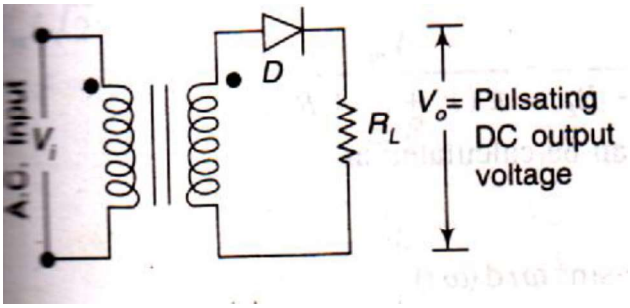


Fig 1.21. Basic structure of a half wave rectifier

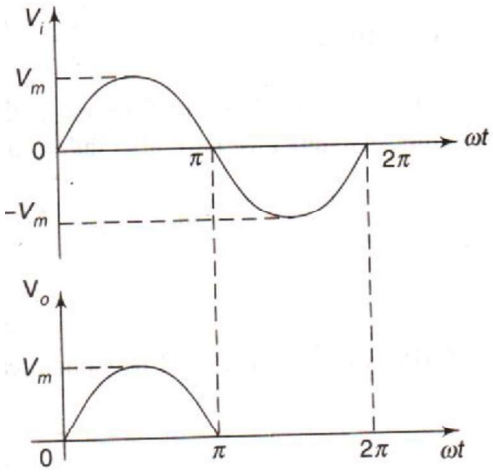


Fig 1.22. Input & output waveforms of half-wave rectifier

During the positive half cycle of the input, anode becomes more positive with respect to the cathode & hence diode D conducts. For an ideal diode, the forward voltage drop is zero. So the whole input voltage will appear across the load resistance, R_L.

During negative half cycle of the input signal, the anode of the diode becomes negative with respect to the cathode & hence diode D does not conduct. For an ideal diode, the impedance offered by the diode is infinity. So th3 whole input voltage appears across diode D. Hence, the voltage drop across R_L is zero.

i) Ripple factor(Γ):

The ratio of rms value of ac component to the d.c. component in the output is known as ripple factor(Γ).

$$\Gamma = \frac{\text{rms value of ac component}}{\text{dc value of component}} = \frac{V_{r,rms}}{V_{dc}}$$

$$\text{where, } V_{r,rms} = \sqrt{V_{rms}^2 - V_{dc}^2}$$

$$\Gamma = \sqrt{\left(\frac{V_{rms}}{V_{dc}}\right)^2 - 1}$$

V_{av} is the average or the d.c. content of the voltage across the load & is given by,

$$V_{av} = V_{dc} = \frac{1}{2\pi}\left[\int_0^{\pi} V_m \sin\omega t d(\omega t)\right]$$

$$= \frac{V_m}{2\pi}[-\cos\omega t]_0^{\pi}$$

$$= \frac{V_m}{2\pi}[1+1]$$

$$V_{av} = \frac{V_m}{\pi}$$

$$I_{dc} = \frac{V_{dc}}{R_L} = \frac{V_m}{\pi R_L} = \frac{I_m}{\pi} \qquad \because I_m = \frac{V_m}{R_L}$$

RMS voltage at the load resistance can be calculated as,

$$V_{rms} = \left[\frac{1}{2\pi}\int_0^{\pi} V_m^2 \sin^2\omega t d(\omega t)\right]^{\frac{1}{2}}$$

$$= V_m \left[\frac{1}{2\pi}\int_0^{\pi} (1 - \cos 2\omega t)\, d(\omega t)\right]^{\frac{1}{2}} \quad \because \sin^2 \omega t = \frac{1 - \cos 2\omega t}{2}$$

$$= \frac{V_m}{2}\left[\frac{1}{\pi}\int_0^{\pi} \left(\omega t - \frac{\sin 2\omega t}{2}\right)_0^{\pi}\right]^{\frac{1}{2}}$$

$$= \frac{V_m}{2}\left[\frac{1}{\pi}\int_0^{\pi} (\pi - 0 - 0 + 0)\right]^{\frac{1}{2}} = \frac{V_m}{2}$$

$$\therefore \Gamma = \sqrt{\left[\frac{V_m/2}{V_m/\pi}\right]^2 - 1}$$

$$= \sqrt{\left(\frac{\pi}{2}\right)^2 - 1} = 1.21$$

From this expression it is clear that the amount of a.c. present in the output is 12% of the d.c. voltage. So the half wave rectifier is not practically useful in converting a.c. into d.c.

ii) Efficiency:

The ratio of d.c. output power to a.c. input power is known as rectifier efficiency(η).

$$\eta = \frac{\text{dc output power}}{\text{ac input power}} = \frac{P_{dc}}{P_{ac}}$$

$$= \frac{V_{dc}^2 / R_L}{V_{rms}^2 / R_L} = \frac{(V_m/\pi)^2}{(V_m/2)^2} = \frac{4}{\pi^2} = 0.406$$

$$\eta = 40.6\%$$

The maximum efficiency of a half wave rectifier is 40.6%.

iii) Peak inverse voltage(PIV):

It is defined as the maximum reverse voltage that a diode can withstand without destroying the junction. The peak inverse voltage across a diode is the peak of the negative half cycle. For hail-wave rectifier, PIV is V_m.

iv) Transformation utilisation factor(TUF):

In the design of any power supply, the rating of the transformer should be determined. This can be done with a knowledge of the d.c. power delivered to the load & the type of rectifying circuit used.

$$\text{TUF} = \frac{\text{d. c. power delivered to the load}}{\text{a. c. rating of the transformer secondary}} = \frac{P_{dc}}{P_{ac}\,\text{rated}}$$

In the half wave rectifying circuit, the rated voltage of the transformer secondary is $V_m / \sqrt{2}$, but the actual rms current flowing through the winding is only $I_m/2$, not $I_m / \sqrt{2}$.

$$\text{TUF} = \frac{\frac{V_m^2}{\pi^2 \times R_L}}{\frac{V_m}{\sqrt{2}} \times \frac{I_m}{2}}$$

$$= \frac{\frac{V_m^2}{\pi^2 \times R_L}}{\frac{V_m}{\sqrt{2}} \times \frac{V_m}{2 \times R_L}} = \frac{2\sqrt{2}}{\pi^2} = 0.287$$

The TUF for a half wave rectifier is 0.287.

v) Form factor:

$$\text{Form factor} = \frac{\text{rms value}}{\text{average value}}$$

$$= \frac{V_m/2}{V_m/\pi} = \frac{\pi}{2} = 1.57$$

vi) Peak factor:

$$\text{Peak factor} = \frac{\text{peak value}}{\text{rms value}}$$

$$= \frac{V_m}{V_m/2} = 2$$

1.12.2. Full wave rectifier:

It converts an a.c. voltage into a pulsating d.c. voltage using both half cycles of the applied a.c. voltage.It uses two diodes of which one conducts during one half cycle while the other diode conducts during the other half cycle of the applied a.c. voltage.

During positive half of the input signal, anode of diode D_1 becomes positive & at the same time the anode of diode D_2 becomes negative. Hence D_1 conducts & D_2 does not conduct. The load current flows through D_1 and the voltage drop across R_L will be equal to the input voltage.

During the negative half cycle of the input, the anode of D_1 becomes negative & the anode of D_2 becomes positive. Hence,D_1 does not conduct & D_2 conducts.

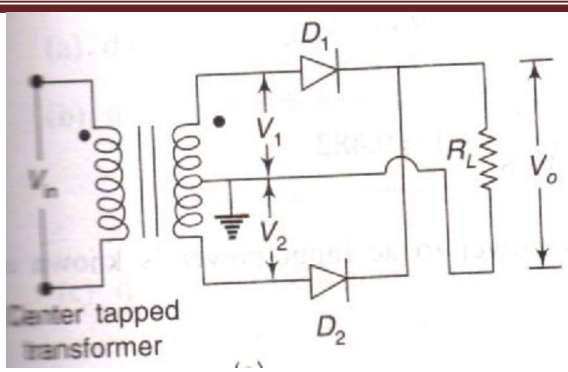


Fig 1.23. Basic structure of a full wave rectifier

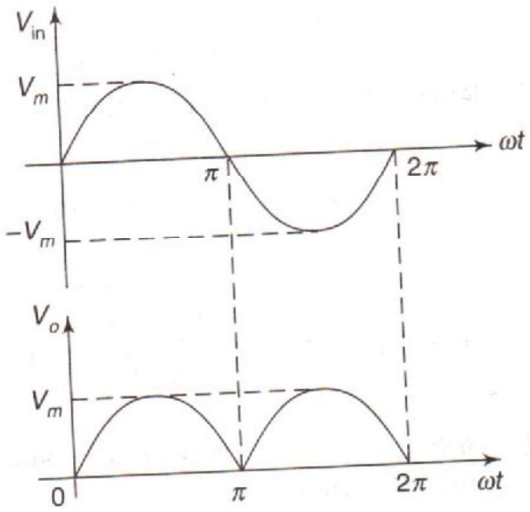


Fig 1.24. Input & output waveforms of full wave rectifier

i) Ripple factor(Γ):

$$\Gamma = \sqrt{\left(\frac{V_{rms}}{V_{dc}}\right)^2 - 1}$$

The average voltage or d.c. voltage available across the load resistance is,

$$V_{av} = V_{dc} = \frac{1}{\pi}\left[\int_0^{\pi} V_m \sin \omega t d(\omega t)\right]$$

$$= \frac{V_m}{\pi}[-\cos \omega t]_0^{\pi}$$

$$= \frac{V_m}{\pi}[1+1]$$

$$V_{av} = \frac{2V_m}{\pi}$$

$$I_{dc} = \frac{V_{dc}}{R_L} = \frac{2V_m}{\pi R_L} = \frac{2I_m}{\pi} \qquad \because I_m = \frac{V_m}{R_L}$$

RMS voltage at the load resistance can be calculated as,

$$V_{rms} = \left[\frac{1}{\pi}\int_0^{\pi} V_m^2 \sin^2 \omega t \, d(\omega t)\right]^{\frac{1}{2}}$$

$$= V_m \left[\frac{1}{2\pi}\int_0^{\pi} (1 - \cos 2\omega t)\, d(\omega t)\right]^{\frac{1}{2}}$$

$$\because \sin^2 \omega t = \frac{1 - \cos 2\omega t}{2}$$

$$= \frac{V_m}{\sqrt{2}}\left[\frac{1}{\pi}\int_0^{\pi} \left(\omega t - \frac{\sin 2\omega t}{2}\right)_0^{\pi}\right]^{\frac{1}{2}}$$

$$= \frac{V_m}{\sqrt{2}}\left[\frac{1}{\pi}\int_0^{\pi} (\pi - 0 - 0 + 0)\right]^{\frac{1}{2}}$$

$$= \frac{V_m}{\sqrt{2}}$$

$$\therefore \Gamma = \sqrt{\left[\frac{V_m/\sqrt{2}}{2V_m/\pi}\right]^2 - 1}$$

$$= \sqrt{\left(\frac{\pi}{2\sqrt{2}}\right)^2 - 1} = 0.482$$

ii) Efficiency:

The ratio of d.c. output power to a.c. input power is known as rectifier efficiency(η).

$$\eta = \frac{\text{dc output power}}{\text{ac input power}} = \frac{P_{dc}}{P_{ac}}$$

$$= \frac{V_{dc}^2 / R_L}{V_{rms}^2 / R_L} = \frac{(2V_m/\pi)^2}{(V_m/\sqrt{2})^2} = \frac{8}{\pi^2} = 0.812$$

$$\eta = 81.2\%.$$

The maximum efficiency of a half wave rectifier is 81.2%.

iii) Peak inverse voltage(PIV):

The peak inverse voltage for full-wave rectifier is $2V_m$, because the entire secondary voltage appears across the non-conducting device.

iv) Transformation utilisation factor(TUF):

The average TUF in a full wave rectifying circuit is determined by considering the primary & secondary windings separately and it gives a value of 0.693.

$$TUF = \frac{primary\ of\ TUF + secondary\ of\ TUF}{2}$$

TUF of primary winding= 2× TUT of half wave circuit

$= 2 \times 0.287 = 0.574$

$$\text{TUF of secondary} = \frac{\text{DC power to the load}}{\text{AC power rating of secondary}} = \eta = 0.812$$

$$\text{TUF} = \frac{0.574 + 0.812}{2} = 0.693$$

v) Form factor:

$$\text{Form factor} = \frac{\text{rms value}}{\text{average value}}$$

$$= \frac{V_m/\sqrt{2}}{2V_m/\pi} = \frac{\pi}{2\sqrt{2}} = 1.11$$

vi) Peak factor:

$$\text{Peak factor} = \frac{\text{peak value}}{\text{rms value}}$$

$$= \frac{V_m}{V_m/\sqrt{2}} = \sqrt{2}$$

1.12.3. Bridge rectifier:

The need for a center tapped transformer in full wave rectifier is eliminated in the bridge rectifier. The bridge rectifier has four diodes connected to form a bridge.

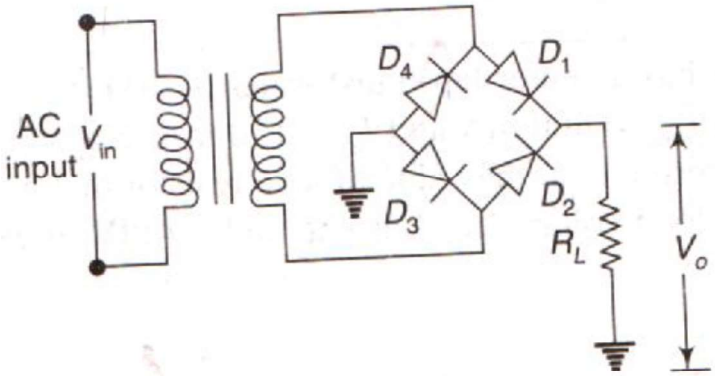


Fig 1.25. Basic structure of a bridge rectifier

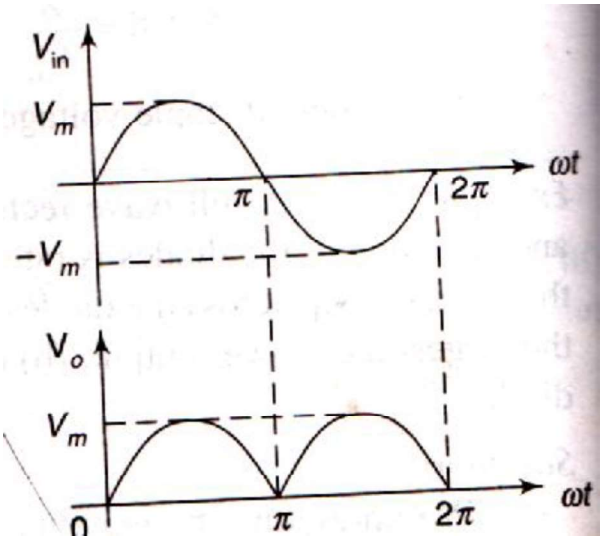


Fig 1.26. Input & output waveforms of bridge rectifier

The a.c. input is voltage is applied to the diagonally opposite ends of the bridge. The load resistance is connected between the other two ends of the bridge.

For the positive half cycle of the input a.c. voltage, diodes D_1 & D_3 conduct, whereas D_2 & D_4 do not conduct. The conductivity diodes will be in series through the load current flows through R_L.

During the negative half cycle of the input a.c. voltage, diodes D_2 & D_4 conduct, whereas diodes D_1 & D_3 do not conduct. The conducting diode D_2 & D_4 will be series through the load R_L & the current flows through RL in the same direction as in the previous half cycle.

i) Ripple factor(Γ):

$$\Gamma = \sqrt{\left(\frac{V_{rms}}{V_{dc}}\right)^2 - 1}$$

The average voltage or d.c. voltage available across the load resistance is,

$$V_{av} = V_{dc} = \frac{1}{\pi}\left[\int_0^{\pi} V_m \sin \omega t d(\omega t)\right]$$

$$= \frac{V_m}{\pi}[-\cos \omega t]_0^{\pi}$$

$$= \frac{V_m}{\pi}[1 + 1]$$

$$V_{av} = \frac{2V_m}{\pi}$$

$$I_{dc} = \frac{V_{dc}}{R_L} = \frac{2V_m}{\pi R_L} = \frac{2I_m}{\pi} \qquad \because I_m = \frac{V_m}{R_L}$$

RMS voltage at the load resistance can be calculated as,

$$V_{rms} = \left[\frac{1}{\pi}\int_0^{\pi} V_m^2 \sin^2 \omega t d(\omega t)\right]^{\frac{1}{2}}$$

$$= V_m\left[\frac{1}{2\pi}\int_0^{\pi} (1 - \cos 2\omega t)\, d(\omega t)\right]^{\frac{1}{2}} \quad \because \sin^2 \omega t = \frac{1 - \cos 2\omega t}{2}$$

$$= \frac{V_m}{\sqrt{2}}\left[\frac{1}{\pi}\int_0^{\pi} \left(\omega t - \frac{\sin 2\omega t}{2}\right)_0^{\pi}\right]^{\frac{1}{2}}$$

$$= \frac{V_m}{\sqrt{2}}\left[\frac{1}{\pi}\int_0^{\pi} (\pi - 0 - 0 + 0)\right]^{\frac{1}{2}}$$

$$= \frac{V_m}{\sqrt{2}}$$

$$\therefore \Gamma = \sqrt{\left[\frac{V_m/\sqrt{2}}{2V_m/\pi}\right]^2 - 1}$$

$$= \sqrt{\left(\frac{\pi}{2\sqrt{2}}\right)^2 - 1} = 0.482$$

ii) Efficiency:

The ratio of d.c. output power to a.c. input power is known as rectifier efficiency(η).

$$\eta = \frac{\text{dc output power}}{\text{ac input power}} = \frac{P_{dc}}{P_{ac}}$$

$$= \frac{V_{dc}^2 / R_L}{V_{rms}^2 / R_L} = \frac{(2V_m/\pi)^2}{\left(V_m/\sqrt{2}\right)^2} = \frac{8}{\pi^2} = 0.812$$

$$\eta = 81.2\%$$

The maximum efficiency of a half wave rectifier is 81.2%.

iii) Peak inverse voltage (PIV):

The peak inverse voltage for bridge rectifier is V_m, because the entire secondary voltage appears across the non-conducting device.

iv) Transformation utilisation factor(TUF):

The average TUF in a full wave rectifying circuit is determined by considering the primary & secondary windings separately and it gives a value of 0.693.

$$\text{TUF} = \frac{\text{primary of TUF} + \text{secondary of TUF}}{2}$$

TUF of primary winding= 2× TUT of half wave circuit

$$= 2 \times 0.287 = 0.574$$

$$\text{TUF of secondary} = \frac{\text{DC power to the loa}}{\text{AC power rating of secondary}} = \eta = 0.812$$

$$\text{TUF} = \frac{0.574 + 0.812}{2} = 0.693$$

v) Form factor:

$$\text{Form factor} = \frac{\text{rms value}}{\text{average value}}$$

$$= \frac{V_m/\sqrt{2}}{2V_m/\pi} = \frac{\pi}{2\sqrt{2}} = 1.11$$

vi) Peak factor:

$$\text{Peak factor} = \frac{\text{peak value}}{\text{rms value}}$$

$$= \frac{V_m}{V_m/\sqrt{2}} = \sqrt{2}$$

Advantages:

1. No center tap is required in the transformer secondary. Hence, wherever possible, a.c. voltage can directly be applied to the bridge.
2. The current in the secondary of the transformer is in opposite direction in two half cycles. Hence net d.c. component flowing is zero which reduces the losses & danger of saturation.
3. Due to pure alternating current in secondary of transformer, the circuit is used for large powers & high voltage applications.

Disadvantages:

The only disadvantage of bridge rectifier is the use of four diodes as compared to two diodes in normal full wave rectifier. This reduces the output voltage.

1.13. Filters:

The output of a rectifier contains d.c. component as well as a.c. component. Filters are used to minimize the undesirable a.c. i.e)ripple leaving only the d.c. component to appear at the output. Some important filters are,

1. Inductor filter
2. Capacitor filter
3. LC filter (or) L section filter
4. CLC filter(or) π filter

1.13.1. Inductor filter

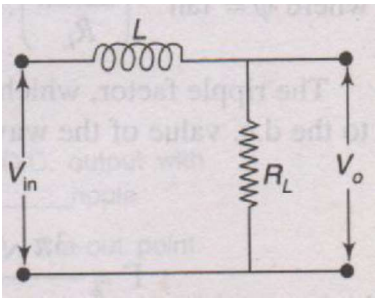


Fig 1.27. Inductor filter

When the output of the rectifier passes through an inductor, it blocks the a.c. component & allows only the d.c. component to reach the load. To analyse this filter for a full wave, the Fourier series can be written as,

$$V_o = \frac{2V_m}{\pi} - \frac{4V_m}{\pi}\left[\frac{1}{3}\cos 2\omega t + \frac{1}{15}\cos 4\omega t + \frac{1}{35}\cos 6\omega t + \cdots\right]$$

$$\text{The d. c. component is } \frac{2V_m}{\pi}$$

Assuming the third & higher terms contribute little output, the output voltage is,

$$V_o = \frac{2V_m}{\pi} - \frac{4V_m}{\pi}\left[\frac{1}{3}\cos 2\omega t\right]$$

The diode, choke & transformer resistance can be neglected since they are very small as compared with R_L. Therefore, the d.c. component of current $I_m = \frac{V_m}{R_L}$.

The impedance of series combination of L & R_L at 2ω is,

$$Z = \sqrt{R_L^2 + (2\omega L)^2}$$

$$= \sqrt{R_L^2 + 4\omega^2 L^2}$$

The a.c. component is,

$$I_m = \frac{V_m}{\sqrt{R_L^2 + 4\omega^2 L^2}}$$

Therefore, the resulting current i is given by,

$$i = \frac{2V_m}{\pi R_L} - \frac{4V_m}{3\pi} \times \frac{\cos(2\omega t - \Phi)}{\sqrt{R_L^2 + 4\omega^2 L^2}}$$

$$\text{Where, } \Phi = \tan^{-1}\left(\frac{2\omega L}{R_L}\right)$$

The ripple factor, which can be defined as the ratio of the rms value of the ripple to the d.c. value of the wave is,

$$\Gamma = \frac{\frac{4V_m}{3\pi\sqrt{2}\sqrt{R_L^2 + 4\omega^2 L^2}}}{\frac{2V_m}{\pi R_L}} \qquad \because I_{rms} = \frac{I_{ac}}{\sqrt{2}}$$

$$\Gamma = \frac{2}{3\sqrt{2}} \times \frac{R_L}{\sqrt{R_L^2 + 4\omega^2 L^2}}$$

$$\Gamma = \frac{2}{3\sqrt{2}} \times \frac{1}{\sqrt{1 + \frac{4\omega^2 L^2}{R_L^2}}}$$

$$\Gamma = \frac{R_L}{3\sqrt{2}\omega L} \qquad \because \frac{4\omega^2 L^2}{R_L^2} \gg 1$$

It shows that the ripple factor will decrease when L is increased & R_L is decreased. Clearly, the inductor filter is more effective only when the load current is high(small R_L). The large value of the inductor can reduce the ripple & at the same time the output d.c. voltage will be lowered as the inductor has a higher d.c. resistance. The operation of the inductor filter depends on its well known fundamental property to oppose any change of current passing through it.

1.13.2. Capacitor filter (or) C filter:

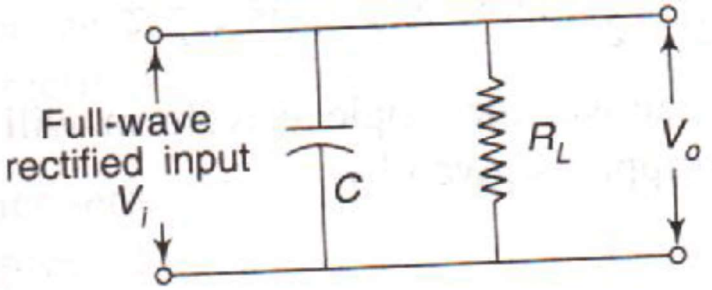


Fig 1.28. Capacitor filter

An inexpensive filter for light loads is found in the capacitor filter which is connected directly across the load. The property of a capacitor is that it allows a.c. component & blocks the d.c. component. The operation of a capacitor filter is to short the ripple to ground but leave the d.c. to appear at the output when it is connected across a pulsating d.c. voltage.

During the positive half cycle, the capacitor charges up to the peak value of the transformer secondary voltage, V_m and will try to maintain this value as the full wave input drops to zero. The capacitor will discharge through R_L slowly until the transformer secondary voltage again increases to a value greater than the capacitor voltage.

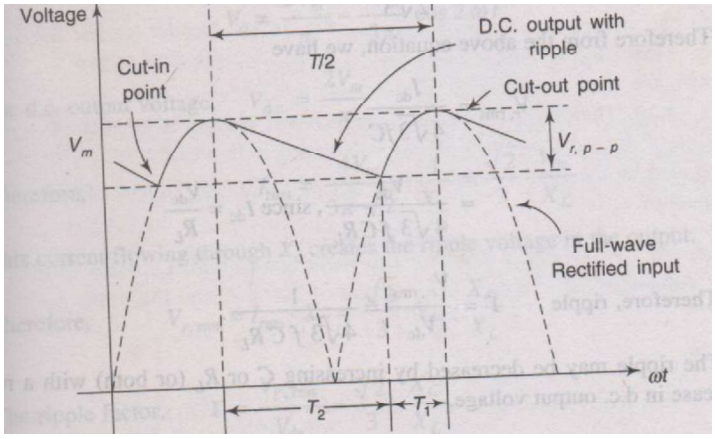


Fig 1.29. Ripple voltage triangular waveform

`The diode conducts for a period which depends on the capacitor voltage. The diode will conduct when the transformer secondary voltage becomes more than the diode voltage. This is called cut-in voltage. The diode stops conducting when the transformer voltage becomes less than the diode voltage. This is called cut-out voltage. The ripple voltage waveform can be assumed as triangular. From the cut-in point to the cut-out point, whatever charge the capacitor acquires is equal to the charge the capacitor has lost during the period of conduction i.e.)from cut-out point to the next cut-in point.

The charge it has acquired=$V_{r,pp} \times C$

The charge it has lost=$I_{dc} \times T_2$

$$\therefore V_{r,pp} \times C = I_{dc} \times T_2$$

If the value of the capacitor is fairly large, or the value of the load resistance is very large, then it can be assumed that the time T_2 is equal to half the periodic time of the waveform.

$$T_2 = \frac{T}{2} = \frac{1}{2f}\ , \text{then } V_{r,pp} = \frac{I_{dc}}{2fc}$$

With the assumptions made, the ripple waveform will be triangular in nature and the rms value of the ripple is given by,

$$V_{r,rms} = \frac{V_{r,pp}}{2\sqrt{3}}$$

$$V_{r,rms} = \frac{I_{dc}}{4\sqrt{3}fC}$$

$$= \frac{V_{dc}}{4\sqrt{3}fCR_L} \qquad \because I_{dc} = \frac{V_{dc}}{R_L}$$

$$\therefore \text{Ripple}, \Gamma = \frac{V_{r,rms}}{V_{dc}}$$

$$\Gamma = \frac{1}{4\sqrt{3}fCR_L}$$

The ripple may be decreased by increasing C (or) R_L (or both) with a resulting increase in d.c. output voltage.

1.13.3. LC filter:

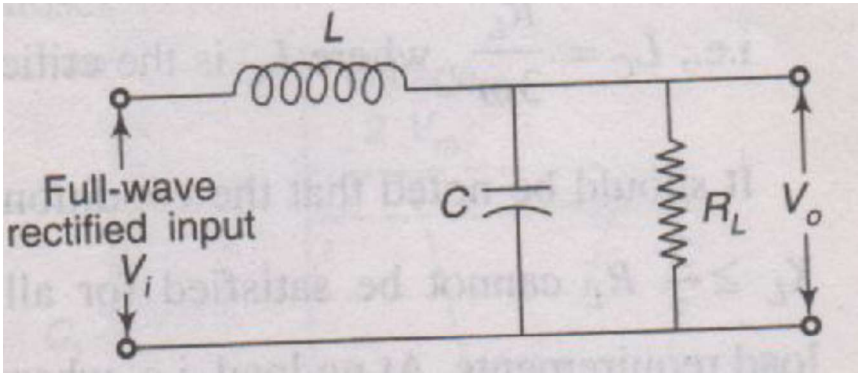


Fig 1.30. LC filter

The ripple factor is directly proportional to the load resistance R_L in the inductor filter and inversely proportional to R_L in the capacitor filter. Therefore, if these two filters are combined as LC filter (or) L-section filter, the ripple factor will be independent of R_L.

If the value of the inductance is increased, it will increase the time of conduction. At some critical value of inductance, one diode, either D1 or D2 in full-wave rectifier will always be conducting.

From Fourier series, the output voltage can be expressed as,

$$V_o = \frac{2V_m}{\pi} - \frac{4V_m}{\pi}\left[\frac{1}{3}\cos 2\omega t\right]$$

The d.c. output voltage,

$$V_{dc} = \frac{2V_m}{\pi}$$

$$I_{rms} = \frac{4V_m}{3\pi\sqrt{2}} \times \frac{1}{X_L}$$

$$= \frac{\sqrt{2}}{3} \times \frac{V_{dc}}{X_L}$$

The current flowing through X_C creates the ripple voltage in the output.

$$\therefore V_{r,rms} = I_{rms} \times X_C = \frac{\sqrt{2}}{3} \times V_{dc} \times \frac{X_C}{X_L}$$

The ripple factor,

$$\Gamma = \frac{V_{r,rms}}{V_{dc}} = \frac{\sqrt{2}}{3} \times \frac{X_C}{X_L}$$

$$\Gamma = \frac{\sqrt{2}}{3} \times \frac{1}{4\omega^2 CL} \qquad \because X_C = \frac{1}{2\omega C}, X_L = 2\omega L$$

1.13.4. CLC filter (or) π -section filter:

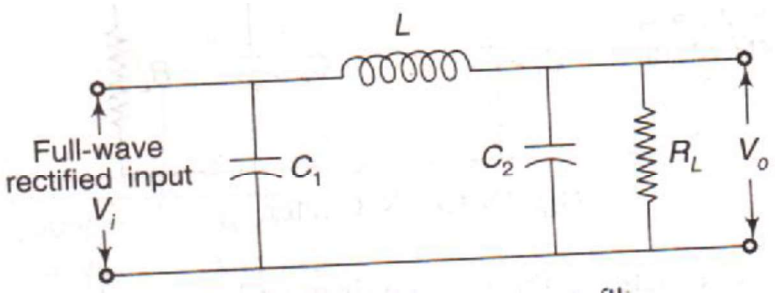


Fig 1.30. LC filter

The CLC (or) π -type filter which basically consists of a capacitor filter followed by an LC section. This filter offers a fairly smooth output, and is characterised by a highly peaked diode currents & poor regulation.

Output of the capacitor filter,

$$V_{r,pp} = \frac{I_{dc}}{2fC_1} = \frac{I_{dc}}{2 \times \frac{\omega}{2\pi} \times C_1} = \frac{\pi I_{dc}}{\omega C_1}$$

$$= \frac{\pi V_{dc}}{\omega C_1 R_L} \qquad \because I_{dc} = \frac{V_{dc}}{R_L}$$

$$V_{r,rms} = \frac{V_{r,pp}}{\pi\sqrt{2}}$$

$$= \frac{\pi V_{dc}}{\omega C_1 R_L \times \pi\sqrt{2}}$$

$$= \frac{\sqrt{2} V_{dc}}{2\omega C_1 R_L}$$

$\because$ multiplying $\sqrt{2}$ in both numerator & *denominator*

$$= \frac{\sqrt{2} V_{dc}}{R_L} \times X_{C1} \qquad \because X_C = \frac{1}{2\omega C}$$

Output of the L-section,

$$V_{r,rms}' = \frac{V_{r,rms} \times X_{C2}}{X_L - X_{C2}} \qquad \because \text{Using voltage division rule}$$

$$= \frac{V_{r,rms}}{\frac{X_L}{X_{C2}} - 1} = \frac{V_{r,rms}}{2\omega L \times 2\omega C2 - 1} \qquad \because X_L = 2\omega L, X_C = \frac{1}{2\omega C}$$

$$= \frac{V_{r,rms}}{4\omega^2 L C_2} \qquad \because 4\omega^2 L C_2 \gg 1$$

$$V_{r,rms}' = \frac{X_{C2}}{X_L} \times V_{r,rms}$$

$$\Gamma = \frac{V_{r,rms}'}{V_{dc}}$$

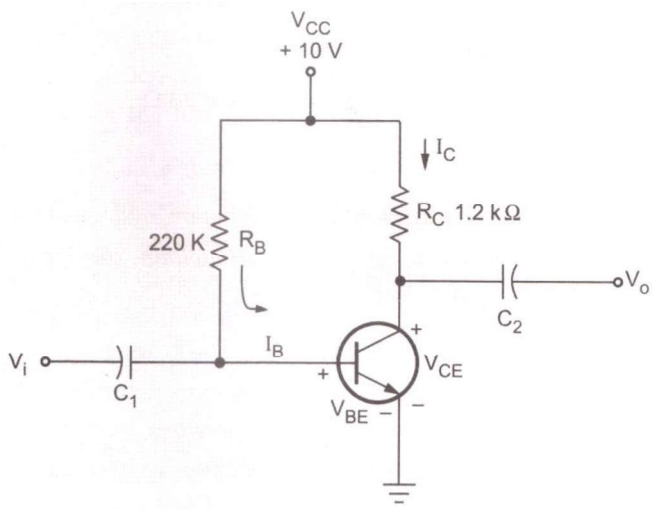
$$V_{r,rms}' = \frac{X_{C2}}{X_L} \times \frac{\sqrt{2} V_{dc}}{R_L} \times X_{C1}$$

$$\Gamma = \frac{\frac{X_{C2}}{X_L} \times \frac{\sqrt{2} V_{dc}}{R_L} \times X_{C1}}{V_{dc}}$$

$$\Gamma = \sqrt{2} \times \frac{X_{C2}}{X_L} \times \frac{X_{C1}}{R_L}$$

SOLVED EXAMPLES:

1. For the circuit shown in fig calculate $I_B, I_C, V_{CE}, V_B, V_C$ and V_{BC}. Assume V_{BE}=0.7V and $\beta = 50$.



Solution:

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{10 - 0.7}{220 \times 10^3} = 42.27\mu A$$

$$I_C = \beta I_B = 50 \times 42.27 \times 10^{-6} = 2.1135mA$$

$$V_{CE} = V_{CC} - I_C R_C = 10 - 2.1135 \times 10^{-3} \times 1.2 \times 10^3 = 7.4638V$$

$$V_B = V_{BE} = 0.7V$$

$$V_C = V_{CE} = 7.4638V$$

$$V_{BC} = V_B - V_C = 0.7 - 7.4638 = -6.7638$$

The negative voltage V_{BC} indicates that base-collector junction is reverse biased.

2. Design a fixed bias circuit to have operating point of (10V,3mA). The circuit is supplied with 20V and uses a silicon transistor of h_{fe}=250.

Solution:

Applying KVL to collector circuit we get,

$$V_{CC} - V_{CE} - I_C R_C = 0$$

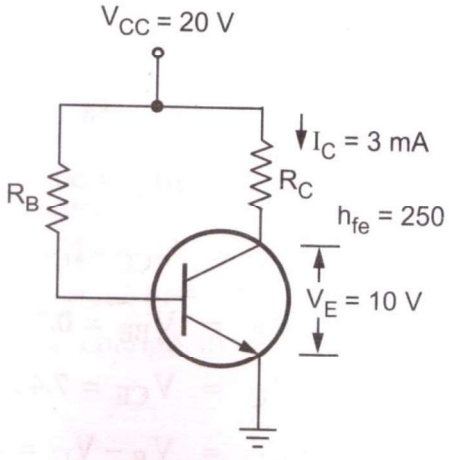
$$R_C = \frac{V_{CC} - V_{CE}}{I_C} = \frac{20 - 10}{3mA} = 3.33K$$

$$I_B = \frac{I_C}{\beta} = \frac{3mA}{250} = 12\mu A$$

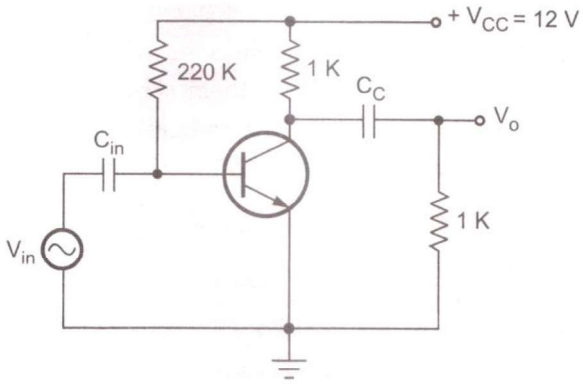
Now, applying KVL to base circuit we get,

$$V_{CC} - I_B R_B - V_{BE} = 0$$

$$R_B = \frac{V_{CC} - V_{BE}}{I_B} = \frac{20 - 0.7}{12\mu A} = 1.6M\Omega$$



3. The circuit of BJT amplifier is shown in fig. Draw d.c. load lines. Also find the Q-point. Assume V_{BE}=0.7 Volts.



Solution:

Step 1 : Obtain I_{CQ} , V_{CEQ}, point A and point B

Applying KVL to the base circuit we have

$$V_{CC} - I_B R_B - V_{BE} = 0$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{12 - 0.7}{220K} = 51.36\mu A$$

$$I_{CQ} = \beta I_B = 100 \times 51.36\mu A = 5.136mA$$

Applying KVL to the collector circuit we have

$$V_{CC} - I_C R_C - V_{CEQ} = 0$$

$$V_{CEQ} = V_{CC} - I_C R_C = 12 - 5.136 \times 10^{-3} \times 1000 = 6.864V$$

Thus Q-point is $I_{CQ}, V_{CEQ} = 3.424mA, 6.864V$

Step-2: Mark axes intersection points

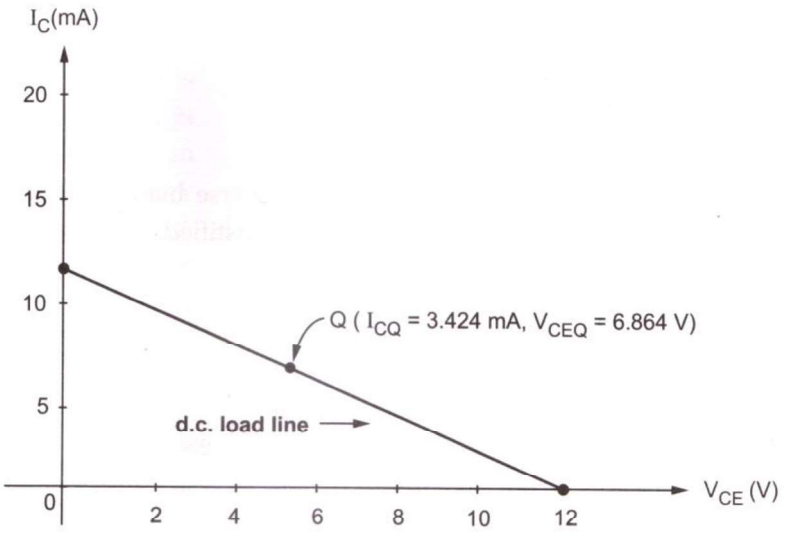
Point A:

$$V_{CE} = V_{CC} = 12V \text{ at } I_c = 0$$

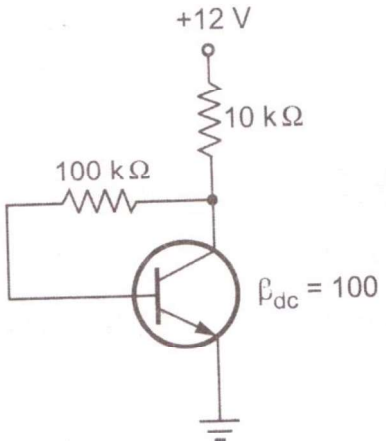
Point B:

$$I_C = \frac{V_{CC}}{R_{dc}} = \frac{V_{CC}}{R_C} = \frac{12}{1K} = 12mA$$

Step 3: Draw dc load line



4. Calculate the Q point values (I_C and V_{CE}) for the circuit in Fig.



Solution:

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (1+\beta)R_C}$$

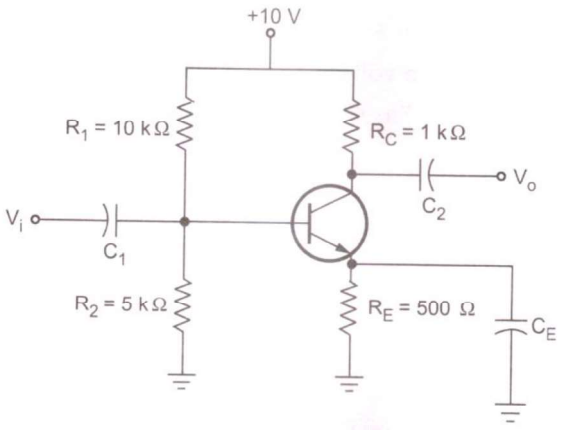
$$= \frac{12 - 0.7}{100 \times 10^3 + [(1+100) \times 10 \times 10^3]} = 10.18\mu A$$

$$I_C = \beta I_B = 100 \times 10.18\mu A = 1.018mA$$

$$V_{CE} = V_{CC} - (I_B + I_C)R_C$$

$$= 12 - (10.18 \times 10^{-6} + 1.018 \times 10^{-3}) \times 10 \times 10^3 = 1.7182V$$

5. For the circuit shown in Fig, β= 100 for the silicon transistor. Calculate V_{CE} and I_C.



Solution:

$$V_{TH} \cong \frac{R_2}{R_1 + R_2} V_{CC} = \frac{5 \times 10^3}{10 \times 10^3 + 5 \times 10^3} \times 10 = 3.33V$$

$$R_B = \frac{10 \times 5}{10 + 5} = 3.33K\Omega$$

Appling KVL to base circuit we have,

$$V_{TH} - I_B R_B - V_{BE} - (1 + \beta) I_B R_E = 0$$

$$I_B = \frac{V_{TH} - V_{BE}}{R_B + (1 + \beta) R_E} = \frac{3.33 - 0.7}{3.33 \times 10^3 + (101)500} = 48.86\mu A$$

$$IC = \beta IB = 100 \times 48.86\mu A = 4.886mA$$

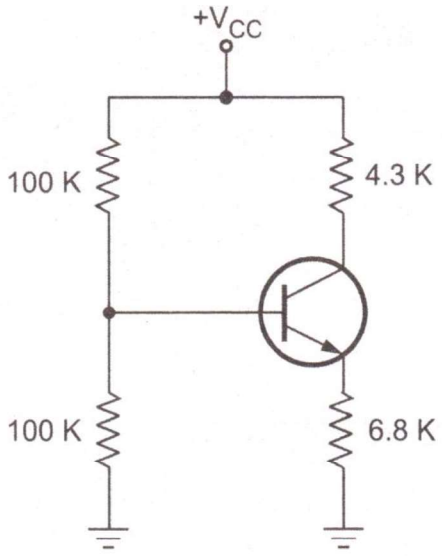
$$I_E = I_B + I_C = 4.935mA$$

Appling KVL to collector circuit we have,

$$V_{CE} = V_{CC} - I_C R_C - I_E R_E$$

$$= 10 - 4.886 \times 1 - 4.935 \times 0.5 = 2.6465V$$

6. For the transistor circuit in fig find the Q-point $V_{CC} = 15V$ and $\beta = 100, V_{BE} = 0.7V$.



Solution:

$$V_{TH} \cong \frac{R_2}{R_1 + R_2} V_{CC}$$

$$= \frac{100 \times 10^3}{100 \times 10^3 + 100 \times 10^3} \times 15 = 7.5V$$

$$R_B = 100K||100K = 50K$$

Appling KVL to base circuit we have,

$$V_{TH} - I_B R_B - V_{BE} - (1+\beta) I_B R_E = 0$$

$$I_B = \frac{V_{TH} - V_{BE}}{R_B + (1+\beta) R_E}$$

$$= \frac{7.5 - 0.7}{50 \times 10^3 + (101) 6.8 \times 10^3} = 9.23\mu A$$

$$I_C = \beta I_B = 100 \times 9.23\mu A = 0.923mA$$

$$I_E = I_B + I_C = 0.932mA$$

Appling KVL to collector circuit we have,

$$V_{CE} = V_{CC} - I_C R_C - I_E R_E$$

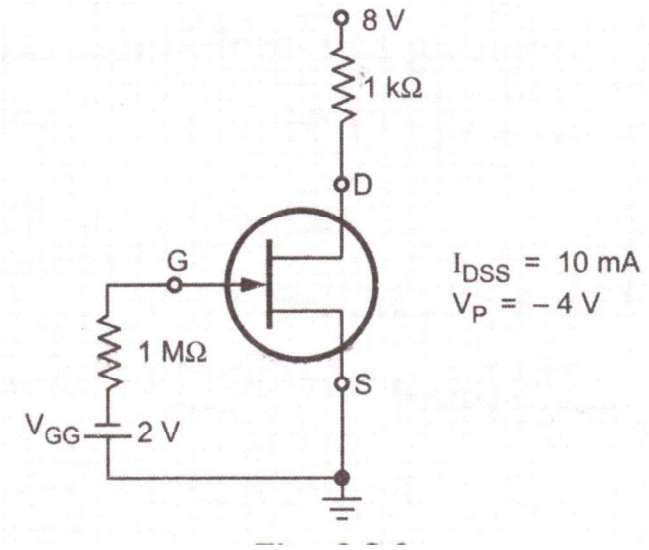
$$= 15 - 0.923 \times 4.3 - 0.923 \times 6.8 = 4.6935V$$

Therefore, Q-point: I_{CQ}=0.923mA and V_{CEQ}=4.6935V.

7. For the circuit shown in the Fig., calculate

a)V_{GSQ} **b)I_{DQ}**

c)V_{DSQ} **d)V_D**



Solution:

a) $V_{GSQ} - = -V_{GG} = -2V$

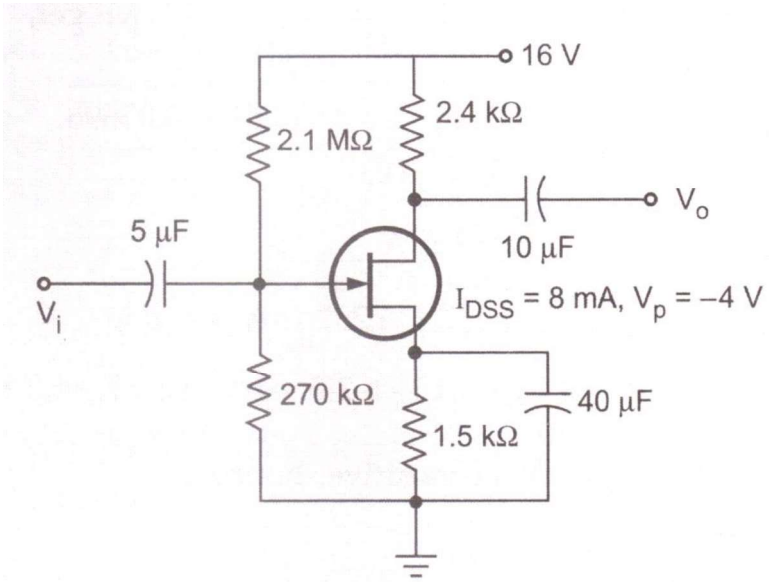
b) $I_{DQ} = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 = 10 \times 10^{-3}\left(1 - \frac{-2V}{-4V}\right)^2$

$= 10 \times 10^{-3}(1 - 0.5)^2 = 10 \times 10^{-3}(0.25) = 2.5mA$

c) $V_{DSQ} = V_{DD} - I_{DQ}R_D = 8V - 2.5 \times 10^{-3}(1 \times 10^3) = 5.5V$

d) $V_D = V_{DS} + V_S = 5.5 + 0 = 5.5V$

8. Determine I_{DQ}, V_{GSQ}, V_D, V_S, V_{DS} and V_{DG} for the network of Fig.



Solution:

Step 1: Calculate V_G

$$V_G = \frac{V_{DD}R_2}{R_1 + R_2} = \frac{16 \times 270K}{2.1M + 270K} = 1.823V$$

Step 2: Obtain expression for V_{GS}

$$V_{GS} = 1.823 - I_D R_S = 1.823 - 1.5 \times 10^{-3} I_D$$

Step 3: Calculate I_D

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$= 8 \times 10^{-3}\left(1 - \frac{(1.823 - I_D \times 1.5 \times 10^3)}{-4}\right)^2$$

$$= 8 \times 10^{-3}[1 - (-0.456 + 375I_D)]$$

$$= 8 \times 10^{-3}(1.456 - 375I_D)$$

$$I_D = 0.01696 - 8.736I_D + 1125I_D^2$$

$$1125I_D^2 - 9.736I_D + 0.01696 = 0$$

Solving quadratic equation using formula,

$$\frac{-b \pm \sqrt{b^2 - 4ac}}{2a}$$

we get,

$$= \frac{-(-9.736) \pm \sqrt{(-9.736)^2 - 4 \times 1125 \times 0.01696}}{2 \times 1125}$$

$$= \frac{9.7361 \pm 4.2976}{2 \times 1125}$$

$$= 6.237\text{mA or } 2.417\text{mA}$$

If we calculate value of V_{DS} taking I_D=6.237mA we get,

$$V_{DS} = V_{DD} - I_D(R_D + R_S) = 16 - 6.237 \times 10^{-3}(2.4K + 1.5K) = -8.3243V$$

Practically, the value of V_{DS} must be positive, hence

$$I_D = 6.237\text{mA is invalid}$$

$$I_D = 2.417\text{mA}$$

Step 4: Calculate V_{DS}, V_{GS}, V_S, V_D and V_{DG}

$$V_{DS} = V_{DD} - I_D(R_D + R_S) = 16 - 2.417 \times 10^{-3}(2.4K + 1.5K) = -6.5737V$$

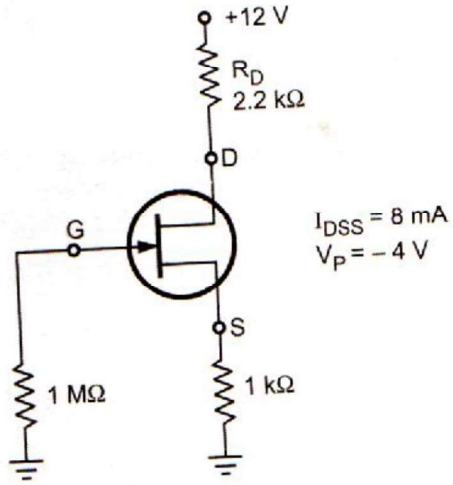
$$V_{GS} = 1.823 - I_D R_S = 1.823 - (2.417 \times 10^{-3} \times 1.5 \times 10^3) = -1.8025V$$

$$V_S = I_D R_S = 2.417 \times 10^{-3} \times 1.5 \times 10^3 = 3.6255V$$

$$V_D = V_{DD} - I_D R_D = 16 - (2.417 \times 10^{-3} \times 1.5 \times 10^3) = 10.2V$$

$$V_{DG} = V_D - V_G = 10.2 - 1.823 = 8.377V$$

9. For the circuit shown in the Fig, calculate V_{GSQ}, I_{DQ}, V_{DS}, V_S, V_D.



Solution:

Step 1: Obtain expression for V_{GS}

$$V_{GS} = -I_D R_S$$

Step 2: Calculate I_D and values of V_{GS} and V_S

$$I_D = I_{DSS}\left(1 - \frac{I_D R_S}{V_P}\right)^2$$

$$I_D = 8 \times 10^{-3}\left(1 + \frac{I_D \times 1 \times 10^3}{-4}\right)^2$$

$$= 8 \times 10^{-3}(1 - 250I_D)^2$$

$$I_D = 8 \times 10^{-3}\,(1 - 500I_D + 62500I_D^2)$$

$$I_D = 8 \times 10^{-3} - 4I_D + 500I_D^2$$

$$500I_D^2 - 5I_D + 8 \times 10^{-3} = 0$$

Solving quadratic equation using formula,

$$\frac{-b \pm \sqrt{b^2 - 4ac}}{2a}$$

we get,

$$= \frac{+5 \pm \sqrt{(-5)^2 - 4 \times 500 \times 8 \times 10^{-3}}}{2 \times 500}$$

$$= \frac{+5 \pm \sqrt{25 - 16}}{1000} = \frac{+5 \pm \sqrt{9}}{1000}$$

$$= \frac{+5 \pm 3}{1000}$$

$$I_D = 8\text{mA or } 2\text{mA}$$

I_{DQ} cannot have value 8mA because maximum value of I_D, I_{DSS} is given as 8mA at V_{GS}=0 and hence I_{DQ} is taken as 2mA.

$$V_{GSQ} = -I_D R_S = -2 \times 10^{-3} \times 1 \times 10^3 = -2V$$

$$V_{GS} = -I_D R_S = -2 \times 10^{-3} \times 1 \times 10^3 = -2V$$

$$V_S = I_D R_S = 2 \times 10^{-3} \times 1 \times 10^3 = 2V$$

Step 3: Calculate V_{DS}

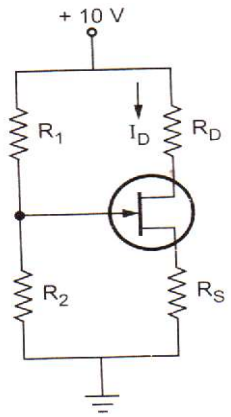
$$V_{DS} = V_{DD} - I_D(R_D + R_S)$$

$$= 12 - 2 \times 10^{-3}(2.2 \times 10^3 + 1 \times 10^3) = 12 - 6.4 = 5.6V$$

Step 4: Calculate V_D

$$V_D = V_{DS} + V_S = 5.6 + 2 = 7.6V$$

10. Design a JFET circuit with a voltage divider bias shown in fig. JFET parameters are I_{DSS}=8mA, V_P=-4V. Assume R_1+R_2=200KΩ and R_S=500KΩ. Design to circuit such that the dc drain current is I_D=4mA and the dc drain to source voltage is V_{DS}=5V.



Solution:

Assume the JFET is biased in the saturation region

Step 1: Determine the V_{GS}

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$4 = 8\left(1 - \frac{V_{GS}}{(-4)}\right)^2$$

$$V_{GS} = -1.17V$$

Step 2: Calculate V_S and V_G

$$V_S = I_D R_S = 4 \times 10^{-3} \times 500 = 2V$$

$$V_G = V_{GS} + V_S = -1.17 + 2 = 0.83V$$

Step 3: Calculate R_1 and R_2

$$V_G = \frac{R_2}{R_1 + R_2} V_{DD}$$

$$0.83 = \frac{R_2}{200 \times 10^3} \times 10$$

$$R_2 = 16.6K\Omega$$

$$R_1 = 200K - 16.6K = 183.4K\Omega$$

Step 4: Calculate R_D

$$V_{DS} = V_{DD} - I_D R_D - I_D R_S$$

$$R_D = \frac{V_{DD} - V_{DS} - I_D R_S}{I_D} = \frac{10 - 5 - (4 \times 0.5)}{4} = 750K\Omega$$

Step 5: Check assumption

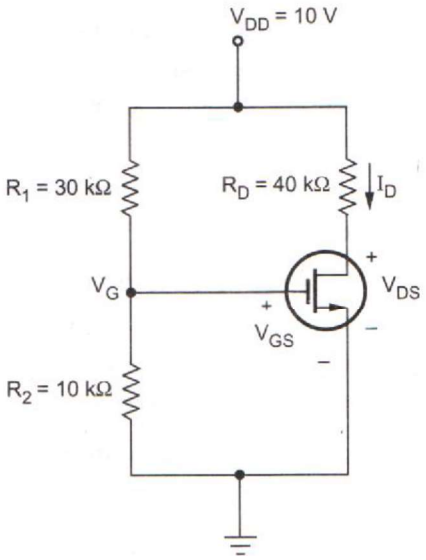
To confirm that JFET is biased in the saturation region

$$V_{DS} > V_{GS} - V_P$$

$$V_{DS} = 5V > V_{GS} - V_P = -1.17 - (-4) = 2.83V$$

This shows that the JFET is indeed biased in the saturation region, as initially assumed.

11. For the circuit shown in fig, assume that R_1=30KΩ, R_2=10KΩ, R_D=40KΩ, V_{DD}=10V, V_T=1V, V_{GS}=2V and K=0.1mA/V^2. Find I_D and V_{DS}.



Solution:

Step 1: Calculate V_G

From the circuit shown in fig and equation we have,

$$V_G = V_{GS} = \frac{R_2}{R_1 + R_2} V_{DD}$$

$$= \left(\frac{10}{10 + 30}\right)(10) = 2.5V$$

Step 2: Calculate I_D

Assuming the MOSFET is biased in the saturation region, the drain current is,

$$I_D = K_n(V_{GS} - V_T)^2 = (0.1)(2 - 1)^2 = 0.1mA$$

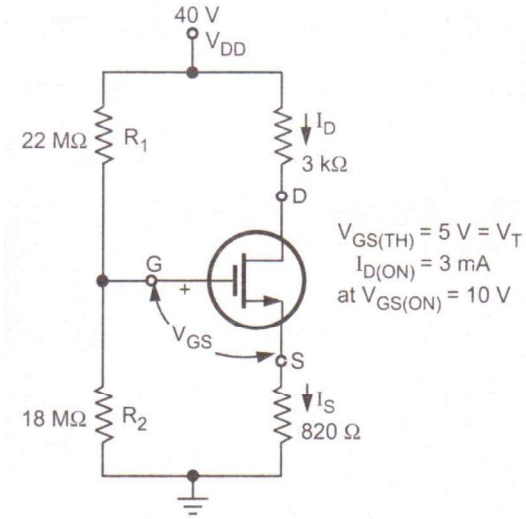
Step 3: Calculate V_{DS}

$$V_{DS} = V_{DD} - I_D R_D = 10 - (0.1)(40) = 6V$$

Validity of assumption:

Since $V_{DS} = 6V > V_{DS\,sat} = V_{GS} - V_T = 2 - 1 = 1V$, the MOSFET is indeed biased in the saturation region and our calculations are correct.

12. For the circuit shown in fig. Calculate V_G, I_D, V_{GS} and V_{DS}.



Solution:

Step 1: Calculate V_G

$$V_G = \frac{V_{DD}\,R_2}{R_1 + R_2} = \frac{40 \times 18}{18 + 22} = 18V$$

Step 2: Obtain expression for V_{GS}

$$V_{GS} = V_G - I_D R_S = 18 - I_D R_S$$
$$= 18 - 820\, I_D$$

Step 3: Calculate K_n

$$Kn = \frac{I_{D(ON)}}{(V_{GS(ON)} - V_{GS(TH)})^2} = \frac{3 \times 10^{-3}}{(10-5)}2 = 0.12 \times 10^{-3} A/V^2$$

Step 4: Obtain the value of I_{DQ}

Assuming that the gate to source voltage is greater than V_T and transistor is biased in the saturation region.

We have, $I_D = K_n(V_{GS} - V_T)^2$

Substituting value of V_{GS} we get, $I_D = 0.12 \times 10^{-3}(18 - 820I_D - 5)^2$

$$I_D = 0.02028 - 2.5584\, I_D + 80.688 I_D^{\,2}$$

$$80.688 I_D^{\,2} - 3.5584 I_D + 0.02028 = 0$$

Solving quadratic equation using formula

$$\frac{-b \pm \sqrt{b^2 - 4ac}}{2a}$$

we get,

$$= \frac{-(-3.5584) \pm \sqrt{(-3.5584)^2 - 4(80.688)(0.02028)}}{2(80.688)} = 37.38\text{mA or}6.725\text{mA}$$

If we calculate value of V_{DS} taking I_D =37.38mA we get,

$$V_{DS} = V_{DD} - I_D(R_D + R_S) = 40 - 37.38 \times 10^{-3}(3 \times 10^3 + 820)$$

$$= -102.8\text{V}$$

For $I_D = 6.725\text{mA}$, $V_{DS} = 40 - 6.725 \times 10^{-3}(3 \times 10^3 + 820)$

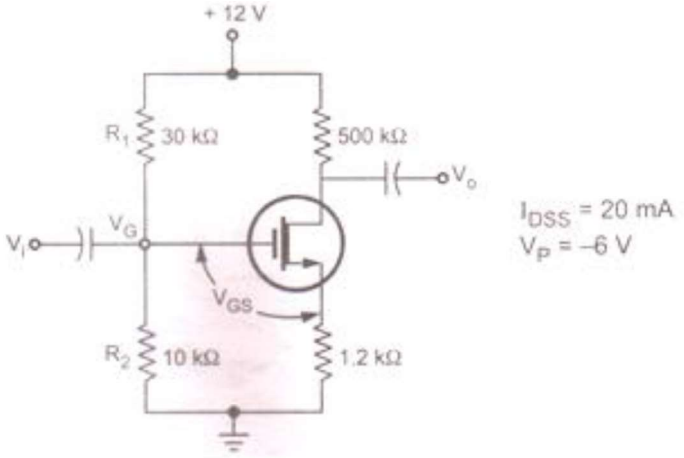
$$= 14.31\text{V}$$

Because $V_{DS} = 14.31\text{V} > V_{DS\,(sat)} = V_{GS} - VT = 10 - 5 = 5\text{V}$, the transistor is indeed biased in the saturation region and our calculation are valid with,

$$V_{DS} = 14.31\text{V and hence valid } I_D = 6.725\text{mA}$$

$$V_{GS} = V_G - I_D R_S = 18 - 6.725 \times 10^{-3}(820) = 12.4855\text{V}$$

13. For the circuit shown in fig. Calculate I_D, V_{DS}, V_G and V_S.



Solution:

$$V_G = \frac{V_{DD} R_2}{R_1 + R_2} = \frac{12 \times 10}{10 + 30} = 3\text{V}$$

Applying KVL to the input circuit we get,

$$V_G - V_{GS} - V_S = 0$$

$$V_{GS} = V_G - V_S$$

$$= 3 - I_S R_S \qquad \because V_S = I_S R_S$$

$$= 3 - I_D R_S \qquad \because I_D = I_S$$

We have,

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

Substituting value of V_{GS} in above equation we get,

$$I_D = I_{DSS}\left(1 - \frac{(3 - I_D R_S)}{V_P}\right)^2$$

$$= 20 \times 10^{-3}\left(1 - \frac{(3 - I_D \times 1.2 \times 10^3)}{-6}\right)^2$$

$$= 20 \times 10^{-3}(1 - [(-0.5) + 200I_D])^2$$

$$= 20 \times 10^{-3}(1.5 - 200I_D)^2$$

$$= 20 \times 10^{-3}(2.25 - 600I_D + 40000I_D^2)$$

$$I_D = 0.045 - 12I_D + 800I_D^2$$

$$800I_D^2 - 13I_D + 0.045 = 0$$

Solving quadratic equation using formula

$$\frac{-b \pm \sqrt{b^2 - 4ac}}{2a}$$

we get,

$$= \frac{-(-13) \pm \sqrt{(13)^2 - 4(800)(0.045)}}{2(800)}$$

$$= \frac{13 \pm \sqrt{169 - 144}}{1600}$$

$$= \frac{13 \pm \sqrt{25}}{1600} = \frac{13 \pm 5}{1600} = 5\text{mA or } 11.25\text{mA}$$

If we calculate value of V_{DS} taking I_D =11.25mA we get,

$$V_{DS} = V_{DD} - I_D(R_D + R_S) = 12 - 11.25 \times 10^{-3}(500 + 1.2 \times 10^3)$$

$$= 12 - 19.125 = -7.125$$

Practically, the value of V_{DS} must be positive, hence I_D=11.25mA is invalid.

Now calculating value of V_{DS} taking I_D=5mA,

$$V_{DS} = V_{DD} - I_D(R_D + R_S) = 12 - 5 \times 10^{-3}(500 + 1.2 \times 10^3)$$

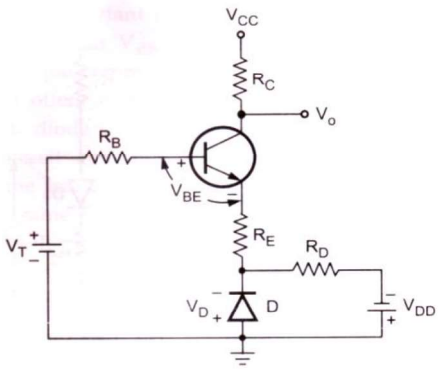
$$= 12 - 8.5 = 3.5\text{V}$$

$$V_{GS} = 3 - I_D R_S = 3 - 5 \times 10^{-3} \times 1.2 \times 10^{-3} = 3 - 6 = -3\text{V}$$

$$V_S = I_D R_S = 5 \times 10^{-3} \times 1.2 \times 10^{-3} = 6\text{V}$$

TWO MARK QUESTIONS AND ANSWERS

1. Give the circuit that offers stabilization of operating point by means of self bias & diode compensation technique.



2. What is thermal runaway?

The increase in collector current increases the power dissipated at the collector junction. This in turn further increases the temperature of the junction and hence increase in collector current. The process is cumulative and referred as self heating. The excess heat produced at the collector base junction may even burn and destroy the transistor. This situation is called Thermal Runaway of transistors.