UNIT V

IC MOSFET Amplifiers

5.1. IC Biasing:

1. An integrated circuit designs biasing circuits use constant current sources.

2. The constant dc ct called reference current is generated at one location & is then replicated at various stages of amplifier present in the circuit .The process is known as current steering.

5.1.1. Advantages of current steering process:

1. The external components such as precision resistors required to generate a predictable & stable reference current , need not be repeated for every amplifier stage.

2. The bias currents of the various stages track each other when there is any change due to power supply voltage or temperature.

5.2. MOSFET current sources

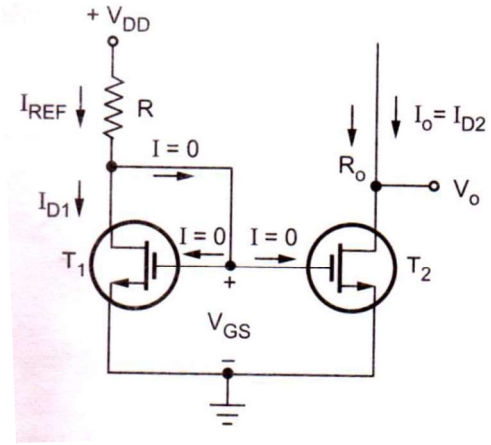

Fig 5.1. MOSFET current source using MOSFET

It uses two MOSFETs T_1& T_2. Since the drain & gate of MOSFET T1 is shorted, it is operated in saturation it is operated in saturation region.

$$I_{REF} = I_{D1} \quad \ldots\ldots\ldots\ldots (1)$$

$$I_{D1} = \frac{1}{2} K'_{n1} \left(\frac{W_1}{L_1}\right) (V_{GS} - V_{T1})^2 \quad \ldots\ldots\ldots\ldots\ldots (2)$$

$$I_{REF} = K_{n1} (V_{GS} - V_{T1})^2 \quad \ldots\ldots\ldots\ldots (3)$$

$$\frac{I_{REF}}{K_{n1}} = (V_{GS} - V_{T1})^2$$

Taking square root on both sides,

$$\sqrt{\frac{I_{REF}}{K_{n1}}} = (V_{GS} - V_{T1})$$

$$V_{GS} = V_{T1} + \sqrt{\frac{I_{REF}}{K_{n1}}} \quad \ldots\ldots\ldots\ldots (4)$$

From the fig,

$$I_{REF} - I_{D1} = \frac{V_{DD} - V_{GS}}{R} \quad \ldots\ldots\ldots\ldots\ldots (5)$$

where, I_{REF} is a reference current of the current of the current source.

The MOSFET T_2 has the same V_{GS} as T_1.It is also operating in the saturation region.

$$I_0 = I_{D2} = \frac{1}{2} K'_{n1} \left(\frac{W_2}{L_2}\right) (V_{GS} - V_{T2})^2 \ldots\ldots\ldots\ldots (6)$$

$$I_o = K_{n2} (V_{GS} - V_{T2})^2 \ldots\ldots\ldots\ldots (7)$$

Since $V_{GS1}=V_{GS2}$ & Sub (4) in (7),

$$I_o = K_{n2} \left(V_{T1} + \sqrt{\frac{I_{REF}}{K_{n1}}} - V_{T2}\right)^2 \ldots\ldots\ldots\ldots\ldots (8)$$

$$\frac{(6)}{(2)} \Rightarrow \frac{I_0}{I_{REF}} = \frac{I_{D2}}{I_{D1}} = \frac{(W_2/L_2)}{(W_1/L_1)} \ldots\ldots\ldots\ldots (9)$$

For identical MOSFETs, $(W_2/L_2) = (W_1/L_1)$ & hence, $I_0=I_{REF}$. For this reason, when two MOSFETs are identical, the circuit is known as MOSFET current mirror circuit.

5.2.1. Effect of V_o & I_0:

1. To ensure that, T_2 is operated in saturation,

$$V_o \geq V_{GS} - V_T \ldots\ldots\ldots\ldots (10)$$

$$V_o \geq V_{ov} \ldots\ldots\ldots\ldots\ldots (11)$$

Where, V_{ov} is the override voltage,

$$V_{ov} = V_{GS} - V_T \quad \ldots\ldots\ldots\ldots\ldots (12)$$

2. For identical MOSFETs, $I_O = I_{REF}$ & $V_o = V_{GS}$. As V_O increases above this value, I_O also increases according to the incremental output resistance r_{o2} of T_2. It is given by,

$$R_0 = r_{o2} = \frac{\Delta V_{DS\,2}}{\Delta I_0} = \frac{\Delta V_0}{\Delta I_0} = \frac{V_{A2}}{I_O} = \frac{1}{\lambda_2 I_O} \quad \ldots\ldots\ldots\ldots (13)$$

Where, V_{A2} is the early voltage of T_2

λ is the channel length modulation

$$\lambda = \frac{1}{V_A} \quad \ldots\ldots\ldots\ldots (14)$$

3. For ideal current source $R_o \rightarrow \infty$. The output current of current source circuit is given by ,

$$I_o = \frac{(W_2/L_2)}{(W_1/L_1)} I_{REF} \left(1 + \frac{V_0 - V_{GS}}{V_{A2}}\right) \quad \ldots\ldots\ldots\ldots (15)$$

5.2.2. Replacing R by another MOSFET:

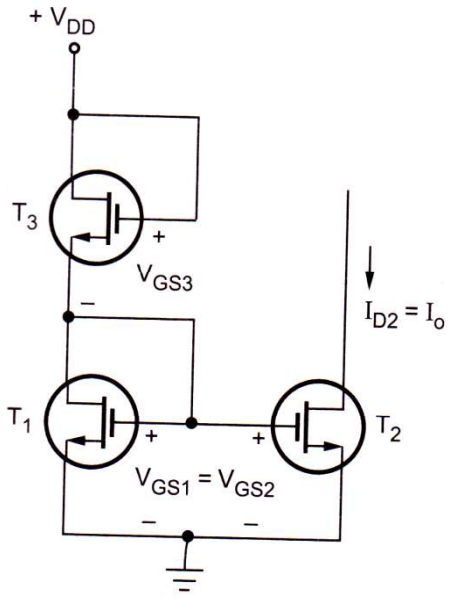

Fig 5.2. MOSFET constant current source

Since T_1 & T_3 are connected in series $I_{D1}=I_{D3}$. Neglecting channel length modulation ($\lambda=0$) we can write,

$$K_{n1}(v_{GS}-v_{T1})^2=K_{n3}(V_{GS}-V_{T3})^2 \quad \ldots\ldots\ldots\ldots (16)$$

From the circuit,

$$V_{DD}=V_{GS1}+V_{GS3} \quad \ldots\ldots\ldots\ldots\ldots (17)$$

$$I_o=\frac{K_n'}{2}\left(\frac{W_2}{L_2}\right)(V_{GS}-V_T)^2 \quad \ldots\ldots\ldots\ldots\ldots (18)$$

5.3. MOSFET current source circuit – cascode current mirror:

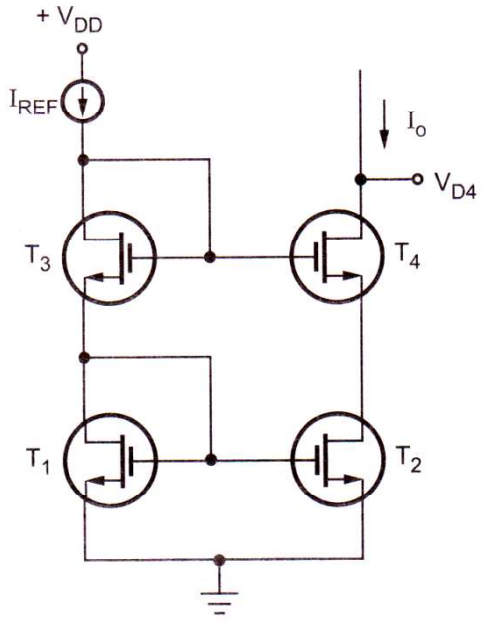

Fig 5.3. MOSFET cascode current mirror circuit

MOSFETs T_3&T_4 are included to provide higher output resistance. This circuit is known as cascade current mirror circuit.

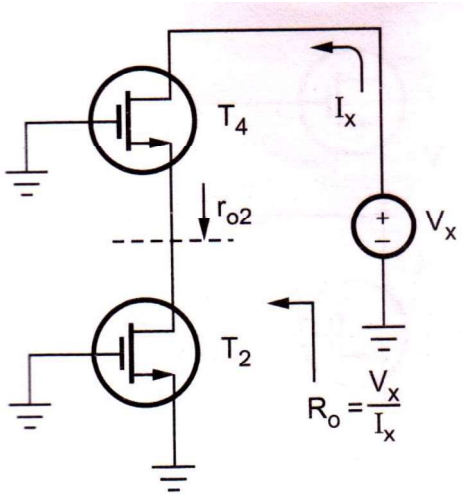

Fig 5.4. Equivalent circuit

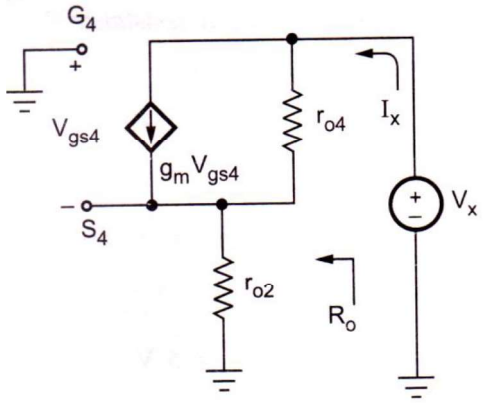

Fig 5.5. Small signal equivalent circuit

Appling KCL to the output node,

$$I_x = -g_m V_{gs4} + \frac{V_x + V_{gs4}}{r_{D4}} \quad \ldots\ldots\ldots\ldots\ldots (1)$$

$$V_{gs4} = -I_x r_{o2} \quad \ldots\ldots\ldots\ldots (2)$$

Sub (2) in (1),

$$I_x = -g_m I_x r_{o2} + \frac{V_x}{r_{o4}} - \frac{I_x r_{o2}}{r_{o4}}$$

$$I_x + g_m I_x r_{o2} + \frac{I_x r_{o2}}{r_{o2}} = \frac{V_x}{r_{o4}}$$

$$I_x \left(1 + g_m r_{o2} + \frac{r_{o2}}{r_{o4}}\right) = \frac{V_x}{r_{o4}}$$

$$R_o = \frac{V_x}{I_x} = r_{o4}\left(1 + g_m r_{o2} + \frac{r_{o2}}{r_{o4}}\right)$$

$$= r_{o4} + g_m r_{o2} r_{o4} + r_{o2}$$

$$= r_{o4} + (1 + g_m r_{o4}) r_{o2}$$

Since $g_m r_{o2} \gg 1$, the output resistance of the cascode current mirror is much greater than basic two MOSFET current source.

5.4. Wilson current mirror:

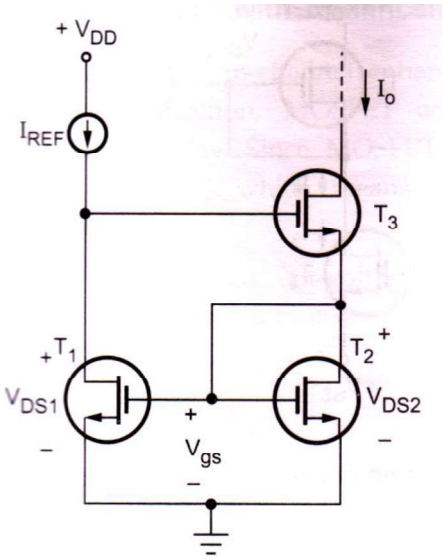

Fig 5.6. MOSFET Wilson current mirror

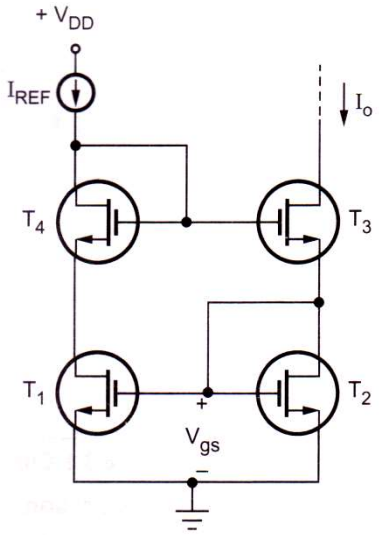

Fig 5.7. Modified MOSFET Wilson current mirror

1. In MOSFET Wilson current source the V_{DS} value of T_1&$T_2$are not equal. Since λ is not zero, the ratio I_O is slightly different from the aspect ratio

2. The modified MOSFET Wilson current circuit solves this problem by including T_4.

3. The advantages of these circuits is the increase in output resistance & hence to increase the stability of output current.

5.5. MOSFET current steering circuit:

1. The constant current source can be replicated to provide dc bias current for the various amplifier stages.

2. T_1 together with R determines the reference current Ierf& transistors T_1, T_2&T_3 from a two output current mirror.

$$\frac{I_2}{I_{REF}} = \frac{(W_2/L_2)}{(W_1/L_1)} \quad \ldots\ldots\ldots (1)$$

$$I_2 = I_{REF}\frac{(W_2/L_2)}{(W_1/L_1)} \quad \ldots\ldots\ldots (2)$$

$$I_3 = I_{REF}\frac{(W_2/L_2)}{(W_1/L_{1)}} \ldots\ldots\ldots (3)$$

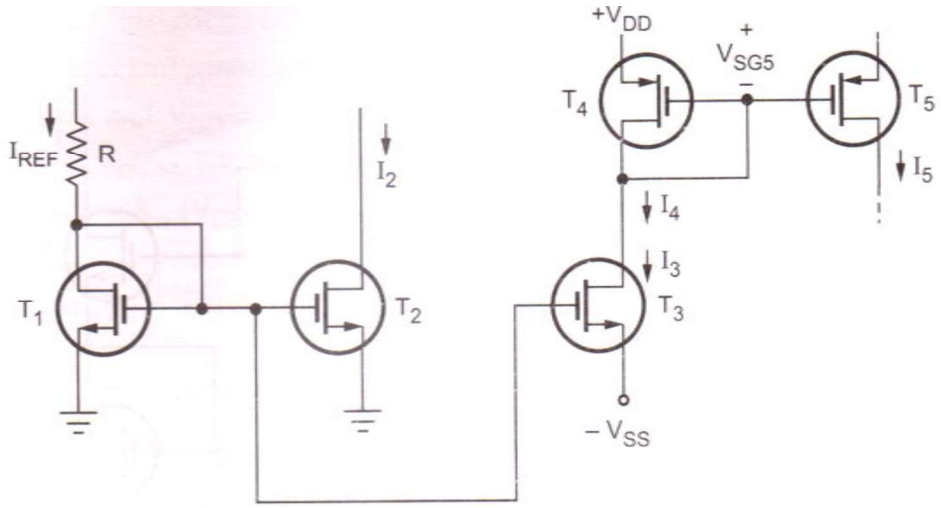

Fig 5.7. Current steering circuit

For T_2 & T_3 to operate in saturation.

$$V_{D2}, V_{D3} \geq -V_{SS} + V_{GS1} - V_T$$

$$V_{D2}, V_{D3} \geq -V_{SS} + V_{OV1}$$

$$I_5 = I_4\frac{(W_S/L_S)}{(W_4/L_4)}$$

Where I_4=I_3 & to keep T_5 in saturation,

$$V_{D5} \leq V_{DD} - |V_{OV5}|$$

5.6. Amplifiers with active load:

When MOSFET itself is used as a load device, it is referred to as active load. There are three types of load device,

1. n-channel enhancement mode device
2. n-channel depletion mode device
3. p-channel enhancement mode device.

5.6.1. NMOS amplifier with enhancement load:

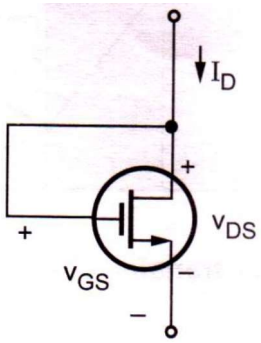

Fig 5.8. N-channel enhancement mode MOSFET with gate & drain shorted

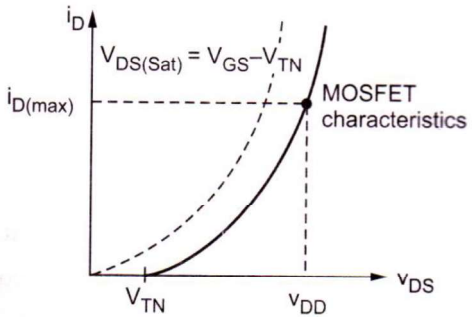

Fig 5.9. Current-Voltage characteristics for n-channel enhancement load device

In this connection, MOSFET acts as a non-linear resistor& is called enhancement load device.

$$V_{ov} = V_{DS(sat)} = V_{GS} - V_T$$

$$I_D = K_n(V_{GS} - V_T)^2$$

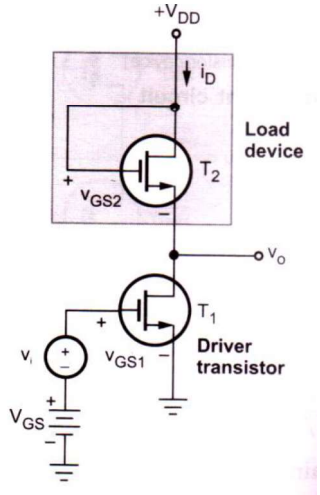

Fig 5.10. NMOS amplifier with enhancement load device

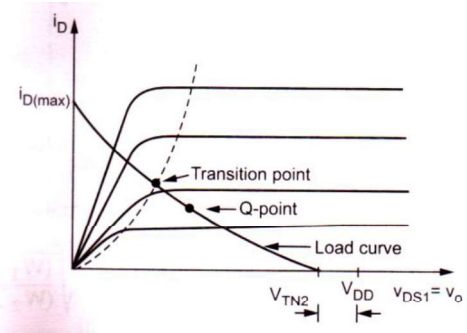

Fig 5.11. V-I characteristics

The enhancement load circuit alone cannot be used as an amplifier, however, if it is connected in a circuit with another MOSFET configuration, the circuit can be used as an amplifier or as an inverter in a digital circuit.

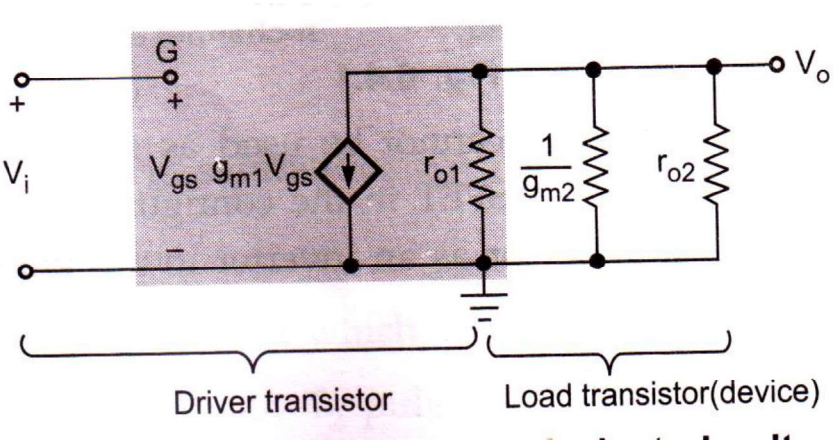

Fig 5.12. Small-signal equivalent circuit

$$R_0 = \frac{1}{g_{m1}} \| r_{o2}$$

$$V_o = -g_{m1} V_{gs} (r_{o1} \| R_0) \qquad \because V_i = V_{gs}$$

$$A_V = \frac{V_o}{V_i} = -\frac{g_{m1} V_{gs} \left(r_{o1} \left\| \frac{1}{g_{m2}} \right\| r_{o2} \right)}{V_{gs}}$$

$$= -g_{m1} (r_{o1} \| \frac{1}{g_{m2}} \| r_{o2})$$

If $\frac{1}{g_{m2}} \ll r_{o2}$ & $\frac{1}{g_{m1}} \ll r_{o1}$,

$$A_V = -\frac{g_{m1}}{g_{m2}} = -\sqrt{\frac{K_{n1}}{K_{n2}}}$$

$$= \sqrt{\frac{W_1/L_1}{W_2/L_2}}$$

$A_V \rightarrow$ Size of the transistor

5.6.2. NMOS amplifier with depletion load:

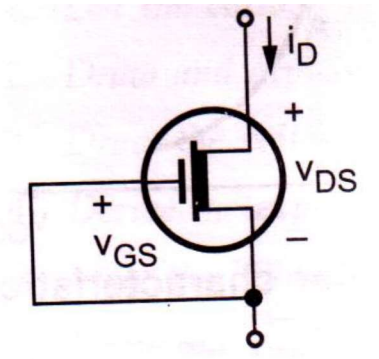

Fig 5.13. NMOS depletion mode device

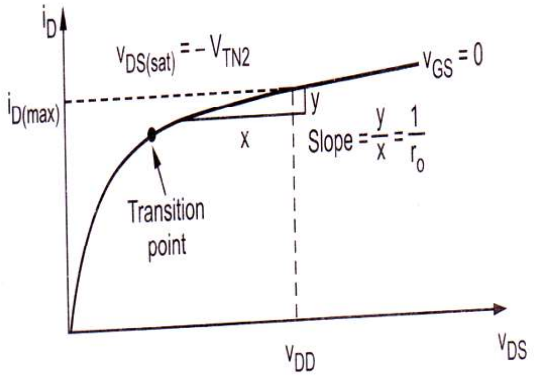

Fig 5.14. Current-Voltage characteristics

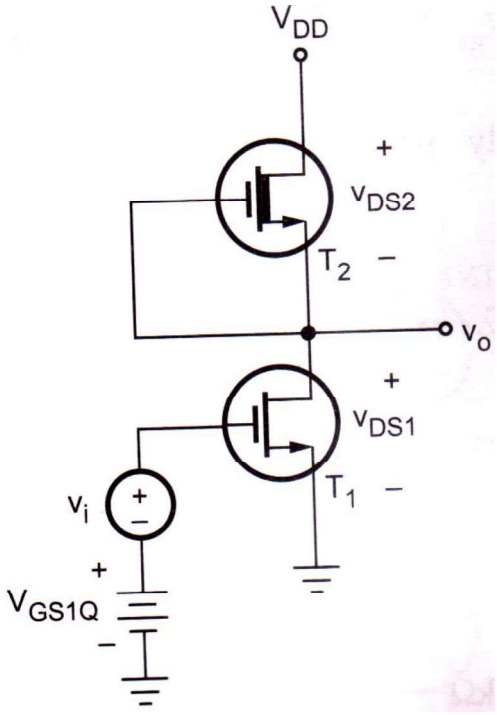

Fig 5.15. NMOS amplifier with depletion load device

Since the gate to source voltage for depletion load (T_2) is zero, $g_m V_{gs2} = 0$.

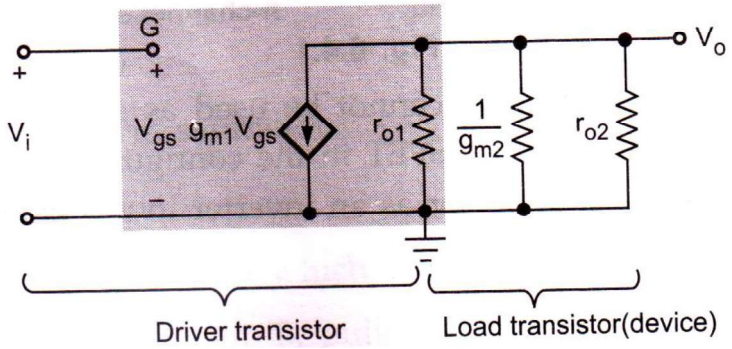

Fig 5.16. Small-signal equivalent circuit of NMOS inverter with depletion load device

$$V_o = -g_{m1}V_{gs}(r_{o1} \| r_{o2})$$

$$V_1 = V_{gs}$$

$$A_V = \frac{V_O}{V_i} = -g_{m1}(r_{o1} \| r_{o2})$$

$A_{V\rightarrow}$ output resistance of the two transistors.

5.7. CMOS CS amplifier:

n–channel enhancement mode MOSFET (T1) is used as a driver and a p-channel enhancement mode MOSFET(T2) is used an active load.

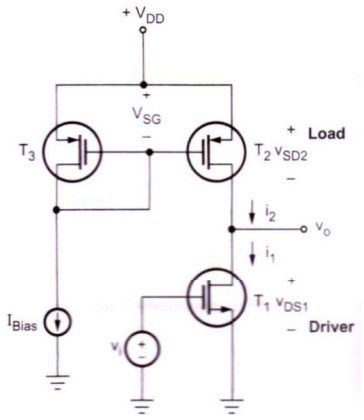

Fig 5.17. CMOS CS amplifier

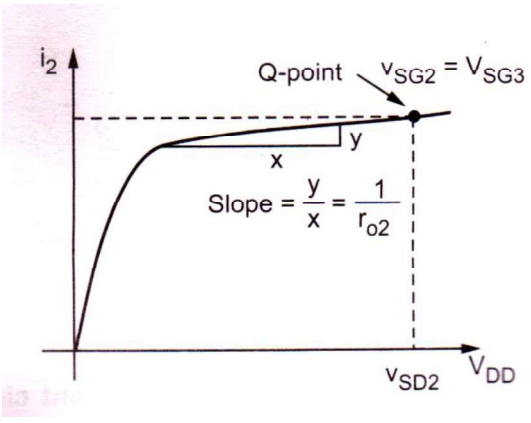

Fig 5.18. PMOS active load I-V characteristics

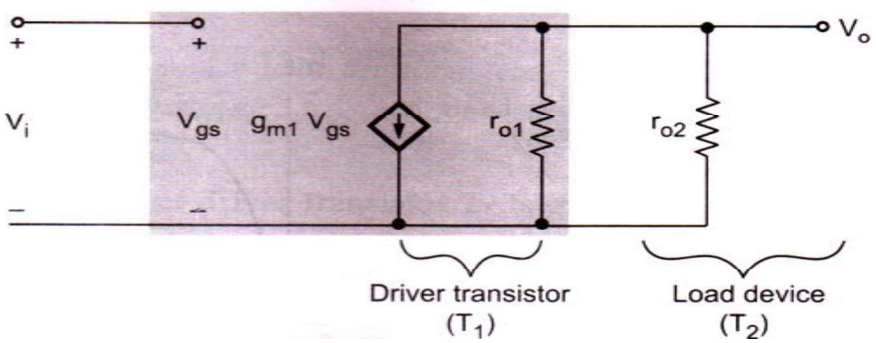

Fig 5.19. Small-signal equivalent circuit for the CMOS CS amplifier

$$V_O = -g_{m1} V_{gs} (r_{o1} \| r_{o2})$$

$$A_V = \frac{V_O}{V_i} = -\frac{g_{m1} V_{gs} (r_{o1} \| r_{o2})}{V_{gs}} \quad \because V_i = V_{gs}$$

$$= -g_{m1} (r_{o1} \| r_{o2})$$

Advantages:

1. CMOS common-source amplifier provides large small signal voltage gain.
2. CMOS amplifier does not suffer from body effect.

5.8. NMOS source follower amplifier:

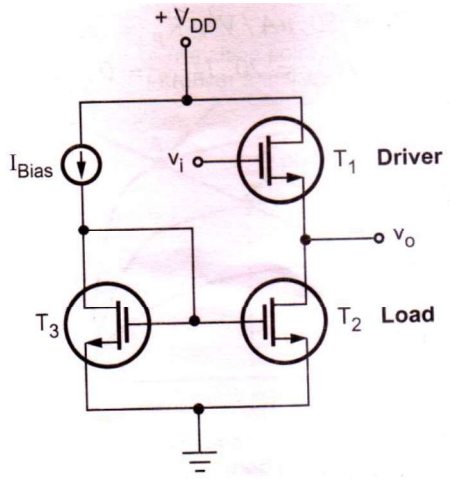

Fig 5.20. NMOS source follower amplifier

The active load is T_2 and driver is n-channel T_1. Input signal is applied to the gate of T_1 and output is at the source of T_1. T_3 & I_{Bias} provides bias for the load device.

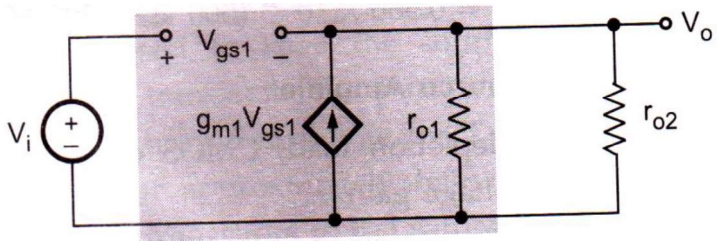

Fig 5.21. Small-signal equivalent circuit for NMOS source follower amplifier

$$V_O = g_{m1}V_{gs1}(r_{o1}\|r_{o2})$$

Apply KVL to the outer loop,

$$V_i = V_{gs1} + V_o$$

$$V_i = V_{gs1} + g_{m1}V_{gs1}(r_{o1}\|r_{o2})$$

$$V_i = V_{gs1}(1 + g_{m1}(r_{o1}\|r_{o2}))$$

$$V_{gs1} = \frac{V_i}{[1+g_{m1}(r_{o1}\|r_{o2})]}$$

Sub V_{gs1} in V_o eqn,

$$V_0 = \frac{g_{m1}V_i(r_{o1}\|r_{o2})}{1 + g_{m1}(r_{o1}\|r_{o2})}$$

$$A_v = \frac{V_0}{V_i} = \frac{g_{m1}(r_{o1}\|r_{o2})}{1 + g_{m1}(r_{o1}\|r_{o2})}$$

5.8.1. Output Resistance:

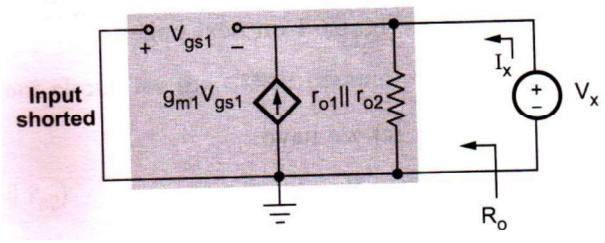

Fig 5.22. Small-signal equivalent circuit to obtain R_o

Apply KCL to the output node,

$$I_x + g_{m1}V_{gs1} = \frac{V_x}{(r_{o1}\|r_{o2})}$$

$$V_{gs1} = -V_x$$

$$I_x - g_{m1}V_x = \frac{V_x}{r_{o1}\|r_{o2}}$$

$$I_x = V_x\left[g_{m1} + \frac{1}{\frac{1}{\frac{1}{r_{o1}}+\frac{1}{r_{o2}}}}\right]$$

$$= V_x[g_{m1} + \frac{1}{r_{o1}} + \frac{1}{r_{o2}}]$$

$$R_o = \frac{V_x}{I_x} = \frac{1}{\frac{1}{1/g_{m1}} + \frac{1}{r_{o1}} + \frac{1}{r_{o2}}}$$

$$R_o = \frac{1}{g_{m1}} + r_{o1}\|r_{o2}$$

5.9. CMOS differential amplifier:

In a differential amplifier the output signal is amplified version of the difference of two inputs of the amplifier.

The CMOS differential amplifier in which a current mirror circuit is employed as an active load for the source coupled pair. Here, transistors T_1 and T_2 are n-channel devices and forms the differential pair biased with I_Q. The load circuit consists of transistors T_3 & T_4, both p-channel devices.

Here, (T_1,T_2) & also (T_3,T_4) are mutually identical with each other thus the tail current I_Q is equally divided between T_1(T_3) & T_2(T_4).

$$i_{D1} = i_{D2} = \frac{I_Q}{2} \text{ …….. (1)}$$

Since gate currents are zero, $i_{D1} = i_{D3}$ & $i_{D2} = i_{D4}$…….(2)

When small differential-mode input voltage, $V_d = V_1 - V_2$ ……..(3)

$$i_{D1} = \frac{I_Q}{2} + i_d = i_{D3} \text{ …….. (4)}$$

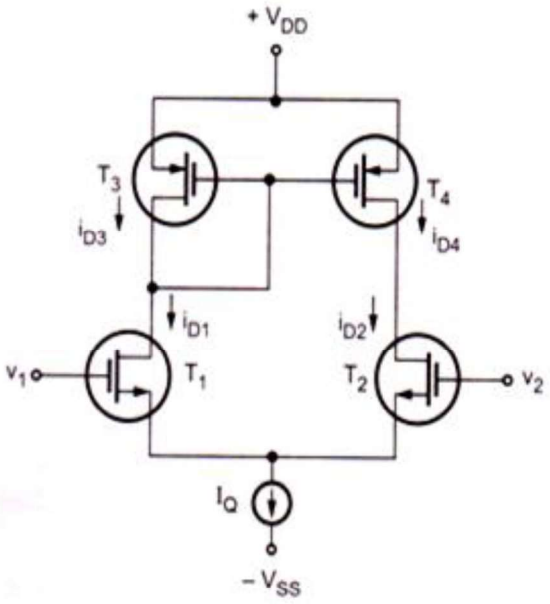

Fig 5.23. CMOS differential amplifier with active load

$$i_{D2} = \frac{I_Q}{2} - i_d = i_{D4} \quad \ldots\ldots\ldots\ldots\ldots (5)$$

Where $i_d \rightarrow$signal current

$$i_d = \frac{g_m V_d}{2} \quad \ldots\ldots\ldots\ldots (6)$$

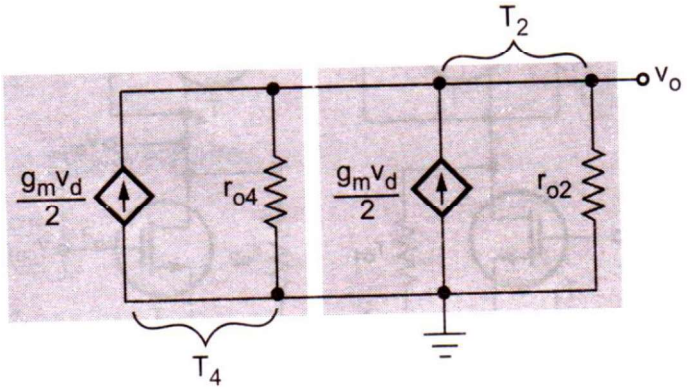

Fig 5.24. Small signal equivalent circuit at drain node of T_2 & T_4

5.9.1. Differential gain (A_d):

$$V_d = \left(\frac{g_m V_d}{2} + \frac{g_m V_d}{2}\right)(r_{o2} \| r_{o4}) \text{ ..... (7)}$$

$$A_d = \frac{V_o}{V_d} = g_m (r_{o2} \| r_{o4}) \text{ ..... (8)}$$

$$= g_m \times \frac{1}{\frac{1}{r_{o2}} + \frac{1}{r_{o4}}} = \frac{g_m}{g_{o2} + g_{o4}} \text{ ..... (9)}$$

Where, $g_m = 2\sqrt{K_n I_D}$

$$= 2\sqrt{K_n \times \frac{I_Q}{2}} \qquad \because I_Q = \frac{I_D}{2}$$

$$= \sqrt{4K_n \frac{I_Q}{2}}$$

$$= \sqrt{2K_n I_Q} \text{ ..... (10)}$$

$$g_{o2} = \lambda_2 I_{DQ2} = \lambda_2 \frac{I_Q}{2} \text{ ..... (11)} \qquad \because \lambda = \frac{1}{vA}$$

$$g_{o4} = \lambda_4 I_{DQ4} = \lambda_4 \frac{I_Q}{2} \text{ ..... (12)}$$

Sub (10), (11) & (12) in (9)

$$A_d = \frac{\sqrt{2K_n I_Q}}{\frac{\lambda_2 I_Q}{2} + \frac{\lambda_4 I_Q}{2}} = \frac{\sqrt{2K_n I_Q}}{\frac{I_Q}{2}[\lambda_2 + \lambda_4]}$$

$$A_d = 2\sqrt{\frac{2K_n}{I_Q}} \times \frac{1}{\lambda_2 + \lambda_4} \text{ ..... (13)}$$

5.9.2. Common mode gain (A_{cm}):

$$i_1 = i_2 = \frac{V_{cm}}{2R_{ss}} \text{ ..... (14)}$$

The output resistance of each T_1&T_2,

$$R_{o1} = R_{o2} = r_o + 2R_{SS} + 2g_m r_o R_{SS} \text{ ..... (15)}$$

$$r_{o1} = r_{o2} = r_o \& g_{m1} = g_{m2} = g_m$$

$$V_{g3} = -i_1 \left(\frac{1}{g_{m3}} \| r_{o3}\right)$$

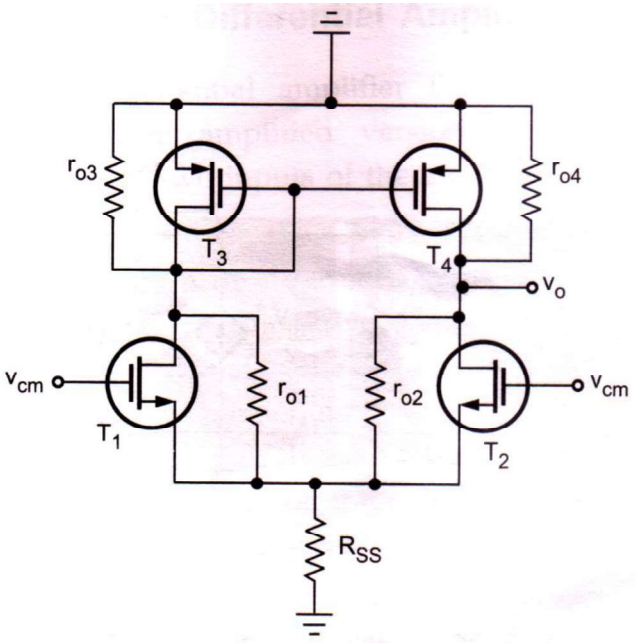

Fig 5.25. Determining common-mode gain

$$i_4 = -g_{m4}V_{g3}$$

$$= i_1 g_{m4}\left(\frac{1}{g_{m3}} \| r_{o3}\right)$$

$$V_o = (i_4 - i_2)r_{o4}$$

Substituting value of i_4,

$$V_o = \left[i_1 g_{m4}\left(\frac{1}{g_{m3}} \| r_{o3}\right) - i_2\right] r_{o4}$$

Substituting values of $i_1 = i_2 = \frac{V_{cm}}{2R_{SS}}$ & $setting\ g_{m3} = g_{m4}$,

$$V_o = \left[\frac{V_{cm}}{2R_{SS}} g_{m3}\left(\frac{1}{g_{m3}} \| r_{o3}\right) - \frac{V_{cm}}{2R_{SS}}\right] r_{o4}$$

$$= \frac{V_{cm}}{2R_{SS}} r_{o4} \left[g_{m3} \left(\frac{\frac{r_{o3}}{g_{m3}}}{\frac{1}{g_{m3}} + r_{o3}} \right) - 1 \right]$$

$$= \frac{V_{cm}}{2R_{SS}} r_{o4} \left[g_{m3} \left(\frac{\frac{r_{o3}}{g_{m3}}}{\frac{1+g_{m3}r_{o3}}{g_{m3}}} \right) - 1 \right]$$

$$= \frac{V_{cm}}{2R_{SS}} r_{o4} \left[g_{m3} \left(\frac{r_{o3}}{1 + g_{m3}r_{o3}} \right) - 1 \right]$$

$$V_o = \frac{V_{cm} r_{O4}}{2R_{SS}} \left[\frac{g_{m3}r_{o3}}{1 + g_{m3}r_{o3}} - 1 \right]$$

$$\frac{V_o}{V_{cm}} = \frac{r_{o4}}{2R_{SS}} \left[\frac{g_{m3}r_{o3} - 1 - g_{m3}r_{o3}}{1 + g_{m3}r_{o3}} \right]$$

$$\frac{V_o}{V_{cm}} = A_{cm} = -\frac{1}{2R_{SS}} \times \frac{r_{o4}}{g_{m3}r_{o3} + 1}$$

If $r_{o3}g_{m3} \gg 1$ & $r_{o3} = r_{o4}$,

$$A_{cm} = -\frac{1}{2R_{SS}} \times \frac{1}{g_{m3}} = -\frac{1}{2R_{SS}g_{m3}}$$

5.9.3. CMRR:

$$CMRR = \left| \frac{A_d}{A_{cm}} \right|$$

$$= \frac{g_m (r_{o2} \| r_{o4})}{\frac{1}{2R_{SS}g_{m3}}}$$

$$= (r_{o2} \| r_{o4}) g_m g_{m3} 2R_{SS}$$

If $r_{o2} = r_{o4} = r_o$ & $g_m = g_{m3}$,

$$CMRR = \left| \frac{A_d}{A_{cm}} \right| = (g_m r_o)(g_m R_{SS})$$

SOLVED EXAMPLES:

1.Design the MOSFET current source circuit for following specifications: V_{DD}=4V, I_{REF}=120µA ,L_1=L_2=1µm, W_1=W_2=10µm,V_T=0.7V and K'_n=200µA/V^2. Find the value of R, calculate the lowest possible value of V_o, and calculate r_{o2} if early voltage V'_{A2}=20V/µm. Also find the change in the output current if change in V_o is +2 V.

Solution:

$$\text{Since } L_1 = L_2 \text{ and } W_1 = W_2 \text{ MOSFETs are idetical and } I_O = I_{REF} = 120\mu A$$

$$I_{D1} = I_{REF} = \frac{1}{2}K'_n\left(\frac{W_1}{L_1}\right)(V_{GS} - V_T)^2$$

$$120 = \frac{1}{2} \times 200 \times 10(V_{GS} - V_T)^2$$

$$(V_{GS} - V_T)^2 = V_{OV}^2 = 0.12$$

$$V_{OV} = 0.3464V$$

$$V_{GS} = V_T + V_{OV} = 0.7 + 0.3464 = 1.0464V$$

$$R = \frac{V_{DD} - V_{GS}}{I_{REF}} = \frac{4 - 1.0464}{120 \times 10^{-6}} = 24.61K\Omega$$

$$V_{omin} = V_{OV} = 0.3464V$$

$$V_{A2}=V'_{A2} \times L_2 = 20 \times 1 = 20V$$

$$r_{o2} = \frac{V_{A2}}{I_0} = \frac{20}{120\mu A} = 166.67k\Omega$$

$$\Delta I_O = \frac{\Delta V_o}{r_{o2}} = \frac{2V}{166.67K\Omega} = 12\mu A$$

2. For NMOS amplifier with depletion load, V_{TN1}=0.8V, $V_{TN2} = -1.0$ V, $K_{n1} = 2mA/V^2$, $K_{n2} = 0.2mA/V^2$, $I_{DQ} = 0.2mA$ and$\lambda_1 = \lambda_2 = 0.01V^{-1}$. calculate the small- signal voltage gain.

Solution:

Transconductance of driver transistor T_1 is given by

$$g_{m1} = 2\sqrt{K_{n1}I_{DQ}} = 2\sqrt{(2 \times 10^{-3})(0.2 \times 10^{-3})} = 1.265mA/V$$

Since $\lambda_1 = \lambda_2$, the output resistances are

$$r_{o1} = r_{o2} = \frac{1}{\lambda I_{DQ}} = \frac{1}{(0.01)(0.2 \times 10^{-3})} = 500K\Omega$$

$$A_v = -g_{m1}(r_{o1} \| r_{o2}) = -1.265 \times 10^{-3}(500k\Omega \| 500k\Omega) = -316.25$$

TWO MARK QUESTIONS AND ANSWERS

1. Define current steering.

In integrated circuit designs biasing circuits use constant current sources.T he constant d.c current called reference current is generated at one location and then replicated at various other locations for biasing the various stages of amplifier present in the circuit. This process is known as current steering.

2. State the advantages of current steering.

1) The external components such as precision resistors required to generate a predictable and stable reference current, need not be repeated for every amplifier stage.

2) The bias currents of the various stages track each other when there is any change due to power supply voltage or temperature.

3. Define override voltage.

Override voltage is denoted as $V_{ov,}$

$$V_{ov} = V_{GS} - V_T$$

$$V_o \geq V_{ov}$$

4. What is meant by Wilson current mirror?

In MOSFET Wilson current source, the V_{DS} values of transistors are not equal. Since λ is not zero, the ratio I_O/I_{REF} is slightly different from aspect ratio. The modified Wilson current mirror solves this problem by including other transistor. The advantage of these circuits is increase in output resistance and hence increase the stability of output current.

5 .List the various types of active loads.

When MOSFET itself is used as a load device,it is referred to as active load.

Three types of load devices are:

1) n-channel enhancement mode device.

2) n-channel depletion mode device.

3) p-channel enhancement mode device.