```
output [3:0] Y;
wireAbar,Bbar;
        not (Abar,A);
        not (Bbar,B);
        and (Y0,Abar,Bbar,En);
        and (Y1,Abar,B,En);
        and (Y2,A,Bbar,En);
        and (Y3,A,B,En);
endmodule
```

Verilog HDL code in structural description of a full adder with two half adder

```
modulefull_add(A,B,Cin,Sum,Cout);
inputA,B,Cin;
outputSum,Cout;
wire S0,C0,C1;
full adder
        HA H1(A,B,S0,C0);
        HA H2(S0,Cin,Sum,C1);
        Or (Cout,C0,C1);
Endmodule
```

5.16Two marks questions with answers

1. **What are secondary variables?**
   Present state variables in asynchronous sequential circuits
2. **What are excitation variables?**
   Next state variables in asynchronous sequential circuits
3. **What is fundamental mode sequential circuit?**
   -input variables changes if the circuit is stable
   -inputs are levels, not pulses
   -only one input can change at a given time
4. **What is pulse mode circuit?**
   -inputs are pulses
   -width of pulses are long for circuit to respond to the input
   -pulse width must not be so long that it is still present after the new state is reached
5. **What are the significance of state assignment?**
   In synchronous circuits-state assignments are made with the objective of circuit Reduction Asynchronous circuits-its objective is to avoid critical races
6. **When does race condition occur?**
   -two or more binary state variables change their value in response to the change in i/p Variable

7. **What is non critical race?**
   -final stable state does not depend on the order in which the state variable changes
   -race condition is not harmful
8. **What is critical race?**
   -final stable state depends on the order in which the state variable changes -race condition is harmful
9. **When does a cycle occur?**
   -asynchronous circuit makes a transition through a series of unstable state
10. **What are the different techniques used in state assignment?**
    -shared row state assignment
    -one hot state assignment
11. **What are the steps for the design of asynchronous sequential circuit?**
    -construction of primitive flow table
    -reduction of flow table
    -state assignment is made
    -realization of primitive flow table
12. **What is hazard?**
    -unwanted switching transients
13. **What is static 1 hazard?**
    -output goes momentarily 0 when it should remain at 1
14. **What are static 0 hazards?**
    -output goes momentarily 1 when it should remain at 0
15. **What is dynamic hazard?**
    -output changes 3 or more times when it changes from 1 to 0 or 0 to 1
16. **What is the cause for essential hazards?**
    -unequal delays along 2 or more path from same input
17. **What is flow table?**
    -state table of an synchronous sequential network
18. **What is SM chart?**
    -describes the behavior of a state machine
    -used in hardware design of digital systems
19. **What are the advantages of SM chart?**
    -easy to understand the operation
    -east to convert to several equivalent forms
20. **What is primitive flow chart?**
    -one stable state per row
21. **What is combinational circuit?**
    Output depends on the given input. It has no storage element.
22. **What is state equivalence theorem?**
    Two states SA and SB, are equivalent if and only if for every possible input X sequence, the outputs are the same and the next states are equivalent i.e., if SA (t + 1) = SB (t + 1) and ZA = ZB then SA = SB.
23. **What do you mean by distinguishing sequences?**

Two states, SA and SB of sequential machine are distinguishable if and only if their exists at least one finite input sequence. Which, when applied to sequential machine causes different output sequences depending on whether SA or SB is the initial state.

24. **Prove that the equivalence partition is unique**
    Consider that there are two equivalence partitions exist: PA and PB, and PA) PB. This states that, there exist 2 states Si &Sj which are in the same block of one partition and not in the same block of the other. If Si &Sj are in different blocks of say PB, there exists at least on input sequence which distinguishes Si &Sj and therefore, they cannot be in the same block of PA.
25. **Define merger graph.**
    The merger graph is defined as follows. It contains the same number of vertices as the state table contains states. A line drawn between the two state vertices indicates each compatible state pair. It two states are incompatible no connecting line is drawn.
26. **Define incompatibility**
    The states are said to be incompatible if no line is drawn in between them. If implied states are incompatible, they are crossed & the corresponding line is ignored
27. **Define closed covering.**
    A Set of compatibles is said to be closed if, for every compatible contained in the set, all its implied compatibles are also contained in the set. A closed set of compatibles, which contains all the states of M, is called a closed covering.
28. **Define machine equivalence.**
    Two machines, M1 and M2 are said to be equivalent if and only if, for every state in M1, there is a corresponding equivalent state in M2 & vice versa.
29. **Define state table**.
    For the design of sequential counters we have to relate present states and next states. The table, which represents the relationship between present states and next states, is called state table.
30. **Define total state.**
    The combination of level signals that appear at the inputs and the outputs of the delays define what is called the total state of the circuit.
31. **What are the steps for the design of asynchronous sequential circuit?**
    Construction of a primitive flow table from the problem statement.
    Primitive flow table is reduced by eliminating redundant states using the state reduction
    State assignment is made
    The primitive flow table is realized using appropriate logic elements.
32. **Define primitive flow table**:
    It is defined as a flow table which has exactly one stable state for each row in the table. The design process begins with the construction of primitive flow table.

33. **What are the types of asynchronous circuits?**
    Fundamental mode circuits
    Pulse mode circuits
34. **Give the comparison between state Assignment Synchronous circuit and state assignment**

In synchronous circuit, the state assignments are made with the objective of circuit reduction. In asynchronous circuits, the objective of state assignment is to avoid critical races.

35. **What are races?**
    When 2 or more binary state variables change their value in response to a change in an input variable, race condition occurs in an asynchronous sequential circuit. In case of unequal delays, a race condition may cause the state variables to change in an unpredictable manner.
36. **Define non critical race.**
    If the final stable state that the circuit reaches does not depend on the order in which the state variable changes, the race condition is not harmful and it is called a non critical race.
37. **Define critical race?**
    If the final stable state depends on the order in which the state variable changes, the race condition is harmful and it is called a critical race.
38. **What is a cycle?**
    A cycle occurs when an asynchronous circuit makes a transition through a series of unstable states. If a cycle does not contain a stable state, the circuit will go from one unstable to stable to another, until the inputs are changed.
39. **List the different techniques used for state assignment**.
    Shared row state assignment
    One hot state assignment.
40. **Write a short note on fundamental mode asynchronous circuit.**
    Fundamental mode circuit assumes that. The input variables change only when the circuit is stable. Only one input variable can change at a given time and inputs are levels and not pulses.
41. **Write a short note on pulse mode circuit**.
    Pulse mode circuit assumes that the input variables are pulses instead of level. The width of the pulses is long enough for the circuit to respond to the input and the pulse width must not be so long that it is still present after the new state is reached.
42. **Define secondary variables.**
    The delay elements provide a short term memory for the sequential circuit. The present state and next state variables in asynchronous sequential circuits are called secondary variables.
43. **Define flow table in asynchronous sequential circuit.**
    In asynchronous sequential circuit state table is known as flow table because of the behaviour of the asynchronous sequential circuit. The stage changes occur in independent of a clock, based on the logic propagation delay, and cause the states to flow from one to another.
44. **What is pulse mode asynchronous machine?**
    A pulse mode asynchronous machine has two inputs. If produces an output whenever two consecutive pulses occur on one input line only. The output remains at 1 until a pulse has occurred on the other input line. Write down the state table for the machine.
45. **What is fundamental mode?**

A transition from one stable state to another occurs only in response to a change in the input state. After a change in one input has occurred, no other change in any input occurs until the circuit enters a stable state. Such a mode of operation is referred to as a fundamental mode.

46. **Write short note on shared row state assignment**.
Races can be avoided by making a proper binary assignment to the state variables. Here, the state variables are assigned with binary numbers in such a way that only one state variable can change at any one state variable can change at any one time when a state transition occurs. To accomplish this, it is necessary that states between which transitions occur be given adjacent assignments. Two binary are said to be adjacent if they differ in only one variable.
47. **Write short note on one hot state assignment**.
The one hot state assignment is another method for finding a race free state assignment. In this method, only one variable is active or hot for each row in the original flow table, ie, it requires one state variable for each row of the flow table. Additional row are introduced to provide single variable changes between internal state transitions.

48. What is an asynchronous sequential circuit?
The sequential circuits in which the change in input signals can affect memory element at any instant of time are called asynchronous sequential circuit.
49. How does the operation of an asynchronous input differ from that of a synchronous input?
a. In synchronous sequential circuits memory elements are clocked flipflops. Hence input signals can affect the memory elements only at discrete instsnts of time.
b. In asynchronous sequential circuits memory elements are either unclocked flipflops or time delay elements. Therefore in asynchronous sequential circuits change in input signals can affect the memory elements at any instant of time.
50. What are the types of asynchronous circuits?
    1.Fundamental mode circuits
    2.Pulse mode circuits
51. What is fundamental mode asynchronous sequential circuits?
According to how input variables are to be considered, fundamental mode circuit assume that:
    The input variables change only when the circuit is stable
    Only one input variable can change at a given time
    Inputs are levels and not pulse
    What is pulse mode circuit?