Reg. No. : | | | | | | | | | | | | |

Question Paper Code : 71675

B.E./B.Tech. DEGREE EXAMINATION, APRIL/MAY 2017

Third/Fifth/Sixth Semester

Computer Science and Engineering

CS 6303 — COMPUTER ARCHITECTURE

(Common to Electronics and Communication Engineering , Electronics and Instrumentation Engineering, Instrumentation and Control Engineering, Robotics and Automation Engineering, Information Technology)

(Regulations 2013)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — ($10 \times 2 = 20$ marks)

1. List the major components of a computer system.
2. State the need for indirect addressing mode. Give an example.
3. Subtract $(11010)_2 - (10000)_2$ using 1's complement and 2's complement method.
4. Write the rules to perform addition on floating point numbers.
5. Name the control signals required to perform arithmetic operations.
6. Define hazard. Give an example for data hazard.
7. What is instruction level parallelism?
8. Distinguish implicit multithreading and explicit multithreading.
9. Define memory interleaving.
10. Summarize the sequence of events involved in handling an interrupt request from a single device.

PART B — (5 × 13 = 65 marks)

11. (a) Explain the important measures of the performance of a computer and derive the basic performance equation. (13)

Or

(b) Explain direct, immediate, relative and indexed addressing modes with examples. (13)

12. (a) (i) Demonstrate multiplication of two binary numbers with an example. Design an arithmetic element to perform this multiplication. (7)

(ii) Describe non restoring division with an example. (6)

Or

(b) (i) Design an arithmetic element to perform the basic floating point operations. (7)

(ii) What is meant by sub word parallelism? Explain. (6)

13. (a) Discuss the modified data path to accommodate pipelined executions with a diagram. (13)

Or

(b) (i) Explain the hazards caused by unconditional branching statements. (7)

(ii) Describe operand forwarding in a pipeline processor with a diagram. (6)

14. (a) (i) Discuss the challenges in parallel processing with necessary examples. (6)

(ii) Explain Flynn's classification of parallel processing with necessary diagrams. (7)

Or

(b) Explain the four principal approaches to multithreading with necessary diagrams. (13)

15. (a) Explain the different mapping functions that can be applied on cache memories in detail. (13)

Or

(b) (i) Explain virtual memory address translation in detail with necessary diagrams. (7)

(ii) What is meant by Direct Memory Access? Explain the use of DMA controllers in a computer system. (6)

PART C — (1 × 15 = 15 marks)

16. (a) (i) Explain mapping functions in cache memory to determine how memory blocks are placed in cache. (8)

(ii) Explain in detail about the Bus Arbitration techniques in DMA. (7)

Or

(b) A pipelined processor uses delayed branch technique. Recommend any one of the following possibility for the design of the processor. In the first possibility, the processor has a 4-stage pipeline and one delay slot. In the second possibility, it has a 6-stage pipeline and two delay slots. Compare the performance of these two alternatives, taking only the branch penalty into account. Assume that 20% of the instructions are branch instructions and that an optimizing compiler has an 80% success rate in filling in the single delay slot. For the second alternative, the compiler is able to fill the second slot 25% of the time.
