778

Register No.:

April 2018

Time – Three hours
(Maximum Marks: 75)

[N.B: (1) Q.No. 8 in PART – A and Q.No. 16 in PART – B are compulsory. Answer any FOUR questions from the remaining in each PART – A and PART – B

(2) Answer division (a) or division (b) of each question in PART – C.

(3) Each question carries 2 marks in PART – A, 3 marks in Part – B and 10 marks in PART – C.]

PART – A

1. What do you mean by hazards in digital circuits?
2. Define glitch in digital circuits.
3. Define design entry.
4. Define storage elements.
5. Define state table.
6. Define ASIC.
7. Expand PLA and PAL.
8. Define relational operators.

PART – B

9. Draw the circuit diagram of NMOS inverter and CMOS inverter.
10. Define half adder with circuit diagram.
11. Explain about architecture in VHDL.
12. Explain arithmetic operators.
13. What are the steps involved in designing a synchronous sequential circuit?
14. Write the VHDL code for D latch.
15. Draw the general structure of a PLA and explain.
16. Draw the general structure of a CPLD.

[Turn over.....

PART – C

17. (a) Draw the CMOS AND, OR, inverter and explain with truth table.

(Or)

(b) Implement the function F={1,2,3,5,7,10,13} with minimal gates.

18. (a) Explain in detail about assignment statements.

(Or)

(b) Write the VHDL code for 8:3 Encoder.

19. (a) Design a modulo 7 counter using D-FF. Use proper excitation table and state diagram.

(Or)

(b) Design a modulo 5 counter using D-FF. Use proper excitation table and state diagram.

20. (a) Write a VHDL code for T-FF with reset input.

(Or)

(b) Write a VHDL code for 2 bit up counter.

21. (a) Explain in detail about PAL and PLA.

(Or)

(b) A combinational circuit is defined by the function $F=\sum\{3,4,5,7,10,14,15\}$. Implement the function in PLA.
