UNIT 1 and UNIT 2
8086 MICROPROCESSOR

1. If [CS]=348AH, [IP]=4214H, then the 20-bit physical address from which the code is accessed will be
(A) 455CAH (B) 0769EH (C) 390B4H (D) 38AB4H
Answer: D
Detailed Solution: Effective address= Base address of CS register X 10H + Address of IP
= 348AH X 10H + 4214H
= 38AB4H

2. Setting of direction flag in 8086 causes,
(A) The microprocessor to operate in single stepping mode
(B) The microprocessor to operate in break point mode
(C) The microprocessor string operations in auto increment mode
(D) The microprocessor string operations in auto decrement mode
Answer: D
Detailed Solution: If directional flag is set (1), then the string data is accessed from higher memory location towards lower memory location.

3. In order to read a word from the memory location 5000AH in a single bus cycle, the status of the 8086 signals A0 and BHE' should be
(A) A0 = 0, BHE', = 0
(B) A0 = 0, BHE' =1
(C) A0 = 1, BHE'= 0
(D) A0 = 1, BHE' = 1
Answer: A
Detailed Solution: As a word is to be read from the memory, $\overline{BHE}$ = 0 is used as a memory enable signal and the memory location 5000AH is even, A0 = 0 for even address.

4: If [BX]=0050H, [DS]=2000H, [00500H]=80H, [20050H]=08H, [CX]=5000H, then after MOV CL,[BX] instruction is executed the contents of CX will be
(A)0050H
(B)5008H
(C) 5080H
(D) 0008H
Answer: B
Detailed Solution: [DS] X 10H + [BX]
= 20000H + 0050H
= 20050H
After the execution of MOV CL,[BX] which copies the contents of the memory at address BX to CL, the contents of CX will be 5008H.

5: Before the execution of POP instruction the stack pointer points to FFFFH. The contents of the stack pointer after execution of POP instruction will be
(A) FFFFH (B) 0000H (C) 0001H (D) 0002H
Answer: C
Detailed Solution: After the execution of POP instruction, the stack pointer is automatically incremented by 2 to point to the next word on the stack.

6: If [AL]=35H and [BL]=39H, after the execution of the following instructions
ADD AL, BL
AAA
the contents of AL will be
(A) 6EH
(B) 3EH
(C) 14H
(D) 04H
Answer: D
Detailed Solution: Numerical data coming into a computer from a terminal is usually in ASCII code. In this code, the numbers 0 to 9 are represented by the ASCII codes 30H to 39H. The 8086 allows to add the ASCII codes for two decimal digits without masking off the "3" in the upper nibble of each. After the addition, the AAA instruction is used to make sure the result is the correct unpacked BCD. If the addition produces a decimal carry (AF=1), the AH register is incremented and the carry (CF) and auxiliary carry (AF) flags are set to 1. If the addition did not produce a decimal carry, CF and AF are cleared to 0 and AH is not altered. In both cases, the high-order 4 bits of AL are cleared to 0.

7: Which of the following is unpacked BCD number
(A) 23 (B) 2B (C) 08 (D) 0A
Answer: C
Detailed Solution: Unpacked BCD number contains only one decimal digit per byte. The digit is stored in the least significant 4 bits and rest of the bits are 0.

8: The WAIT instruction causes the 8086 to enter into ideal state until
(A) The LOCK' pin is made LOW
(B) The LOCK' pin is made HIGH
(C) The TEST' pin is made LOW
(D) The TEST' pin is made HIGH
Answer: C
Detailed Solution: If the TEST pin is Low, execution continues otherwise the processor waits in an "idle" state.

9: If [AX]=009BH, after the execution of CBW instruction the contents of AX will be
(A) 009BH (B) FF9BH (C) 0000H (D) 9B9BH
Answer: B

Detailed Solution: CBW converts the signed value in the AL register into an equivalent 16 bit signed value in the AX register by duplicating the sign bit to the left. This instruction copies the sign (bit 7) in the source operand into every bit in the AH register.

10: Which of the following is not an 8086 maximum mode signal?
(A) LOCK
(B) S0
(C)ALE
(D) QS0
Answer: C
Detailed Solution: ALE is a minimum mode signal.

11: What is the maximum capacity of the memory that can be interfaced to the microprocessor which contains 20 address lines?
a.) 64 KB
b.) 1 MB
c.) 64 MB
d.) 1 GB
Answer: B
Detailed Solution: Maximum Capacity = 2^{20} = 1048576 = 1MB

12: The size of ALU in 8086 is
a.) 8 bit
b.) 16 bit
c.) 24 bit
d.) 32 bit
Answer: B

13: Which of the following is used to sequence the execution of instructions
a.) Segment register
b.) Stack pointer
c.) Instruction pointer
d.) Flag register
Answer: C

14: What are the status of carry and auxiliary carry flags after performing the subtraction of 0FH from F0H
a.) Both the flags are reset
b.) Both the flags are set
c.) Carry flag is set and auxiliary carry flag is reset
d.) Carry flag is reset and auxiliary carry flag is set
Answer: D

Detailed Solution: Consider the Subtraction as follows:

Since Minuend is greater than Subtrahend, there will be no carry. Hence the Carry flag will be reset. In this arithmetic operation, a borrow is transferred from bit position 4 to bit position 3. Hence auxiliary carry flag will be set.

15: If [CS] = 5500H, [IP] = 1200H, then the 20-bit physical address would be
a.) 56200H b.) 67000H c.) 17500H d.) 57500H

Answer: A
Detailed Solution: Effective Address = Base address of CS register × 10H + Address of IP
= 5500H × 10H + 1200H = 56200H

16: The 8086 XLAT is used to
a.) Exchange the contents of memory with register b.) Convert the byte into word
c.) Convert the word into double word d.) Convert the ASCII into EBCDIC
Answer: D

17: What is the ASCII code corresponds to decimal 9
a.) 39H
b.) 49H
c.) E9H
d.) F9H

Answer: A

18: In order to perform multi-byte addition, which of the following instruction will be used
a.) ADD
b.) ADC
c.) AAA
d.) AAD
Answer: B

19: What will be the contents of AX after execution of the following instructions
MOV AL, FFH
MOV BL, 05H
MUL BL

a.) 04FAH b.) 04FBH c.) 04FCH d.) 04FDH
Answer: B
Detailed Solution: After execution of 1st instruction, the content of AL is FFH i.e 255 in decimal. Similarly, after execution of 2nd instruction, the content of BL is 05H i.e 05 in decimal. The third instruction multiplies content of BL (05) with that of AL (i.e) 255 and stores the result in AX. We know that 255 × 5 = 1275 which is equal to 04FBH in hexadecimal.

20: What will be the contents of AL after execution of the following instructions
MOV AL, 65H

MOV BL, 75H
ADD AL, BL
DAA

a.) DAH
b.) E0H
c.) 40H
d.) 41H
Answer: C
Detailed Solution: Upon the execution of 1st and 2nd instruction, we have 65H and 75H in AL and BL respectively. The third instruction adds the content of AL and BL and the result is stored in AL.
Consider the following:
0110 0101 (65H) + 0111 0101 (75H) = 1101 1010 (DAH)

Now, the DAA instruction adds 0110 (6H) to first nibble i.e 1010, if greater than 1001 (9H). Similarly, it adds 0110 (6H) to second nibble i.e. 1101, as well because it is also greater than 1001 (9H). As a result, we get the final result as, 1101 1010 + 0110 0110 = 0100 0000 (40H).

21: What will be the contents of AL after execution of the following instructions
MOV AL, 39H
MOV BL, 34H
ADD AL, BL
AAA
a.) 6DH
b.) 13H
c.) 33H
d.) 03H
Answer: D
Detailed Solution: https://www.youtube.com/watch?v=-z1U-ys8HCc

22: If [DL]=EFH and carry flag is reset, what will be the contents of DL after execution of the instruction ROL DL,01H
a.) 5FH
b.) DFH
c.) F7H
d.) 77H
Answer: B
Detailed Solution: The instruction, ROL DL,01H, rotates the content of [DL] by one bit to the left. The content of DL is EFH which is 1110 1111 in binary. When we rotate it by 1 bit to the left we get 1101 1111 which is DFH in hexadecimal.

23: If [AL]=EFH, after the execution of NEG AL, the contents of AL would be
a.) 00H
b.) 10H
c.) 11H

d.) 12H
Answer: C
Detailed Solution: EFH is equal to 1110 1111 in binary. The NEG AL instruction corresponds to 2's complement of the content of AL which is 1110 1111. The 2's complement of 1110 1111 is 0001 0001 which is equal to 11H.

24: Which of the following instruction is equivalent to XOR AL, AL
a.) OR AL,00H
b.) AND AL,00H
c.) OR AL, FFH
d.) AND AL, FFH
Answer: B
Detailed Solution: Ex-OR of a quantity with itself is always 0. Also, when we do the AND operation of any quantity with 0, the result is always 0. Hence option B is the Answer.

25: After the execution of CALL instruction
(A) The contents of stack pointer will be incremented by 1
(B) The contents of stack pointer will be decremented by 1
(C) The contents of stack pointer will be incremented by 2
(D) The contents of stack pointer will be decremented by 2

Answer: D

26: The instruction REPZ CMPSB compares string bytes
(A) Until end of the string or until string bytes not equal
(B) Until end of the string or until string bytes equal
(C) Until end of the string or until string words not equal
(D) Until end of the string or until string words equal

Answer: A

27: Type 3 interrupt is
(A) Divide by zero interrupt
(B) Single step interrupt
(C) Breakpoint interrupt
(D) Interrupt on overflow
Answer: C
Detailed Solution: The starting address for type0 interrupt is 000000H, for type1 interrupt is 00004H similarly for type2 is 00008H and so on. The first five pointers are dedicated interrupt pointers. i.e. –

- TYPE 0 interrupt represents division by zero situation.
- TYPE 1 interrupt represents single-step execution during the debugging of a program.
- TYPE 2 interrupt represents non-maskable NMI interrupt.
- TYPE 3 interrupt represents break-point interrupt.
- TYPE 4 interrupt represents overflow interrupt.

The interrupts from Type 5 to Type 31 are reserved for other advanced microprocessors, and interrupts from 32 to Type 255 are available for hardware and software interrupts.

28: The size of interrupt pointer table in 8086 is
(A) 256 bytes
(B) 512 bytes
(C) 1024 bytes
(D) 2048 bytes
Answer: C

Detailed Solution: The interrupt vector table in the 8086/8088 is the first 1024 bytes in memory. There are 256 vectors, each containing 4 bytes, CS: IP, for each possible interrupt source.

29: After the execution of INT 2 instruction
A) The contents of stack pointer will be incremented by 2
(B) The contents of stack pointer will be decremented by 2
(C) The contents of stack pointer will be incremented by 4
(D) The contents of stack pointer will be decremented by 4

Answer: D
Detailed Solution: 8086 responds to the interrupt by performing series of actions:
1. It decrements stack pointer by 2 and pushes the flag register on the stack.
2. It disables the INTR interrupt input by clearing the interrupt flag in the flag
3. It resets the trap flag in the flag register.
4. It decrements stack pointer by 2 and pushes the current code segment register contents on the stack.
5. It decrements stack pointer by 2 and pushes the current instruction pointer contents on the stack.
6. It does an indirect far jump at the start of the procedure by loading the CS and IP values for the start of the interrupt service routine (ISR).

30: Which of the following instruction is used to pass the instructions from 8086 to coprocessor 8087?
(A) INT 3
(B) JMP
(C) LOCK
(D) ESC
Answer: D

31: The execution of WAIT instruction causes 8086 to enter into ideal state until
(A) The $\overline{TEST}$ pin is made LOW
(B) The $\overline{TEST}$ pin is made HIGH

(C) The $\overline{LOCK}$ pin is made LOW

(D) The $\overline{LOCK}$ pin is made HIGH

Answer: A
Detailed Solution: The WAIT instruction monitors the BUSY and TEST pin of 8086 Microprocessor. If TEST=0, then Microprocessor executes WAIT instruction until TEST=1.

32: If [DX]=0000H and [AX]=F000H, after the execution of the instruction CWD, the contents of DX and AX respectively are
(A) 0000H and F000H
(B) F000H and 0000H
(C) FFFFH and F000H
(D) F000H and FFFFH
Answer: C
Detailed Solution: CWD instruction enlarges the sign bit of a word into AX register to all the bits of the DX register. This is used before a signed word in AX is to be divided through another signed word by using IDIV instructions. No flags are influenced.

33: To evaluate which of the following expressions subroutine concept is useful
(A) $X + Y^2$ (B) $X^2 + Y$ (C) $X + Y$ (D) $X^2 + Y^2$
Answer: D
Detailed Solution: In option (D), two multiplications are involved. So, subroutine concept is useful.

34: An 8× 4 ROM can be constructed using
(A) A 2× 4 decoder and four 4-input OR gates
(B) A 2× 4 decoder and four 8-input OR gates
(C) A 3× 8 decoder and four 4-input OR gates
(D) A 3× 8 decoder and four 8-input OR gates
Answer: D
Detailed Solution: A 2k x n ROM will have an internal k x 2k decoder and n 2k-input OR gates.

35: The number of basic cells in a 16 × 4 RAM are
(A) 4 (B) 16 (C) 64 (D) 128
Answer: C
Detailed Solution: It consists of 16 words of 4 bits each and has a total of 64 binary cells.

36: Which of the following statement is TRUE
(A) Both ROM and RAM are combinational circuits
(B) ROM is a combinational circuit and RAM is a sequential circuit
(C) ROM is a sequential circuit and RAM is a combinational circuit
(D) Both ROM and RAM are sequential circuits

Answer: B

37: Which of the following memory is volatile
(A) ROM
(B) PROM
(C) EPROM
(D) RAM
Answer: D
Detailed Solution: Data in RAM is not permanently written. When you power off your computer the data stored in RAM is deleted.

38: Upon RESET, the 8086 microprocessor starts the operations from the memory location
(A) 0000H
(B)0FFFFH
(C)FFFF0H
(D)FFFFH
Answer: C
Detailed Solution: The reset pin of 8086 and other processors will cause the CS: IP to point to FFFF:0000 which is the lowest 16 bytes of the memory. In that location there is a jump instruction to somewhere else in the memory space to initialize the processor.

39: If the starting address of 1KB memory is 00500H, then the ending address would be
(A) 008FFH
(B) 00CFFH (C) 01400H (D) 01500H
Answer: A
Detailed Solution: 00500 H when converted to decimal becomes 1280 and 1KB = 1024, so 1280+1024 = 2304. So the memory location will be 2303 converted to hex which is 08FF H.

40: If the chip select of 8KB RAM is

$\overline{CS} = \overline{(A13)(A14)(A15)(A16)(A17)(A18)(A19)}$. The address range of RAM would be
(A) 00000H-1FFFFH
(B) FC000H-FFFFFH
(C) FE000H-FFFFFH
(D) FF000H-FFFFFH

Answer: C
Detailed Solution: The address lines are 0 to 19. In hexadecimal this range is from 00000 H to FFFFF H values. This entire range is not addressable because of the chip select line connected to the address lines 13 to 19. The CS line is driven by an A13 to A19 have values 1111 1110 0000 0000 0000 H to 1111 1111 1111 1111 1111 H. The final address range, which in hexadecimal is FE000 H to FFFFF H.

41: In order to program Port A and Port B as output ports in Mode 0 and Port C as input port in Mode 0, the control word for 8255 would be
(A) 89H
(B) 98H
(C) 6FH
(D) F6H

Answer: A
Detailed Solution: https://www.geeksforgeeks.org/programmable-peripheral-interface-8255/

42 : The time taken to execute MOV CX, FFFFH using 8086 with 5 MHz clock would be
(A) 0.2 µs
(B) 0.4 µs
(C) 0.6 µs
(D) 0.8 µs

Answer: D
Detailed Solution: https://theencarta.com/mov-instruction-8086/

43: The number of clock cycles required to execute NOP operation of 8086 is
(A) 1
(B) 2
(C) 3
(D) 4

Answer: C
Detailed Solution: At the time of execution of NOP instruction, no operation is performed except fetch and decode. It takes three clock cycles to execute the instruction. NOP instruction does not affect any flag. This instruction is used to fill in time delays or to delete and insert instructions in the program while trouble shooting.

44. Number of the times the instruction sequence below will loop before coming out of loop is
MOV AL, 00h
A1: INC AL
JNZ A1

(A) 00
(B) 01
(C) 255
(D) 256
Ans Answer is (D)

45. What will be the contents of register AL after the following has been executed
MOV BL, 8C

MOV AL, 7E
ADD AL, BL
(A) 0A and carry flag is set (B) 0A and carry flag is reset
(C) 6A and carry flag is set (D) 6A and carry flag is reset
Ans, Result is 1,0A. Hence answer is (A).

46. Direction flag is used with
(A) String instructions. (B) Stack instructions.
(C) Arithmetic instructions. (D) Branch instructions.
Ans The direction flag is used only with the string instructions. Hence answer is (A).

47. Ready pin of a microprocessor is used
(A) to indicate that the microprocessor is ready to receive inputs.
(B) to indicate that the microprocessor is ready to receive outputs.
(C) to introduce wait states.
(D) to provide direct memory access.
Ans This input is controlled to insert wait states into the timing of the microprocessor.
Hence answer is (C).

48. These are two ways in which a microprocessor can come out of Halt state.
(A) When hold line is a logical 1.
(B) When interrupt occurs and the interrupt system has been enabled.
(C) When both (A) and (B) are true.
(D) When either (A) or (B) are true.
Ans Answer is (A)

49. LOCK prefix is used most often
(A) during normal execution. (B) during DMA accesses
(C) during interrupt servicing. (D) during memory accesses.
Ans LOCK is a prefix which is used to make an instruction of 8086 non-interruptable.
Hence answer is (C).

50. The Pentium microprocessor has_____execution units.
(A) 1
(B) 2
(C) 3
(D) 4
Ans The Pentium microprocessor is organized with three execution units. One executes floating-point instructions, and the other two (U-pipe and V-pipe) execute integer instructions. Hence answer is (C).

51. The memory data bus width in Pentium is
(A) 16 bit
(B) 32 bit

(C) 64 bit
(D) None of these
Ans The Data bus width is 64 bits. Hence answer is (C).

52. The no. of address lines required to address a memory of size 32 K is
(A) 15 lines (B) 16 lines
(C) 18 lines (D) 14 lines

Ans 32K= 32X1024bits= $2^5X2^{10}=2^{15}$. Hence answer is (A).

53. NMI input is
(A) Edge sensitive (B) Level sensitive
(C) Both edge and level triggered (D) edge triggered and level sensitive

Ans Non-maskable interrupt (NMI) is an edge –triggered input that requests an interrupt on the positive edge (0 to 1 transition).

54. How many types of basic multiprocessor configurations?
A. 2
B. 3
C. 4
D. 5
Ans : B

Explanation: Multiprocessor means a multiple set of processors that executes instructions simultaneously. There are three basic multiprocessor configurations : Coprocessor configuration, Closely coupled configuration and Loosely coupled configuration.

55. A _____ is a specially designed circuit on microprocessor chip which can perform the same task very quickly, which the microprocessor performs
A. Coprocessor configuration
B. Closely coupled configuration
C. Loosely coupled configuration
D. None of the above

Ans : A

56. The coprocessor and the processor is connected via?
A. TEST
B. QS0
C. QS1
D. All of the above

Ans : D

Explanation: The coprocessor and the processor is connected via TEST, RQ-/GT- and QS0 & QS1 signals.

57. _____signal takes care of the coprocessor's activity, i.e. the coprocessor is busy or idle.
A. TEST
B. QS0
C. QS1
D. None of the above
Ans : A

58. Which of the following are advantage of Loosely Coupled Configuration?
A. Having more than one processor results in increased efficiency.
B. easy to achieve parallel processing.
C. system structure is flexible
D. All of the above

Ans : D

59.. 8087 numeric data processor is also known as?
A. Math co-processor
B. Numeric processor extension
C. Floating point unit
D. All of the above

Ans : D

60. 8087 Architecture is divided into?
A. 2
B. 3
C. 4
D. 5

Ans : B

Explanation: 8087 Architecture is divided into two groups, i.e., Control Unit (CU) and Numeric Extension Unit (NEU).

61. The _____ handles all the communication between the processor and the memory
A. numeric extension unit
B. Packed Unit
C. control unit
D. Binary Unit

Ans : C

62. 8087 Numeric Data Processor designed by?
A. Intel
B. IBM
C. Microsoft
D. VAX

Ans : A

Explanation: It was the first math coprocessor designed by Intel to pair with 8086/8088 resulting in easier and faster calculation.