

## UNIT 3 I/O INTERFACING

1. Which of the following operation is not involved in interfacing a keyboard to 8086

- (A) Detect a keypress
- (B) Debounce the keypress
- (C) Decode the keypress
- (D) Encode the keypress

Correct Answer: C

2. The process of making sure a previous key has been released before looking for next one is called

- (A) Decoding of the key
- (B) Debouncing of the key
- (C) Encoding of the key
- (D) Two key lockout

Correct Answer: D

3. In order to interface a hexadecimal keyboard to 8086

- (A) One 8-bit port of 8255 must be programmed as input port and 4-bits of another port must be programmed as output port
- (B) One 8-bit port of 8255 must be programmed as output port and 4-bits of another port must be programmed as input port
- (C) One 8-bit port of 8255 and 4-bits of another port must be programmed as output ports
- (D) 01500H One 8-bit port of 8255 and 4-bits of another port must be programmed as input ports

Correct Answer: A

4. Let a BCD to 7-segment decoder (7447) is interfaced to a common anode type 7- segment display. If the BCD input to 7447 is 1001 and common signal of 7-segment display is connected to logic 1,

- a. All the segments of display will be at logic 0
- b. Only the segment "e" will be at logic 0
- c. All the segments except "e" will be at logic 0
- d. All the segments except "e" will be at logic 1

Correct Answer: C

5. In order to rotate stepper motor in anti-clockwise direction, which of the following bit sequence need to be applied to its windings

- a. 0011,1001,1100,0110
- b. 0110,1100,1001,0011
- c. 1000,1100,1110,1111
- d. 1111,1110,1100,1000

Correct Answer: B

6. In order to start the conversion, the WR signal of A/D converter 0804 must be

- a. Kept HIGH
- b. Kept LOW
- c. Changed from LOW to HIGH
- d. Changed from HIGH to LOW

Correct Answer: C

Detailed Solution: WR which is connected to PC3 of 8255, acts as start of conversion signal so whenever microprocessor wants to start any conversion, WR changed from LOW to HIGH.

7. The end of conversion of A/D converter 0804 is represented by
- a. INTR = 0
  - b. INTR = 1
  - c. WR = 0
  - d. WR = 1

Correct Answer: A

8. For  $\pm 5V$  analog input voltage range, the A/D converter 0804 produces digital output in the range of 00H to FFH. If the input analog voltage is 0 V, the corresponding digital output would be
- a. 00H
  - b. 70H
  - c. 80H
  - d. 90H

Correct Answer: C

Detailed Solution: Total range of voltage is +5 V to -5V, i.e., total voltage is 10V and the bit range is 8 bit (00H to FFH). So each step has a voltage of  $10V/255(2^8-1)=0.039V$ . It is given that -5V is 00 H, so 0V, i.e.,  $-5V+5V=0V$ , there is 5V difference between 0V and -5V. So 0.039 shows one step so 5V shows  $5V/0.039$  steps, i.e., 128 steps. So 0V will be represented by  $00H$  (for -5V)  $+128=128=10000000=80H$  (for 0V).

9. For 0 – 5V analog input voltage range, the A/D converter 0804 produces digital output in the range of 00H to FFH. If the input analog voltage is 0.196 V, the corresponding digital output would be
- a. 01H
  - b. 05H
  - c. 0AH
  - d. 10H

Correct Answer: C

Detailed Solution: Total range of voltage is 0 V to 5V, i.e., total voltage is 5V and the bit range is 8 bit (00H to FFH). So each step has a voltage of  $5V/255(2^8-1)=0.0196V$ . It is given that 0V is 00 H, so 0.196V, i.e.,  $0V+0.196V=0.196V$ , there is 0.196V difference between 0V and 0.0196V. So 0.0196 shows one step so 0.196V shows  $0.196V / 0.0196$  steps, i.e., 10 steps. So 0.196V will be represented by  $00H$  (for 0V)  $+10=00001010=0AH$  (for 0.196V).

10. If 0800 would be
- a. 1 mA
  - b. 2 mA

- c. 3 mA
- d. 4 mA

IREF = 2mA and digital input to D/A converter IC 0800 is 10000000, the output current of

Correct Answer: A

Detailed Solution:  $I_{OUT} = I_{REF} ((1/2) B_n + (1/4) B_{n-1} + \dots + (1/2^n) B_0) = 2mA ((1/2) \times 1 + 0) = 1mA$

11. A 5 K  $\Omega$  feedback resistor is connected in the current to voltage converter at the output of D/A converter. If the digital input to IC 0800 is FFH, the analog output voltage for bipolar operation would be
- a. -10 V
  - b. 0 V
  - c. +5 V
  - d. +10 V

Correct Answer: C and D

12. In the above question 7, the analog output voltage for unipolar operation would be
- a. -10 V
  - b. 0 V
  - c. +5 V
  - d. +10 V

Correct Answer: C and D

13. If the address of 8254 control word register is 97H, the address of counter 0 would be
- a. 96H
  - b. 95H
  - c. 94H
  - d. 93H

Correct Answer: C

Detailed Solution: The least significant two bits are used to point counter 0, counter 1, counter 2 and Control word register. 00 for counter 0, 01 for counter 1, 10 for counter 2 and 11 for control word register. In this way, if 97H points to CWR then 96H would point to counter 2, 95H for counter 1 and 94H for counter 0.

14. If 0FH is loaded into control word register of 8254, then the mode selected would be
- a. Mode 2
  - b. Mode 3
  - c. Mode 4
  - d. Mode 5

Correct Answer: B

Detailed Solution: 0FH corresponds to 0000 1111. So, M2, M1 and M0 is 111 which corresponds to Mode 3.

15. In mode 0 of 8254, the GATE input must
- a. kept LOW
  - b. kept HIGH

- c. change from LOW to HIGH
- d. change from HIGH to LOW

Correct Answer: B

16. Which of the following mode generates square wave?
- a. Mode 2
  - b. Mode 3
  - c. Mode 4
  - d. Mode 5

Correct Answer: B

17. In order to read the count in the 8254 counter while count is still going on, which of the following operation would be performed?
- a. Latching
  - b. Triggering
  - c. Strobe
  - d. Single stepping

Correct Answer: A

18. If the chip select of 8254 is generated using \_\_\_\_\_, the address of counter 2 would be
- a. 48H
  - b. B5H
  - c. B6H
  - d. B7H

Correct Answer: C

Detailed Solution: The given Chip select corresponds to 101101. For counter 2, A1, A0 will be 10. So, the address of counter 2 would be 10110110 which is nothing but B6H.

19. In order to generate 1 KHz square wave using 8254 operated at 2 MHz clock, the count that must be loaded into counter would be
- a. 03FFH
  - b. 07D0H
  - c. 1000H
  - d. 2000H

Correct Answer: B

Detailed Solution: Frequency of the square wave is 1 KHz which corresponds to 1ms. Similarly, Clock time period is 0.5 microsecond. So, the required count would be  $1\text{ms}/0.5\text{ microsecond}$ , which is equal to 2000. The Hexadecimal equivalent of 2000 is 07D0 H.

20. The hardware-triggered strobe mode of 8254 is same as software-triggered strobe mode except that
- a. Triggering is performed by rising pulse at GATE
  - b. Triggering is performed by falling pulse at GATE
  - c. Triggering is performed by rising pulse at Clock
  - d. Triggering is performed by falling pulse at Clock

Correct Answer: A

21. Assuming that the interrupt request IR2 has just been serviced in automatic rotation mode, then the next highest priority will be assigned to

- a. IR0
- b. IR1
- c. IR3
- d. IR7

Correct Answer: C

Detailed solution: In automatic rotation mode, the interrupt request that has just been serviced is given the lowest priority and the next one is given the highest priority.

22. In automatic end of interrupt,
- a. 8259A resets the highest priority in-service register (ISR) bit
  - b. The command specifies which ISR bit to be reset
  - c. 8259A resets the lowest priority in-service register (ISR) bit
  - d. No command is necessary, during third  $\overline{INTA}$  the ISR bit is reset

Correct Answer: D

23. In which of the following modes the ISR does not have information on which IR is being serviced
- a. Nonspecific EOI
  - b. Specific EOI
  - c. Automatic EOI
  - d. None of the above

Correct Answer: C

24. Which of the following is used in cascading mode of 8259A?
- a. ICW 1
  - b. ICW 2
  - c. ICW 3
  - d. ICW 4

Correct Answer: C

25. If the port address of the 8259A for ICW 2 is 81H, then the port address of ICW 3 would be
- a. 80H
  - b. 81H
  - c. 82H
  - d. 83H

Correct Answer: B

Detailed Solution: In both cases  $A_0 = 1$ . Hence the port address of ICW 3 would be 81H.

26. If the chip select of 8259A is generated using  $CS = A7A6A5A4A3A2A1$ , then the port address of operation command word OCW 2 would be
- a. 48H
  - b. 49H
  - c. B6H
  - d. B7H

Correct answer: C

Detailed solution: The chip select corresponds to 1011 011 and  $A_0$  will be 0. Hence, port address would be 1011 0110 which is B6H.

27. If 16H is loaded into ICW 1 of 8259A, then the 8259A operates in
- Single mode with call address interval of 4
  - Single mode with call address interval of 8
  - Cascade mode with call address interval of 4
  - Cascade mode with call address interval of 8

Correct answer: A

Detailed solution: 16H corresponds to 0001 0110. The D1 i.e. 2nd LSB is 1 which corresponds to Single mode. Similarly, D2 i.e. 3rd LSB is 1 which corresponds to 4 bytes interval.

28. If 10H is loaded into OCW 1 of 8259A, then
- IR2 is masked
  - IR3 is masked
  - IR4 is masked
  - IR5 is masked

Correct answer: C

29. If 00H is the address of 8237A channel 0 memory address register, then the address of channel 3 count register would be
- 01H
  - 03H
  - 05H
  - 07H

Correct Answer: D

30. The signals AEN and ADSTB of 8237A are used to latch a
- Lower order address byte
  - Higher order address byte
  - Lower order data byte
  - Higher order data byte

Correct answer: B

31. In slave mode DMA controller is treated as
- Peripheral
  - Processor for data transfer from memory to I/O
  - Processor for data transfer from I/O to memory
  - Processor for bidirectional data transfer

Correct answer: A

32. Which of the following statement is FALSE with respect to synchronous serial data transmission?
- Transmitter and receiver will be operated by the same clock
  - Character is transmitted along with the synchronization information
  - Character is transmitted along with the start and stop bits
  - Used for high-speed transmission with bit rates more than 20 Kbps

Correct Answer: C

33. In order to transmit ASCII characters in serial bit format at 2000 baud, each bit time duration would be
- 0.5 ms
  - 1 ms
  - 2 ms
  - 3.5 ms

Correct Answer: A

34. In order to convert data bits into audio signals, which of the following is used
- Serial to parallel converter
  - Parallel to serial converter
  - RS-232C
  - MODEM

Correct answer: D

35. The integrated circuit MC 1488 is used to
- Convert RS-232C levels into TTL levels
  - Convert TTL levels into RS-232C levels
  - Convert RS-232C current levels into RS-232C voltage levels
  - Convert RS-232C voltage levels into RS-232C current levels

Correct answer: B

36. The example of full duplex transmission is
- Computer to printer
  - Computer to CRT terminal
  - Computer to 7-segment display
  - Computer to computer

Correct Answer: D

37. If 02H is loaded into 8251A mode word register, which of the following is correct
- 8251A operates in synchronous mode
  - 8251A operates in asynchronous mode with baud rate factor of 1
  - 8251A operates in asynchronous mode with baud rate factor of 16
  - 8251A operates in asynchronous mode with baud rate factor of 64

Correct Answer: C

Detailed Solution: D1D0=10 in mode word register indicates asynchronous mode with baud rate factor of 16.

38. If the port address of 8251A status register is FFH, the port address of control register would be
- FCH
  - FDH
  - FEH
  - FFH

Correct Answer: D

39. If the transmitter clock frequency of 8251A is 153.6 kHz and the baud rate in asynchronous mode is 2400, the baud rate factor would be
- 1
  - 16
  - 32
  - 64

Correct Answer: D

Detailed Solution: In asynchronous mode, the baud rate is a fraction of the actual clock frequency. Baud rate factor = Clock frequency/Baud rate

40. The size of display random access memory in 8279 is
- 8×8 (B) 16×8 (C) 32×8 (D) 64×8

Correct Answer: B

Detailed Solution: Self-explanatory

41. The size of FIFO/Sensor RAM in 8279 is
- 8×8 (F) 16×8 (G) 32×8 (H) 64×8

Correct Answer: A