UNIT 4
8051 MICROCONTROLLER

1. What do you mean by micro in microcontroller?
a) Distance between 2 IC's
b) Distance between 2 transistors
c) Size of a controller
d) Distance between 2 pins

Answer: b
…

2. What is the bit size of the 8051 microcontroller?
a) 8-bit
b) 4-bit
c) 16-bit
d) 32-bit

Answer: a

3. Name the architecture and the instruction set for microcontroller?
a) Van- Neumann Architecture with CISC Instruction Set
b) Harvard Architecture with CISC Instruction Set
c) Van- Neumann Architecture with RISC Instruction Set
d) Harvard Architecture with RISC Instruction Set

Answer: b

4. Number of I/O ports in the 8051 microcontroller?
a) 3 ports
b) 4 ports
c) 5 ports
d) 4 ports with last port having 5 pins

Answer: b

5. Is ROM is used for storing data storage?
a) True

b) False

Answer: b

6. SCON in serial port is used for which operation?
a) Transferring data
b) Receiving data
c) Controlling
d) Controlling and transferring

Answer: c

7. Program counter stores what?
a) Address of before instruction
b) Address of the next instruction
c) Data of the before execution to be executed
d) Data of the execution instruction

Answer: b

8. Auxiliary carry is set during which condition?
a) When carry is generated from D3 to D4
b) When carry is generated from D7
c) When carry is generated from both D3 to D4 and D7
d) When carry is generated at either D3 to D4 or D7

Answer: a

9. What is order of the assembly and running 8051 program?
i) Myfile.asm
ii) Myfile.lst
iii) Myfile.obj
iv) Myfile.hex
a) i,ii,iii,iv
b) ii,iii,I,iv
c) iv,ii,I,iii
d) iii,ii,I,iv

Answer: a.

10. The use of Address Latch Enable is to multiplex address and data memory.
a) True
b) False

Answer: a

11. Which pin provides a reset option in 8051?
a) Pin 1
b) Pin 8
c) Pin 11
d) Pin 9

Answer: d

12. External Access is used to permit _____
a) Peripherals
b) Power supply
c) ALE
d) Memory interfacing

Answer: d

13. What is the address range of SFRs?
a) 80h to feh
b) 00h to ffh
c) 80h to ffh
d) 70h to 80h

Answer: c

14. How many interrupts are there in micro controller?
a) 3
b) 6
c) 4
d) 5

Answer: d

15. Timer 0 is a _____ bit register.
a) 32-bit
b) 8-bit
c) 16-bit
d) 10-bit

Answer: c

16. Number of pins in 8051 microcontroller with _____ package.
a) 40 pin with LLC
b) 60 Pin with QFP
c) 40 pin with DIP
d) 60 pin with QFP

Answer: c

17. Does an 8051 microcontroller need external oscillator to run?
a) True
b) False

Answer: a

18. We use any other frequency source other than crystal oscillator.
a) True
b) False

Answer: a

19. Reset work is _____
a) To make program counter zero but values in registers values are made as zero
b) Program counter is not zero but values in registers values are made as Zero
c) Program counter not zero but values in registers values remain same

d) To make program counter zero but values in registers values remain same

Answer: d

20. What is the minimum no of cycles required for reset operation?
a) 3 cycle
b) 2 cycles
c) 1 cycles
d) 4 cycles

Answer: c

21. PSEN stands for _____
a) Program Select Enable
b) Peripheral Store Enable
c) Program Store Enable
d) Peripheral Select Enable

Answer: c

22. Find the machine cycle for 8051 if XTAL = 11.0592MHz.
a) 90.42us
b) 361.68us
c) 1.085us
d) 150.145us

Answer: b
Explanation: Machine cycle = No.of cycles/frequency
Time = 1/frequency
Time(ns) = 1/11.0592MHz
= 90.42ns
Machine cycles = 12*90.42
= 1.085us.

23. What is the operation for mode 0?
a) 13-bit timer mode, 8-bit timer/counter THx and TLx as 5-bit prescalar
b) 16-bit timer mode, 16-bit timer/counter THx and TLx are cascaded, no prescalar
c) 8-bit auto reload mode, 8-bit auto reload time/counter; THx holds a value

which is to be reloaded into TLx each time it overflows
d) Spilt timer mode

Answer: a

24. What is the operation for mode 1?
a) 13-bit timer mode, 8-bit timer/counter THx and TLx as 5-bit prescalar
b) 16-bit timer mode, 16-bit timer/counter THx and TLx are cascaded, no prescalar
c) 8-bit auto reload mode, 8-bit auto reload time/counter; THx holds a value which is to be reloaded into TLx each time it overflows
d) Spilt timer mode

Answer: b

25. Which is the operation for mode 2?
a) 13-bit timer mode, 8-bit timer/counter THx and TLx as 5-bit prescalar
b) 16-bit timer mode, 16-bit timer/counter THx and TLx are cascaded, no prescalar
c) 8-bit auto reload mode, 8-bit auto reload time/counter; THx holds a value which is to be reloaded into TLx each time it overflows
d) Spilt timer mode

Answer: c

26. Which is the operation for mode 3?
a) 13-bit timer mode, 8-bit timer/counter THx and TLx as 5-bit prescalar
b) 16-bit timer mode, 16-bit timer/counter THx and TLx are cascaded, no prescalar
c) 8-bit auto reload mode, 8-bit auto reload time/counter; THx holds a value which is to be reloaded into TLx each time it overflows
d) Spilt timer mode

Answer: d

27. Function of IE1 in TCON register?
a) External interrupt 1 Edge flag. Not related to timer operations
b) External interrupt 1 Edge flag. Not related to timer operations

c) External interrupt 0 single type control bit
d) External interrupt 1 to be triggered by a falling edge signal

Answer: a

28. 8051 controller contains how many registers?
a) 5
b) 3
c) 1
d) 2

Answer: d

29. General purpose memory is called as _____
a) ROM memory
b) RAM memory
c) SRAM memory
d) EPROM memory

Answer: b

30. Which timer register has both timers in it?
a) TMOD
b) TCON
c) Both TMOD and TCON
d) Neither TMOD nor TCON

Answer: a

31. How many registers can be utilized to write the programs by an effective selection of register bank in program status word (PSW)?
a. 8
b. 16
c. 32
d. 64
ANSWER: (c) 32

32. Which operations are performed by stack pointer during its incremental phase?
a. Push
b. Pop

c. Return
d. All of the above
ANSWER: (a) Push

33) Which is the only register without internal on-chip RAM address in MCS-51?
a. Stack Pointer
b. Program Counter
c. Data Pointer
d. Timer Register
ANSWER: (b) Program Counter

34) What kind of instructions usually affect the program counter?
a.Call & Jump
b. Call & Return
c. Push & Pop
d. Return & Jump
ANSWER: (a) Call & Jump4

35) What is the default value of stack once after the system undergoes the reset condition?
a. 07H
b. 08H
c. 09H
d. 00H
ANSWER:(a) 07H

36) Which bit/s play/s a significant role in the selection of a bank register of Program Status Word (PSW)?
a.RS1
b. RS0
c. Both a & b
d. None of the above
ANSWER: (c) Both a & b

37) Which flags represent the least significant bit (LSB) and most significant bit (MSB) of Program Status Word (PSW) respectively?
a. Parity Flag & Carry Flag
b. Parity Flag & Auxiliary Carry Flag
c. Carry Flag & Overflow Flag
d. Carry Flag & Auxiliary Carry Flag
ANSWER: (a) Parity Flag & Carry Flag

38) Which register bank is supposed to get selected if the values of register bank select bits RS1 & Rs0 are detected to be '1' & '0' respectively?
a.Bank 0
b. Bank 1
c. Bank 2
d. Bank 3
ANSWER: (c) Bank 2

39) It is possible to set the auxiliary carry flag while performing addition or subtraction operations only when the carry exceeds _____
a. 1st bit
b. 2nd bit
c. 3rd bit
d. 4th bit
ANSWER: (c) 3rd bit

40) Which locations of 128 bytes on-chip additional RAM are generally reserved for special functions?
a. 80H to 0FFH
b. 70H to 0FFH
c. 90H to 0FFH
d. 60H to 0FFH
ANSWER: (a) 80H to 0FFH

41) Which commands are used for addressing the off-chip data and associated codes respectively by data pointer?
a. MOVX & MOVC

b. MOVY & MOVB
c. MOVZ & MOVA
d. MOVC & MOVY
ANSWER: (a) MOVX & MOVC

42) Which instruction find its utility in loading the data pointer with 16 bits immediate data?
a. MOV
b. INC
c. DEC
d. ADDC
ANSWER: (a) MOV

43) What is the maximum capability of addressing the off-chip data memory & off-chip program memory in a data pointer?
a. 8K
b. 16K
c. 32K
d. 64K
ANSWER: (d) 64K

44) Which among the below stated registers does not belong to the category of special function registers?
a. TCON & TMOD
b. TH0 & TL0
c. P0 & P1
d. SP & PC
ANSWER: (d) SP & PC

45) What is the required baud rate for an efficient operation of serial port devices in 8051 microcontroller?
a. 1200
b. 2400
c. 4800
d. 9600
ANSWER: (d) 9600

46) Which among the below mentioned functions does not belong to the category of alternate functions usually performed by Port 3 (Pins 10-17)?
a. External Interrupts
b. Internal Interrupts
c. Serial Ports
d. Read / Write Control signals
ANSWER: (b) Internal Interrupts

47) Which output control signal is activated after every six oscillator periods while fetching the external program memory and almost remains high during internal program execution?
a. ALE
b. PSEN
c. EA
d. All of the above
ANSWER: (b) PSEN

48) Which memory allow the execution of instructions till the address limit of 0FFFH especially when the External Access (EA) pin is held high?
a.Internal Program Memory
b. External Program Memory
c. Both a & b
d. None of the above
ANSWER: (a) Internal Program Memory

49) Which signal from CPU has an ability to respond the clocking value of D-flipflop (bit latch) from the internal bus?
a. Write-to-Read Signal
b. Write-to-Latch Signal
c. Read-to-Write Signal
d. Read-to-Latch Signal
ANSWER: (b) Write-to-Latch Signal

50) The upper 128 bytes of an internal data memory from 80H through FFH usually represent _____.
a. general-purpose registers
b. special function registers
c. stack pointers
d. program counters
ANSWER: (b) special function registers

51) What is the bit addressing range of addressable individual bits over the on-chip RAM?
a.00H to FFH
b. 01H to 7FH
c. 00H to 7FH
d. 80H to FFH
ANSWER: (c) 00H to 7FH

52) What is the divisional range of program memory for internal and external memory portions respectively when enable access pin is held high (unity)?
a. 0000H – 0FFFH & 1000H – FFFFH
b. 0000H – 1000H & 0FFFH – FFFFH
c. 0001H – 0FFFH & 01FFH – FFFFH
d. None of the above
ANSWER: (a) 0000H – 0FFFH & 1000H – FFFFH

53) Consider the following statements. Which of them is/are correct in case of program execution related to program memory?
a. External Program memory execution takes place from 1000H through 0FFFFH only when the status of EA pin is high (1)
b. External Program memory execution takes place from 0000H through 0FFFH only when the status of EA pin is low (0)
c. Internal Program execution occurs from 0000H through 0FFFH only when the status of EA pin is held low (0)
d. Internal program memory execution occurs from 0000H through 0FFFH only when EA pin is held high (1)
A & C

b. B & D
c. A & B
d. Only A
ANSWER: (b) B & D

54) How does the processor respond to an occurrence of the interrupt?
a. By Interrupt Service Subroutine
b. By Interrupt Status Subroutine
c. By Interrupt Structure Subroutine
d. By Interrupt System Subroutine
ANSWER: (a) By Interrupt Service Subroutine

55) Which location specify the storage/loading of vector address during the interrupt generation?
a. Stack Pointer
b. Program Counter
c. Data Pointer
d. All of the above
ANSWER: (b) Program Counter

56) Match the following :
a. ISS ———————————— 1. Monitors the status of interrupt pin
b. IER ———————————— 2. Allows the termination of ISS
c. RETI ———————————— 3. MCS-51 Interrupts Initialization
d. INTO ———————————— 4. Occurrence of high to low transition level
A-1, B-2, C-3, D-4
b. A-3, B-2, C-4, D-1
c. A-1, B-3, C-2, D-4
d. A-4, B-3, C-2, D-1
ANSWER:(c) A-1, B-3, C-2, D-4

57) Which among the below mentioned reasons is/are responsible for the generation of Serial Port Interrupt?
a. Overflow of timer/counter 1
b. High to low transition on pin INT1

c. High to low transition on pin INT0
d. Setting of either TI or RI flag
a. A & B
b. Only B
c. C & D
d. Only D
ANSWER: (d) Only D

58) What is the counting rate of a machine cycle in correlation to the oscillator frequency for timers?
1 / 10
b. 1 / 12
c. 1 / 15
d. 1 / 20
ANSWER: (b) 1 / 12

59) Which special function register play a vital role in the timer/counter mode selection process by allocating the bits in it?
a. TMOD
b. TCON
c. SCON
d. PCON
ANSWER:(a) TMOD

60) How many machine cycle/s is/are executed by the counters in 8051 in order to detect '1' to '0' transition at the external pin?
a. One
b. Two
c. Four
d. Eight
ANSWER: (b) Two

61) Which bit must be set in TCON register in order to start the 'Timer 0' while operating in 'Mode 0'?
a. TR0

b. TF0
c. IT0
d. IE0
ANSWER: (a) TR0
62)

62) Consider the below generated program segment for initializing Timer 1 in Mode 1 operation :

```
MOV SP, # 54 H
MOV TMOD ,# 0010 0000 C
SET C ET1
SETC TR0
SJMP $
```

a.Which among the below mentioned program segments represent the correct code?

```
MOV SP, # 54 H
MOV TCON ,# 0010 0000 C
SETC ET1
SETC TR0
SJMP $
```

b. MOV SP, # 54H

```
MOV TMOD ,# 0010 0000 C
SETC ET0
SETC TR0
SJMP $
```

c. MOV SP, # 54 H

```
MOV TMOD ,# 0010 0000 C
SETC ET1
SETC TR1
SETC EA
SJMP $
```

d. MOV SP, # 54 H

```
MOV TMOD ,# 0010 0000 C
SETC ET0
SETC TR1
```

SETC EA
SJMP $

ANSWER: (c)
MOV SP, # 54 H
MOV TMOD ,# 0010 0000 C
SETC ET1
SETC TR1
SETC EA
SJMP $

63) What is the maximum delay generated by the 12 MHz clock frequency in accordance to an auto-reload mode (Mode 2) operation of the timer?
a. 125 µs
b. 250 µs
c. 256 µs
d. 1200 µs
ANSWER: (c) 256 µs

64) Which among the below mentioned sequence of program instructions represent the correct chronological order for the generation of 2kHz square wave frequency?
MOV TMOD, 0000 0010 B
MOV TL0, # 06H
MOV TH0, # 06H
SETB TR0
CPL p1.0
ORG 0000H
6, 5, 2, 4, 1, 3
b. 6, 1, 3, 2, 4, 5
c. 6, 5, 4, 3, 2, 1
d. 6, 2, 4, 5, 1, 3
ANSWER: (b) 6, 1, 3, 2, 4, 5

65) Why is it not necessary to specify the baud rate to be equal to the number of bits per second?

Because each bit is preceded by a start bit & followed by one stop bit

b. Because each byte is preceded by a start byte & followed by one stop byte

c. Because each byte is preceded by a start bit & followed by one stop bit

d. Because each bit is preceded by a start byte &followed by one stop byte

ANSWER: (c) Because each byte is preceded by a start bit & followed by one stop bit