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Question Paper Code : 70081

M.E./M.Tech. DEGREE EXAMINATIONS, NOVEMBER/DECEMBER 2019
Second Semester
Applied Electronics
AP 5252 – ASIC AND FPGA DESIGN
(Common to M.E. Electronics and Communication Engineering)
(Regulations 2017)

Time : Three Hours | Maximum : 100 Marks

Answer ALL questions

PART – A **(10×2=20 Marks)**

1. List the advantages and disadvantages of cell-based and array-based designs.
2. What are programmable logic devices ?
3. List the floor planning algorithms.
4. What are the goals and objectives of routing ?
5. Define critical path delay, setup time and hold time.
6. Define controllability and observability.
7. Give the differences between ASIC and FPGA design.
8. What is meant by logic synthesis ?
9. Why SoC have performance oriented design ?
10. What is platform ? What are different types of platforms ?

PART – B **(5×13=65 Marks)**

11. a) What is an ASIC design ? Draw the design flow of ASIC and explain the function of each step in detail.

(OR)

b) i) Explain the memory architectures and building blocks with neat diagram. **(8)**

ii) Draw the PLA structure for the function F1 = xy + yz + x′z. **(5)**

12. a) Write the floor planning goals and objectives. What is logical partitioning and physical partitioning ? Explain the partitioning algorithms.

(OR)

b) What is meant by detailed routing ? What are the routing constraints ? Explain the algorithms for the detailed routing.

13. a) i) Explain the different types of simulation with example. **(6)**

ii) What is ATPG ? Explain few algorithm for ATPG. **(7)**

(OR)

b) Draw the architecture of boundary scan test and explain the operation.

14. a) i) What are the components of an FPGA ? Discuss each of them in detail. **(8)**

ii) What is meant by LUT ? Realise a given Boolean function f(x, y, z) xy + z by using LUT based logic block. **(5)**

(OR)

b) Explain placement and routing concepts used for different FPGA devices.

15. a) Explain platform-based and IP based SoC design and its limitations.

(OR)

b) Discuss on SoC system level interconnection of bus based approach and discuss the AMBA standard buses.

PART – C **(1×15=15 Marks)**

16. a) Design validation is a very important SoC design consideration. Find several approaches specific to SoC design. Evaluate each from the perspective of a small SoC vendor.

(OR)

b) Draw the hardware units required in an SoC design for video conference. Explain the functions of each unit.