Reg. No. : | | | | | | | | | | | | |

Question Paper Code : 70077

M.E./M.Tech. DEGREE EXAMINATIONS, NOVEMBER/DECEMBER 2019

First Semester

Applied Electronics

AP5151 – ADVANCED DIGITAL SYSTEM DESIGN

(Common to : M.E. VLSI Design, M.E. VLSI Design and Embedded Systems)

(Regulations 2017)

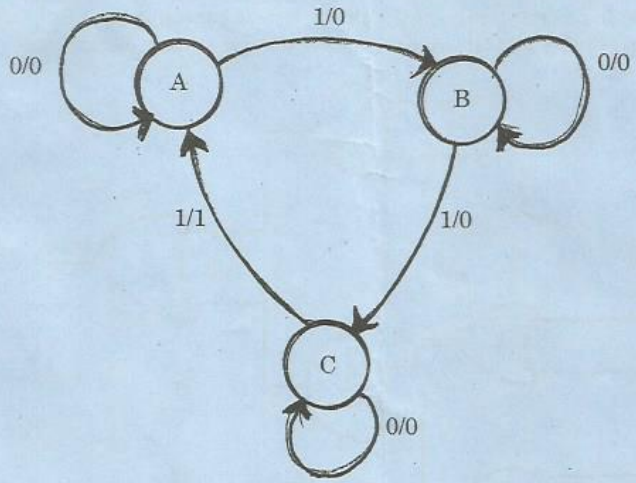
Time : Three Hours | Maximum : 100 Marks

Answer ALL questions

PART – A **(10×2=20 Marks)**

1. State the two rules for state assignment in synchronous sequential circuits.

2. Draw the ASM chart for the following state diagram :



3. What are races and cycles in asynchronous sequential circuits ?

4. What are the two types of asynchronous sequential circuits ?

5. What is primitive D cube ?

6. Sate the difference between PLA and PAL.

7. Mention any two advantages of Programmable Logic Devices.

8. Illustrate SRAM technology used in Xilinx FPGAs.

9. What is UDP in verilog ?

10. State the difference between task and function in verilog.

PART – B (5×13=65 Marks)

11. a) Design a sequential network to convert BCD to Excess-3 Code. The input and output will be serial with the least significant bit first.

(OR)

b) i) Design an iterative sequential parity-checking network which determines whether the number of ones in an n-bit word is even or odd. (5)

ii) Draw the ASM chart for a binary divider and multiplier. (8)

12. a) i) In the following logic circuit assume that inputs b, c, d are provided with 1, 1 and 1 respectively. If the input a is changing from 0 to 1, analyse the hazard present at the output F. Also design a hazard-free logic. (8)

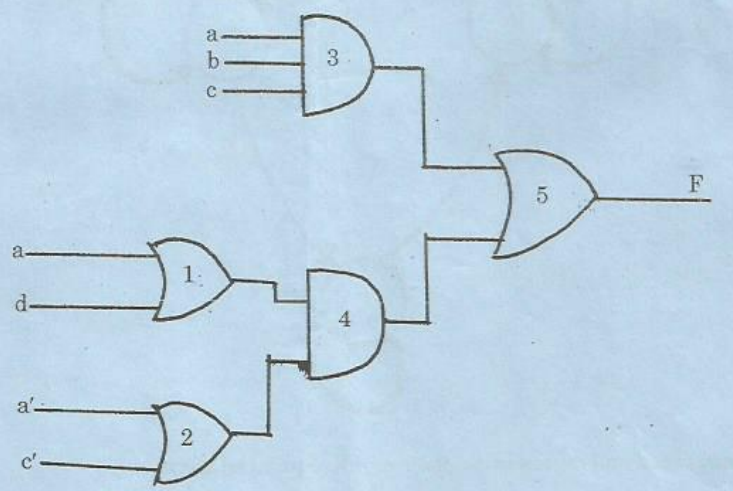


Fig.

ii) What are dynamiz hazards ? Give example. (5)

(OR)

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b) For the given flow table :

i) Find all critical races and tell why they are critical.

ii) Find all non-critical races and

iii) Find all cycles.

iv) Draw a timing diagram showing what happens to Q_1, Q_2 and Z when the network is started in state b and the input is changed from 01 to 00.

Q_1Q_2	X_1X_2				Z			
	00	01	11	10	00	01	11	10
00	(a)	c	b	c	0	0	0	0
01	c	(b)	(b)	d	1	0	1	0
11	d	(c)	b	d	0	1	0	0
10	c	(d)	b	(d)	1	1	0	0

13. a) For the logic circuit shown in Fig.

Derive the input test vector for the single stuck-at-fault in line h using.

i) Fault-table method. **(7)**

ii) Path-sensitization method. **(6)**

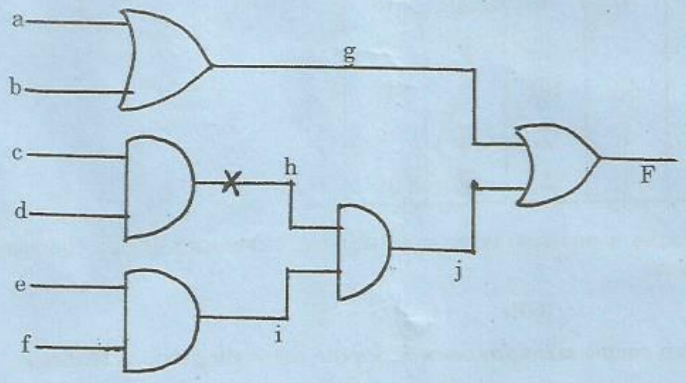

Fig.

(OR)

b) Explain :

i) D-algorithm. **(8)**

ii) Built-in Self-Test Technique. **(5)**

14. a) Design a 2-bit up-down counter and implement it using suitable PLA.

(OR)

b) i) Explain the types of interconnects used in FPGAs. (5)

ii) With neat sketch, explain the Configurable Logic Block (CLB) of a Xilinx 4000 series FPGA. (8)

15. a) i) Design a full adder and write the verilog code using structural modeling. (5)

ii) Design a 2-bit parallel-in parallel-out shift register and write the verilog code to realize it using behavioral modeling. (8)

(OR)

b) Design a multiplier and write the verilog code to realize it using behavioral modeling.

PART – C (1×15=15 Marks)

16. a) Make a proper state assignment for the following table and give the expanded table.

	X_1X_2			
	00	01	11	10
a	①	7	②	10
b	5	③	9	4
c	⑤	⑥	8	10
d	1	⑦	⑧	4
e	1	3	⑨	⑩

Also make a one-hot assignment for the table and derive the next-state equations.

(OR)

b) Design a simple microprocessor and write the verilog code to realize it.

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