Reg. No. : | | | | | | | | | | | | |

Question Paper Code : 10504

M.E./M.Tech. DEGREE EXAMINATIONS, APRIL/MAY 2019.

First Semester

Computer Science and Engineering

CP 5152 — ADVANCED COMPUTER ARCHITECTURE

(Common to M.E. Computer Science and Engineering (With Specialization in Networks)/M.E. Multimedia Technology/M.Tech. Information Technology)

(Regulation 2017)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Define : Instruction level parallelism.
2. Define : Dynamic scheduling.
3. List any four techniques used for cache optimization.
4. State the need for virtual memory.
5. Define : Cache coherence problem.
6. State the types of Interconnection networks.
7. State some unique features of IBM cell architecture.
8. State the salient features of Cloud computing.
9. Define : SIMD.
10. State the need for Graphic processing unit.

PART B — (5 × 13 = 65 marks)

11. (a) Describe the issues to be considered in Measuring, reporting and summarizing performance. (13)

Or

(b) Explain the concepts and challenges in ILP. (13)

12. (a) Examine the role of advanced memory optimization on the performance of cache. (13)

Or

(b) Explain the virtual memory translation and TLB with necessary diagram. (13)

13. (a) Illustrate the implementation of various symmetric-shared memory architecture. (13)

Or

(b) What is the need for Interconnection networks? List the different types and explain any two interconnection networks in detail. (13)

14. (a) Design a Snoopy cache coherence protocol for a shared memory multiprocessor with a write back policy, that will reduce the overhead associated during the memory write operation and minimize the number of bus transactions. (13)

Or

(b) Describe the architecture of the IBM cell processor in detail. (13)

15. (a) With suitable illustrations explain the vector architecture in detail. (13)

Or

(b) Explain the principle behind detecting and enhancing loop level parallelism. (13)

PART C — (1 × 15 = 15 marks)

16. (a) Consider three different processors P1, P2 and P3 executing the same instruction set. Processor P1 has a 3 GHz clock rate and a CPI of 1.5. P2 has a 2.5 GHz clock rate and a CPI of 1.0. P3 has a 4 GHz clock rate and a CPI of 2.2. Which processor has the highest performance expressed in instructions per second? If the processors each execute a program in 10 seconds, find the number of cycles and the number of instructions. We are trying to reduce the execution time to 30% but this leads to an increase of 20% in CPI. What clock rate should we have to get this time reduction? (15)

Or

(b) With suitable case study explain the working principle of Google warehouse. (15)